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The S-4544A is a 17- or 33-common, 128-segment output graphic (bit map) LCD controller-driver with built-in 8-bit and serial interfaces. The internal 65 x 128 bit display data RAM can directly access the 8-bit and the serial data bus, making the display of both graphics and characters possible. It displays the data independently of the CPU through the built-in oscillating circuit or clock input. It has a wide variety of command instructions which minimize the load onto the CPU. It also features a wide voltage range and the low power consumption during display, making the S-4544A a suitable display for system applications in portable electronics.

FEATURES

- Interface
  8-bit 80/68-Family Microcomputer Interface Serial Interface
- Driver Output
  128 segments
  17 commons: Command Setting
  33 commons: Default
- Display Data RAM
  65×128 bits
- Display Clock
  Both built-in CR oscillating circuit and external clock input are available.
  Oscillating Frequency: 18 kHz
- Duty Cycle
  1/17: Command Setting
  1/33: Default
- LCD Bias Resistor
  Internal 1/6.7: Default
  Internal 1/5: Command Setting
  Internal 1/4: Command Setting
  External 1/2 to 1/4
- Commands
  Display ON/OFF, Display Start Line Set, Page Address Set, Column Address Set, Status Read, Display All-Lit, Display Normal/Reverse, Display Data Read/Write, ADC Select, Duty Cycle Selection, Alternate Common Output, Reset, Power Save, Read/Modify/Write, Bias Select, Icon Only Display
- Voltage Range
  Logic: -2.4 V to -5.5 V
  LCD drive: -2.7 V to -11.0 V
- Low Current Consumption (Low Power Consumption)
  typ. 110μA for CR oscillation 18 kHz, Vss=-5V, Dual Booster and V5=-8V
- Delivered on
  Gold bumps (bare chips)
  TCP
- Other
  Power Save Current Consumption:
  1 μA or less (actually 1 nA or less)
  Smooth scrolling
  Blinking is possible
  Dual/Triple Booster
  Built-in 1/4, 1/5, 1/6.7 Bias Resistor
  Built-in LCD Power Supply Circuit
  Built-in LCD Drive Voltage Command Fine Adjustment Circuit
  2 Internal Icon Common Output Systems

■ BLOCK DIAGRAM

1. Block Overview

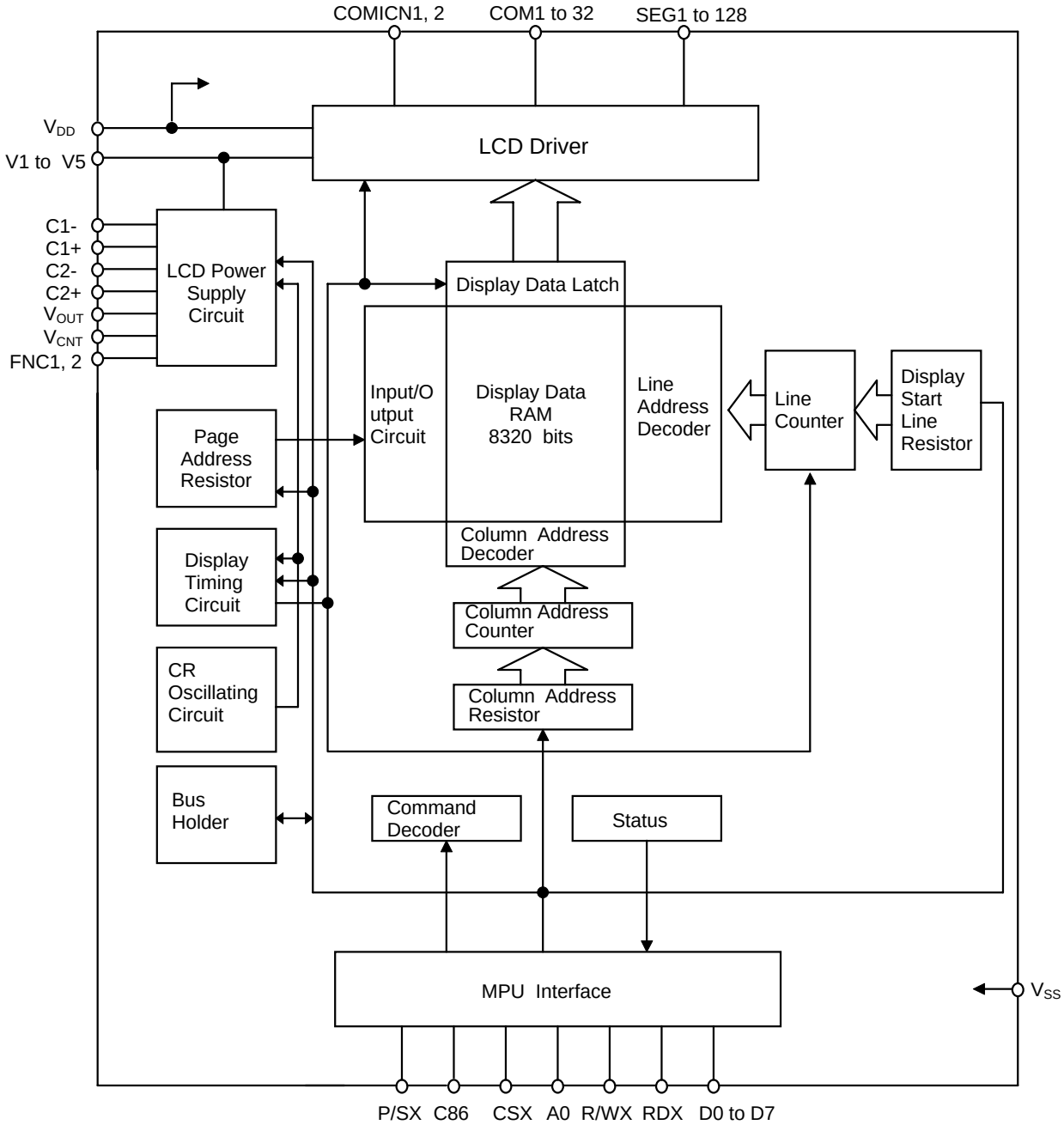


Figure 1 Block Overview

2. LCD Power Supply Circuit Block Diagram

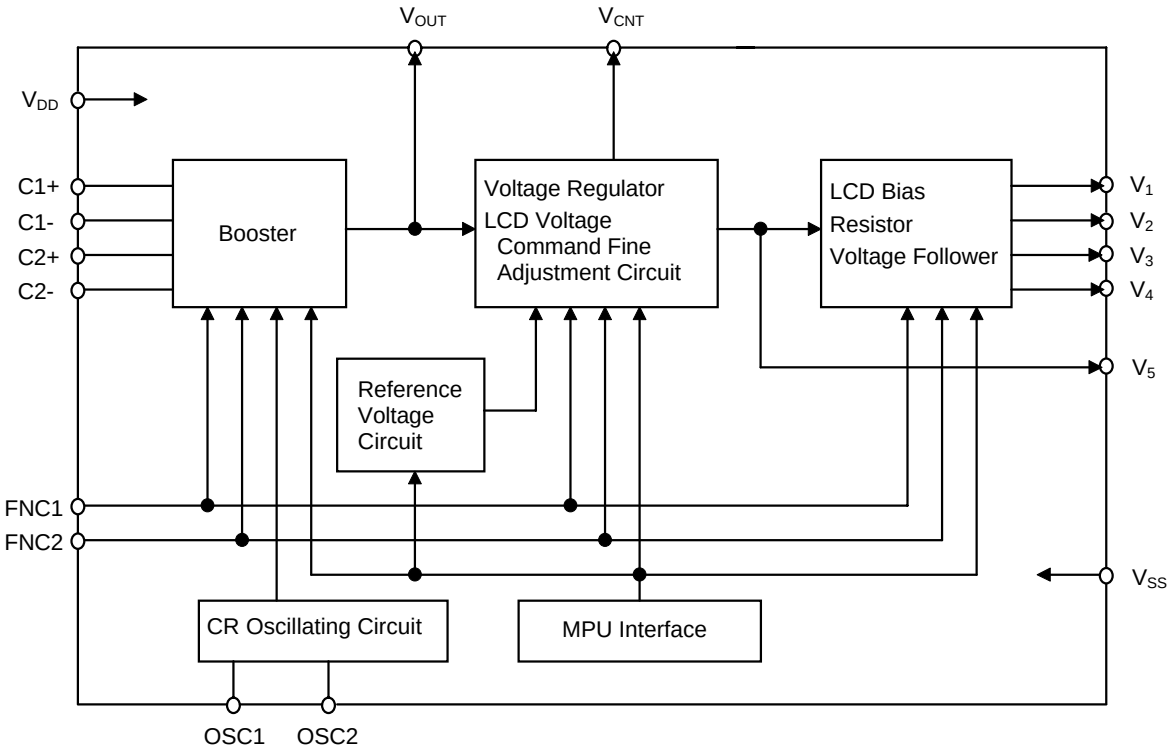


Figure 2 LCD Power Supply Circuit Block Diagram

■ PIN DESCRIPTION

1. Logic Circuit Power Supply Pins

Table 1 Logic Circuit Power Supply Pins

Pin No.	Pin Name	Description
20 , 39	VSS	Negative power supply: Usually connected to -3 or -5 V.
10 , 58	VDD	Positive power supply: Usually connected to 0 V.

2. Control Pins

Table 2 Control Pins

Pin No.	Pin Name	Description
12	CSX	Chip-select input Active “L”
13	A0	Display data or display control command change Usually connected to the lowermost bit of the MPU address bus A0=“0”: DB0 to DB7: Control command input. A0=“1”: DB0 to DB7: Display data input and outputs
14	R / WX	[68-family MPU] Read/write signal input R/WX=“H”: Read R/WX=“L”: Write [80-family MPU] Write signal input Active “L” Data bus output state
15	RDX	[68-family MPU] Enable clock signal input Active “H” [80-family MPU] Read signal input Active “L” Data bus output state
16	P / SX	Parallel/serial interface change P/SX=“H”: 8-bit parallel interface P/SX=“L”: Serial interface
17	C86	MPU interface select C86=“H”: 68-family interface C86=“L”: 80-family interface
25	D0	P/SX="H": 8-bit configuration data bus connection 3-state input/output configuration P/SX="L": Serial interface connection D0 Serial data input D1 Serial clock input D2 Serial data output
26	D1	
28	D2	
29	D3	
31	D4	
32	D5	
34	D6	
35	D7	

3. CR Oscillation Pins

Table 3 CR Oscillation Pins

Pin No.	Pin Name	Description
18	OSC2	CR oscillating circuit output. Connects oscillation resistor Rf.
19	OSC1	CR oscillating circuit input. Connects oscillation resistor Rf.

4. LCD Drive Voltage Pins

Table 4 LCD Drive Voltage Pins

Pin No.	Pin Name	Description
37	FNC2	LCD power supply circuit operation control pin 2. Connected to VDD or VSS only.
38	FNC1	LCD power supply circuit operation control pin 1. Connected to VDD or VSS only.
42	VOUT	Boosting voltage output
46	C2-	2nd-step boosting capacitor negative connection
49	C2+	2nd-step boosting capacitor positive connection
50	C1-	1st-step boosting capacitor negative connection
51	C1+	1st-step boosting capacitor positive connection
57	VCNT	LCD power supply voltage control
59	V1	LCD drive bias voltage • Outputs LCD drive bias voltage when using a built-in LCD power supply circuit. 1/ 4 bias: V1 1 / 4×V5, V2 2 / 4×V5, V3 2 / 4×V5, V4 3 / 4×V5 1 / 5 bias: V1 1 / 5×V5, V2 2 / 5×V5, V3 3 / 5×V5, V4 4 / 5×V5 1 / 6.75 bias: V1 1 / 6.75×V5, V2 2 / 6.75×V5, V3 4.75 / 6.75×V5, V4 5.75 / 6.75×V5 • Inputs LCD drive bias voltage when using an external LCD power supply circuit. VDD≥ V1, V2, V3, V4≥ V5, VSS≥V5
60	V2	
61	V3	
62	V4	
63	V5	

5. Driver Output Pins

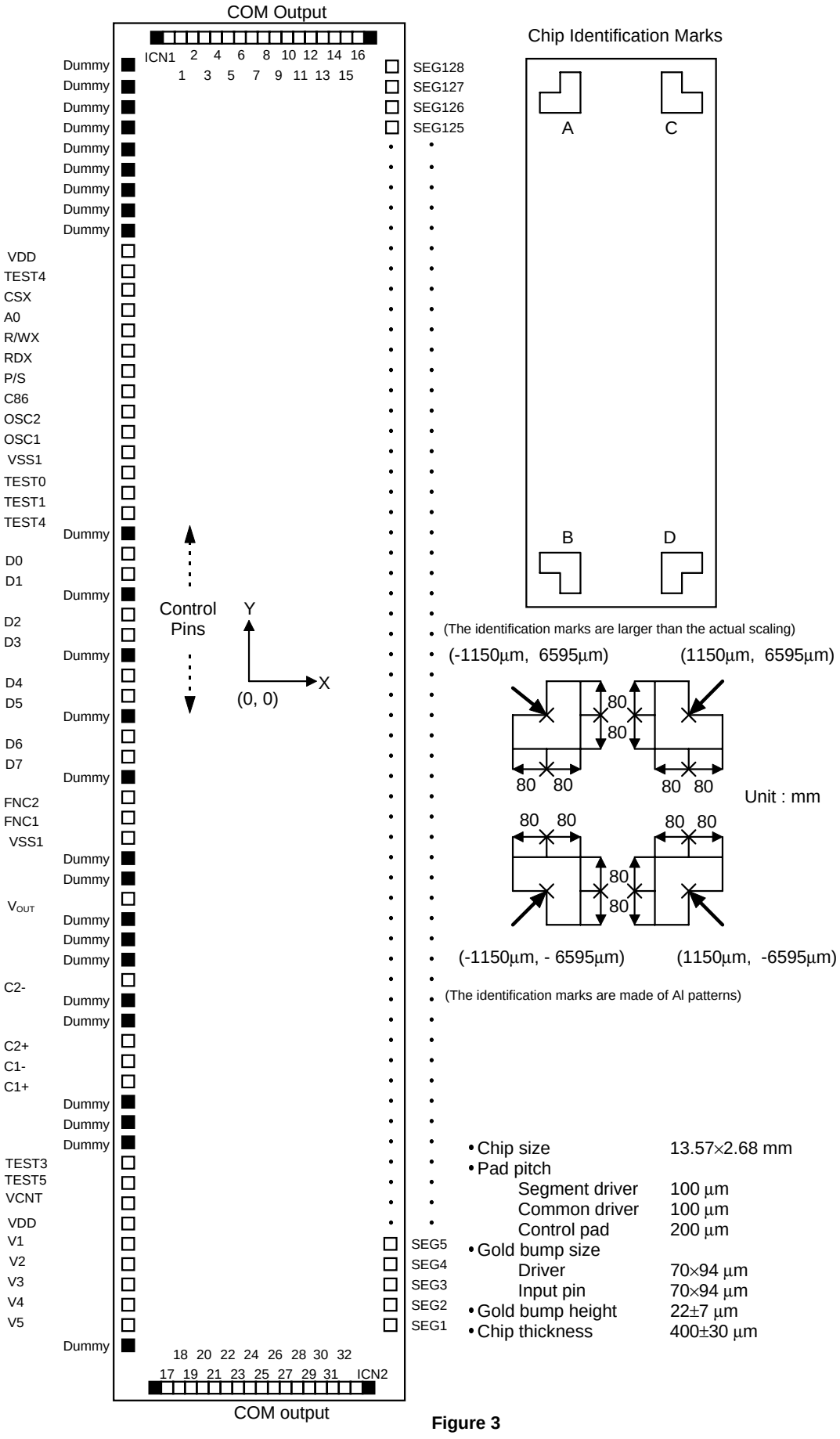
Table 5 Driver Output Pins

Pin No.	Pin Name	Description
84 to 211	SEG1 to SEG128	Segment drive output
66 to 81 213 to 228	COM1 to COM32	Common drive output
229 82	COMICN1 COMICN2	Icon common drive output: COMICN1 and COMICN2 output the same phase waveform.

6. Other Pins Table 6

Pin No.	Pin Name	Description
1 to 9 24, 27, 30 33, 36, 40, 41 43 to 45, 47, 48 52 to 54, 64, 65 83, 212, 230	Dummy	Dummy: Insulated from the inside of the IC.
11	TEST4	IC delivery test. Cannot be wired to the outside. Open when in use.
21	TEST0	
22	TEST1	
23	TEST2	
55	TEST3	
56	TEST5	

■ PAD ASSIGNMENT



- Chip size 13.57×2.68 mm
- Pad pitch
  - Segment driver 100 μm
  - Common driver 100 μm
  - Control pad 200 μm
- Gold bump size
  - Driver 70×94 μm
  - Input pin 70×94 μm
- Gold bump height 22±7 μm
- Chip thickness 400±30 μm

Figure 3

■ PAD COORDINATES

Table 7-1 Pad Coordinates

Unit: μm (The origin is the center of the chip)

No.	Pin Name	X	Y	No.	Pin Name	X	Y
1	Dummy	-1191	6250	64	Dummy	-1191	-6350
2	Dummy	-1191	6050	65	Dummy	-900	-6636
3	Dummy	-1191	5850	66	COM17	-800	-6636
4	Dummy	-1191	5650	67	COM18	-700	-6636
5	Dummy	-1191	5450	68	COM19	-600	-6636
6	Dummy	-1191	5250	69	COM20	-500	-6636
7	Dummy	-1191	5050	70	COM21	-400	-6636
8	Dummy	-1191	4850	71	COM22	-300	-6636
9	Dummy	-1191	4650	72	COM23	-200	-6636
10	VDD	-1191	4450	73	COM24	-100	-6636
11	TEST4	-1191	4250	74	COM25	0	-6636
12	CSX	-1191	4050	75	COM26	100	-6636
13	A0	-1191	3850	76	COM27	200	-6636
14	R/WX	-1191	3650	77	COM28	300	-6636
15	RDX	-1191	3450	78	COM29	400	-6636
16	P/SX	-1191	3250	79	COM30	500	-6636
17	C86	-1191	3050	80	COM31	600	-6636
18	OSC2	-1191	2850	81	COM32	700	-6636
19	OSC1	-1191	2650	82	COMICN2	800	-6636
20	VSS	-1191	2450	83	Dummy	900	-6636
21	TEST0	-1191	2250	84	SEG1	1191	-6350
22	TEST1	-1191	2050	85	SEG2	1191	-6250
23	TEST2	-1191	1850	86	SEG3	1191	-6150
24	Dummy	-1191	1650	87	SEG4	1191	-6050
25	D0	-1191	1450	88	SEG5	1191	-5950
26	D1	-1191	1250	89	SEG6	1191	-5850
27	Dummy	-1191	1050	90	SEG7	1191	-5750
28	D2	-1191	850	91	SEG8	1191	-5650
29	D3	-1191	650	92	SEG9	1191	-5550
30	Dummy	-1191	450	93	SEG10	1191	-5450
31	D4	-1191	250	94	SEG11	1191	-5350
32	D5	-1191	50	95	SEG12	1191	-5250
33	Dummy	-1191	-150	96	SEG13	1191	-5150
34	D6	-1191	-350	97	SEG14	1191	-5050
35	D7	-1191	-550	98	SEG15	1191	-4950
36	Dummy	-1191	-750	99	SEG16	1191	-4850
37	FNC2	-1191	-950	100	SEG17	1191	-4750
38	FNC1	-1191	-1150	101	SEG18	1191	-4650
39	VSS	-1191	-1350	102	SEG19	1191	-4550
40	Dummy	-1191	-1550	103	SEG20	1191	-4450
41	Dummy	-1191	-1750	104	SEG21	1191	-4350
42	VOUT	-1191	-1950	105	SEG22	1191	-4250
43	Dummy	-1191	-2150	106	SEG23	1191	-4150
44	Dummy	-1191	-2350	107	SEG24	1191	-4050
45	Dummy	-1191	-2550	108	SEG25	1191	-3950
46	C2-	-1191	-2750	109	SEG26	1191	-3850
47	Dummy	-1191	-2950	110	SEG27	1191	-3750
48	Dummy	-1191	-3150	111	SEG28	1191	-3650
49	C2+	-1191	-3350	112	SEG29	1191	-3550
50	C1-	-1191	-3550	113	SEG30	1191	-3450
51	C1+	-1191	-3750	114	SEG31	1191	-3350
52	Dummy	-1191	-3950	115	SEG32	1191	-3250
53	Dummy	-1191	-4150	116	SEG33	1191	-3150
54	Dummy	-1191	-4350	117	SEG34	1191	-3050
55	TEST3	-1191	-4550	118	SEG35	1191	-2950
56	TEST5	-1191	-4750	119	SEG36	1191	-2850
57	VCNT	-1191	-4950	120	SEG37	1191	-2750
58	VDD	-1191	-5150	121	SEG38	1191	-2650
59	V1	-1191	-5350	122	SEG39	1191	-2550
60	V2	-1191	-5550	123	SEG40	1191	-2450
61	V3	-1191	-5750	124	SEG41	1191	-2350
62	V4	-1191	-5950	125	SEG42	1191	-2250
63	V5	-1191	-6150	126	SEG43	1191	-2150

Table 7-2 Pad Coordinates

No.	Pin Name	X	Y	No.	Pin Name	X	Y
127	SEG44	1191	-2050	179	SEG96	1191	3150
128	SEG45	1191	-1950	180	SEG97	1191	3250
129	SEG46	1191	-1850	181	SEG98	1191	3350
130	SEG47	1191	-1750	182	SEG99	1191	3450
131	SEG48	1191	-1650	183	SEG100	1191	3550
132	SEG49	1191	-1550	184	SEG101	1191	3650
133	SEG50	1191	-1450	185	SEG102	1191	3750
134	SEG51	1191	-1350	186	SEG103	1191	3850
135	SEG52	1191	-1250	187	SEG104	1191	3950
136	SEG53	1191	-1150	188	SEG105	1191	4050
137	SEG54	1191	-1050	189	SEG106	1191	4150
138	SEG55	1191	-950	190	SEG107	1191	4250
139	SEG56	1191	-850	191	SEG108	1191	4350
140	SEG57	1191	-750	192	SEG109	1191	4450
141	SEG58	1191	-650	193	SEG110	1191	4550
142	SEG59	1191	-550	194	SEG111	1191	4650
143	SEG60	1191	-450	195	SEG112	1191	4750
144	SEG61	1191	-350	196	SEG113	1191	4850
145	SEG62	1191	-250	197	SEG114	1191	4950
146	SEG63	1191	-150	198	SEG115	1191	5050
147	SEG64	1191	-50	199	SEG116	1191	5150
148	SEG65	1191	50	200	SEG117	1191	5250
149	SEG66	1191	150	201	SEG118	1191	5350
150	SEG67	1191	250	202	SEG119	1191	5450
151	SEG68	1191	350	203	SEG120	1191	5550
152	SEG69	1191	450	204	SEG121	1191	5650
153	SEG70	1191	550	205	SEG122	1191	5750
154	SEG71	1191	650	206	SEG123	1191	5850
155	SEG72	1191	750	207	SEG124	1191	5950
156	SEG73	1191	850	208	SEG125	1191	6050
157	SEG74	1191	950	209	SEG126	1191	6150
158	SEG75	1191	1050	210	SEG127	1191	6250
159	SEG76	1191	1150	211	SEG128	1191	6350
160	SEG77	1191	1250	212	Dummy	900	6636
161	SEG78	1191	1350	213	COM16	800	6636
162	SEG79	1191	1450	214	COM15	700	6636
163	SEG80	1191	1550	215	COM14	600	6636
164	SEG81	1191	1650	216	COM13	500	6636
165	SEG82	1191	1750	217	COM12	400	6636
166	SEG83	1191	1850	218	COM11	300	6636
167	SEG84	1191	1950	219	COM10	200	6636
168	SEG85	1191	2050	220	COM9	100	6636
169	SEG86	1191	2150	221	COM8	0	6636
170	SEG87	1191	2250	222	COM7	-100	6636
171	SEG88	1191	2350	223	COM6	-200	6636
172	SEG89	1191	2450	224	COM5	-300	6636
173	SEG90	1191	2550	225	COM4	-400	6636
174	SEG91	1191	2650	226	COM3	-500	6636
175	SEG92	1191	2750	227	COM2	-600	6636
176	SEG93	1191	2850	228	COM1	-700	6636
177	SEG94	1191	2950	229	COMICN1	-800	6636
178	SEG95	1191	3050	230	Dummy	-900	6636

Chip Identification Mark Coordinates (Al pattern)

	Chip Identification Mark	X	Y		Chip Identification Mark	X	Y
	A	-1150	6595		C	1150	6595
	B	-1150	-6595		D	1150	-6595

■ OPERATION

1. Powering ON

Input the Display OFF command immediately after the CPU starts to operate at powering ON. Unnecessary character display can be prevented by inputting the Display OFF command. Connect and fix pins C86, P/SX, FNC1 and FNC2 to the V_{DD} or V_{SS}.

Recommended Command Setting Sequence at Powering ON:

① Display Screen Setting
- Display OFF
  D0: 0 Display OFF — Once the display OFF is engaged, unnecessary characters are not displayed.
- Display All-Lit ON/OFF
  D0: 0 Display All-Lit OFF — Normal display operation and the oscillation start.

② LCD Power Supply Circuit Operation Setting
- LCD Power Supply Circuit ON
  D0: 1 LCD Power Supply Circuit ON
- Bias Select
- LCD Drive Voltage Fine Adjustment Data Setting
- Icon Only Display OFF/Booster Drive Frequency Setting
  D2: 0 Normal Display
  D0, 1: Boosted Voltage Control Data
- Reference Voltage Temperature Compensation Coefficient Select

③ LCD Screen Setup
- End Command Input
- Duty Select/Alternate Common Output Select
- Display Normal/Reverse
- Display Start Line Setting
- Common Output Sequence Setting
- Icon Only Display

④ Display Start
- Display Data Write
- Display ON
  D0: 0 Display ON (Display starts)

[Note] Since the display data RAM is uncertain at powering ON, write “L” or data to be displayed in all display data RAMs before turning the display ON.

2. Powering OFF

In order to prevent unnecessary characters from being displayed during shutdown of the power, always input the display OFF command from the CPU, next shut down the power.

Recommended Command Setting Sequence at Powering OFF:

① Display OFF
D0: 1 Display OFF

② LCD Power Supply Circuit OFF
D0: 0 LCD Power Supply Circuit OFF

3. MPU Interface Select

In the S-4544A, the parallel interface or the serial interface can be selected.

Table 8 Interface Selection

P/SX Pin Logic	C86 Pin Logic	MPU Interface
H	L	80-family Interface
	H	68-family Interface
L	don't care	Serial Interface

3.1 Parallel Interface

Table 9 Connection Relationship between MPU and Pins

S-4544A Pin Name	A0	RDX	R/WX	CSX	D0 to D7
68-Family MPU Signal Name	A0	E	R/$\overline{W}$	$\overline{CS}$	D0 to D7
80-Family MPU Signal Name	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	D0 to D7

3.2 Serial Interface

P/SX : "L" Serial interface "H" Parallel Interface
CSX : "L" Chip Active "H" Chip Reset
R/WX : "L" WRITE Command "H" READ Command
A0 : "L" Command Data "H" Display Data
D0 : Serial Data Input (SDI)
D1 : Serial Clock Input (SCLK)
D2 : Serial Data Output (SDO)
D3 to D7 : Open
RDX : Open
C86 : Open

By setting P/SX to "L." the serial interface is selected. The instruction code is the same as for the parallel interface. In this case, the RDX pin should be "Open."
By setting CSX to "H," the serial interface circuit is reset and the counter is initialized. By setting CSX to "L," the serial interface circuit enters an operating state.
The commands and displayed data are written at the rising edge of the serial clock. Data is input in the order D0 to D7 in 8-bit data. The status and displayed data are read at the falling edge of the serial clock. Further displayed data reading needs dummy reading.

A0	R/WX	Operation
L	L	Inputs the command
H	H	Reads the display data
L	H	Reads the status
H	L	Writes the display data

When the serial interface is selected, the D2 pin (SDO: Serial Data Output Pin) goes "H" during reset.

Status reading in a reset operation is invalidated when the serial interface is selected. However, "H" is output to the D2 pin (SDO: Serial Data Output Pin) . Serial clock wiring must be made by considering external noise and reflecting noise. Be sure to check the operation of the equipment.

4. Command Execution Time

The command is completely executed within the cycle time (tcyc) according to the timing characteristics of the command input. Therefore, commands can be input continuously without confirming the busy flag at the Status Read mode. Reinputting the command within the cycle time is inhibited.

5. Chip Select

The MPU interface is turned to “Active” by setting CSK pin to “L”

Table 10 Chip Select Logic

CSX	State	Description
“H”	Standby	D0 to D7 : High impedance A0 : Invalid RDX : Invalid R/WX : Invalid
“L”	Active	All pins are valid

6. Data Bus Select

Table 11 Data Bus Select

	68-Family	80-Family		Description
A0	R/WX	RDX	R/WX	
1	1	0	1	Reads from Display Data RAM
1	0	1	0	Writes to Display Data RAM
0	1	0	1	Status Read
0	0	1	0	Command Read to internal register

7. Display Data RAM

The S-4544A has Display Data RAM (8-bits × 8-pages x 128 columns +128 columns =8320 bits]. It is possible to use the not-used area for display as normal SRAM. The Display /data RAM is made of dual-port RAM. The read/write access form the MPU interface is performed independently of the read access to the LC display.

At the moment power is turned on, the contents of the Display Data RAM are uncertain. Following turning on power, write “0” in all bits of the Display Data RAM or write the display data with display OFF and then turn the display ON.

8. Reading and Writing Display Data From MPU

The S-4544A reads and writes the display data through the internal bus holder. The display data is read to the bus holder from the Display Data RAM, and in the next read cycle on the data bus. Therefore, a dummy read cycle is needed before the first read cycle. When reading the display data after the column address set and the data write cycle, a dummy read is needed. Since the reading of the display data is executed using this bus holder, it is possible to read the data at high speed.
Display data is written to the Display Data RAM through the bus holder within a write cycle. Therefore, writing the display data does not need a dummy cycle.

After executing READ and WRITE commands, the column address is incremented by 1. When the cycle time represented with timing characteristics is met, READ and WRITE commands can be executed in succession. Increment of the column address stops at the upper address of the Display Data RAM.

9. Column Address

The column address of the Display Data RAM is used for reading/writing displayed data from/to the MPU. The column address is set by a command. When the displayed data RAM is accessed by the MPU, the address increments by one.

10. Page Address

The display RAM is composed of nine pages. When accessing the Display Data RAM from MPU, the page of the Display Data RAM is set by a command.

Page	D3	D2	D1	D0	
0	0	0	0	0	Graphic display area
1	0	0	0	1	Graphic display area
2	0	0	1	0	Graphic display area
3	0	0	1	1	Graphic display area
4	0	1	0	0	Graphic display area
5	0	1	0	1	Graphic display area
6	0	1	1	0	Graphic display area
7	0	1	1	1	Graphic display area
8	1	0	0	0	Icon (annunciator) display area

11. Display Start Line Address

The display start line address is a read start address of the Display Data RAM which corresponds to the COM0 output. Set the display start line address with the corresponding command. Use the Display Start Line Address set command in changing the display page or smooth scroll.

12. Reading the Display Data to LCD Panel

Regardless of the state of the MPU, the S-4544A reads the data to the LCD panel. That is, it reads a 1-line of the display data specified with the line address from the Display Data RAM to the display data latch in the display drive side. After reading 1-line address, the S-4544A increments the line address in synchronization with the common output. After reading 1-frame line address, the S-4544A reads the display data from the display start line address again.

13. Display Data Latch

The display data latch is the circuit for latching one line's display data from the Display Data RAM. The display data is output from this latch to the LCD drive circuit. Since the display ON/OFF, the display All-Lit ON/OFF and Display Normal/Reverse control the display data latch, it has no effect on the display RAM data.

14. CR Oscillation Circuit

A built-in CR oscillation circuit generates a fundamental clock which conforms to the display timing. The oscillating frequency "fosc" is approximately 18 kHz, when Rf=1 MΩ. Operation through external clock is possible when external clock is input to OSC1, and OSC2 is "Open"

	Frame Frequency	
1/17 duty	66.17 Hz	at fosc = 18 kHz
1/33 duty	68.18 Hz	at fosc = 18 kHz

15. LCD Drive Circuit

Has LCD drive output pins (i.e., 32 for common output, 2 for icon common, and 128 for segment output) and generates a 2-frame AC drive waveform (type B). 2 icon common output pins which are configured oppositely to the chip generate a drive waveform at the same timing. The icon display can be assigned the top or the bottom of the LCD panel. When the icon display is in no use, turn the icon common output to "Open."

16. LCD Power Supply Circuit

The LCD power supply circuit consists of a doubler/tripler, an LCD voltage adjustment circuit, an LCD bias resistor, and a voltage follower. The LCD voltage adjustment circuit consists of a voltage regulator and an LCD voltage command fine adjustment circuit. The LCD power supply circuit can be controlled by pins FNC1 and 2 and the LCD power supply circuit ON/OFF command. Internal or external power supply for the doubler/tripler, voltage regulator, and LCD voltage adjustment circuit can be changed with pins FNC1 and 2.

When turning OFF the LCD power supply circuit with the ON/OFF command, the S-4544A can stop the LCD power supply circuit.

When turning OFF all of built-in LCD power supply circuits with FNC1 = "L," FNC2 = "H," the LCD power supply circuit, however, can run at LCD bias voltage V1 through V5 generated by external bias resistors.

Table 12

FNC1	FNC2	Doubler/ Tripler	Voltage Regulator	Voltage Follower/ LCD Bias Resistor	Notes
L	L	Valid	Valid	Valid	Use all of internal LCD power supply circuits.
L	H	Invalid	Invalid	Invalid	Use external bias resistors.
H	L	Invalid	Valid	Valid	Use the external power supply circuit.
H	H	Invalid	Invalid	Valid	Externally create and input V5 voltage.

Notes: • Always connect FNC1 and 2 to VDD or VSS.
• Externally-connected pins VOUT and V1 through V5 are not used as a drive power supply of other circuit.
• Externally connecting the power supply, with the built-in LCD power supply circuit ON may lead to a breakdown.

16.1 Doubler/Tripler

The voltage is boosted below VDD on a VDD basis and output to the VOUT.
To boost the voltage 3 times, connect a specified capacitor between C1+ and C1-, C2+ and C2-, and VSS and VOUT. Use the booster in the range of VSS=-2.4 to -3.6V.
To boost the voltage twice, connect a capacitor between C1+ and C1- as well as between VSS and VOUT, and connect C2- to VOUT. Turn C2+ to "Open." Use the booster in the range of VSS=-2.4 to -5.5V.

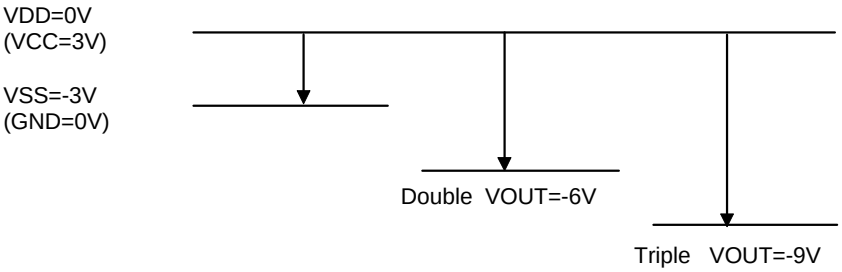


Figure Example of Booster Output

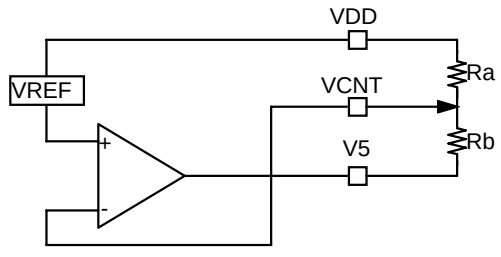
16.2 LCD Voltage Adjustment

There are two methods of adjusting the LCD voltage as follows:

16.2.1 Voltage Regulator

Voltage regulator output V5 is adjusted by externally-attached Ra and Rb.
V5 can be calculated as a resistor division ratior of built-in reference voltage VREF. The VREF with a temperature characteristics from approximately - 0.13%/°C to +0.01%/°C can compensate the LCD temperature characteristics. The value of the VREF differs depending upon the temperature compensation coefficient of the reference voltage for which the command is selected.

$$V5 = \frac{Ra+Rb}{Ra} VREF\ (V)$$



When a volume resistance is used in the resistor, V5 can be set variably. Feedback voltage noises occurring at the V_{CNT} pin directly affects on V5. Take appropriate measures against noises.

16.2.2 LCD Voltage Command Fine Adjustment Circuit

The contrast can be adjusted by adjusting V5. It is also adjusted through a corresponding command input. V5 is set by the lower 4 bits of the data bus and can be adjusted to 16 steps. It is effective to adjust V5 together with the LCD voltage command fine adjustment circuit and the voltage regulator. First, set the fine adjustment data to (0, 1, 1, 1) or (1, 0, 0, 0), and adjust to the optimum contrast using a voltage regulator. The values Ra and Rb are calculated from the fine adjustment voltage width and minimum voltage of V5 to be set. When the LCD voltage command fine adjustment circuit is not in use, set the minimum voltage to (0, 0, 0, 0).

D3	D2	D1	D0	V5	
0	0	0	0	Minimum Voltage Setting	Default
		:			
0	1	1	1		
1	0	0	0		
		:			
1	1	1	1	Maximum Voltage Setting	

16.3 LCD Bias Voltage

A built-in LCD bias resistor creates bias voltage for the LCD drive. The LCD bias can be selected among 1/6.7, 1/5, and 1/4 with the corresponding command. Since the bias voltage is supplied via the voltage follower to the LCD driver, current consumption is significantly reduced.

When FNC1 is “L” and FNC2 is “H,” it is possible to connect the externally-attached bias resistor directly to pins V1 through V5. A 1/2 or more bias ratio can be freely supplied as an LCD drive voltage. Regardless of the level, the voltage can be inputted to pins V1 through V4.
When using an externally-attached bias resistor, the S-4544A stops the voltage follower. Select an appropriate value of resistance of the bias resistor according to the size of the LCD panel and LC capacity.

16.4 Voltage Follower

The voltage follower buffers the LCD bias voltage created by the built-in bias resistor, and supplies it to the LCD drive circuit. At the same time, the LCD bias voltage is output to pins V1 through V4. Thus, connect a capacitor in accordance with the size and capacity of the LCD panel to stabilize the LCD bias voltage. It is not possible to output the LCD bias voltage from pins V1 through V5 or supply the LCD bias voltage to other circuits.

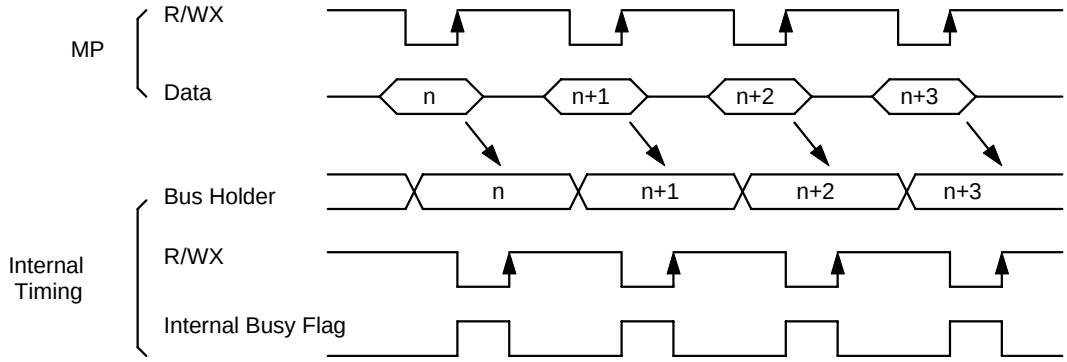
16.5 Reference Voltage Circuit

The reference voltage circuit generates VREF reference voltage of the voltage regulator. There are two values of VREF depending upon the temperature coefficient. For details, refer to “COMMAND EXPLANATION, 20. Reference Voltage Temperature Compensation Coefficient Selection.”

■ INTERFACE

1. Parallel Interface

1.1 Display Data Write (Example of the 80-Family interface)



1.2 Display Data Read (Example of the 80-Family interface)

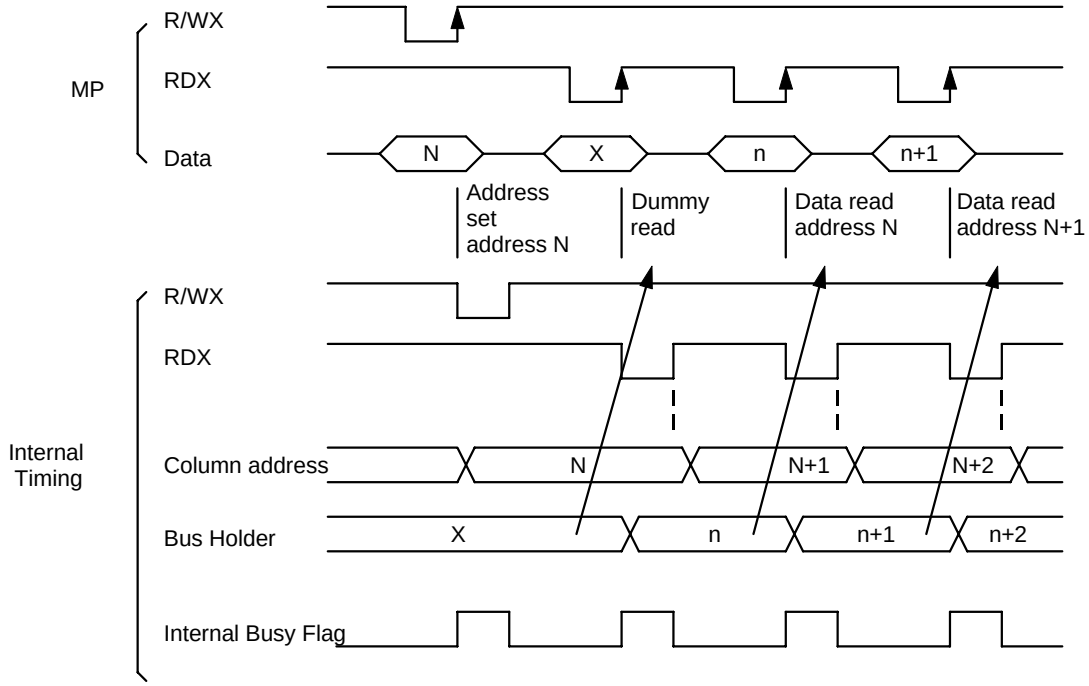
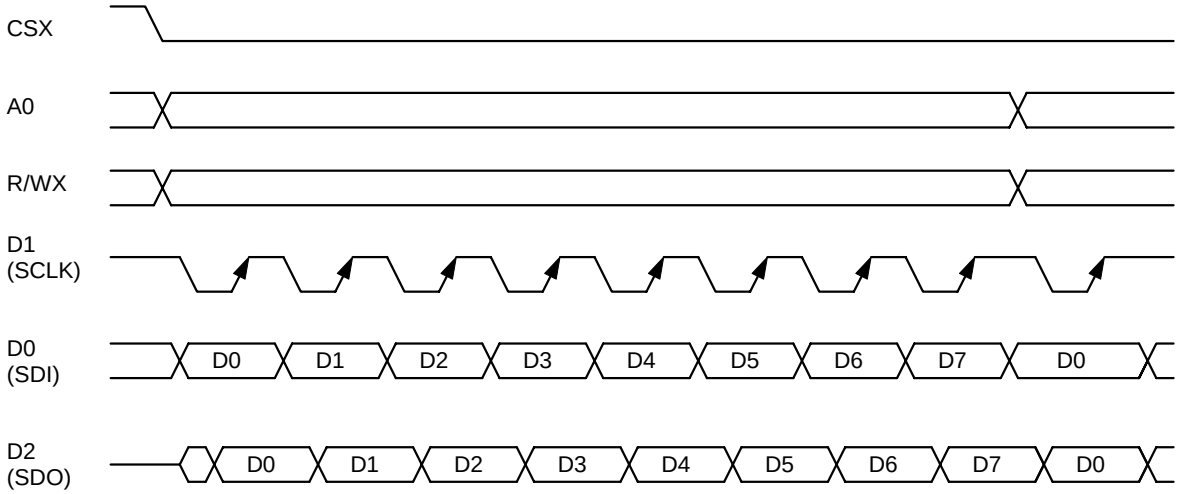


Figure4 Parallel Interface Examples

2. Serial interface



A0	R/WX	D0 (SDI)	D2 (SDO)
0	0	Command Write	Status Read
0	1	Invalid	Status Read
1	0	Data Write	Status Read
1	1	Invalid	Data Read (Note)

Note: Data Read needs a dummy read.

Figure 5 Serial interface Display Data Write/Read Timing

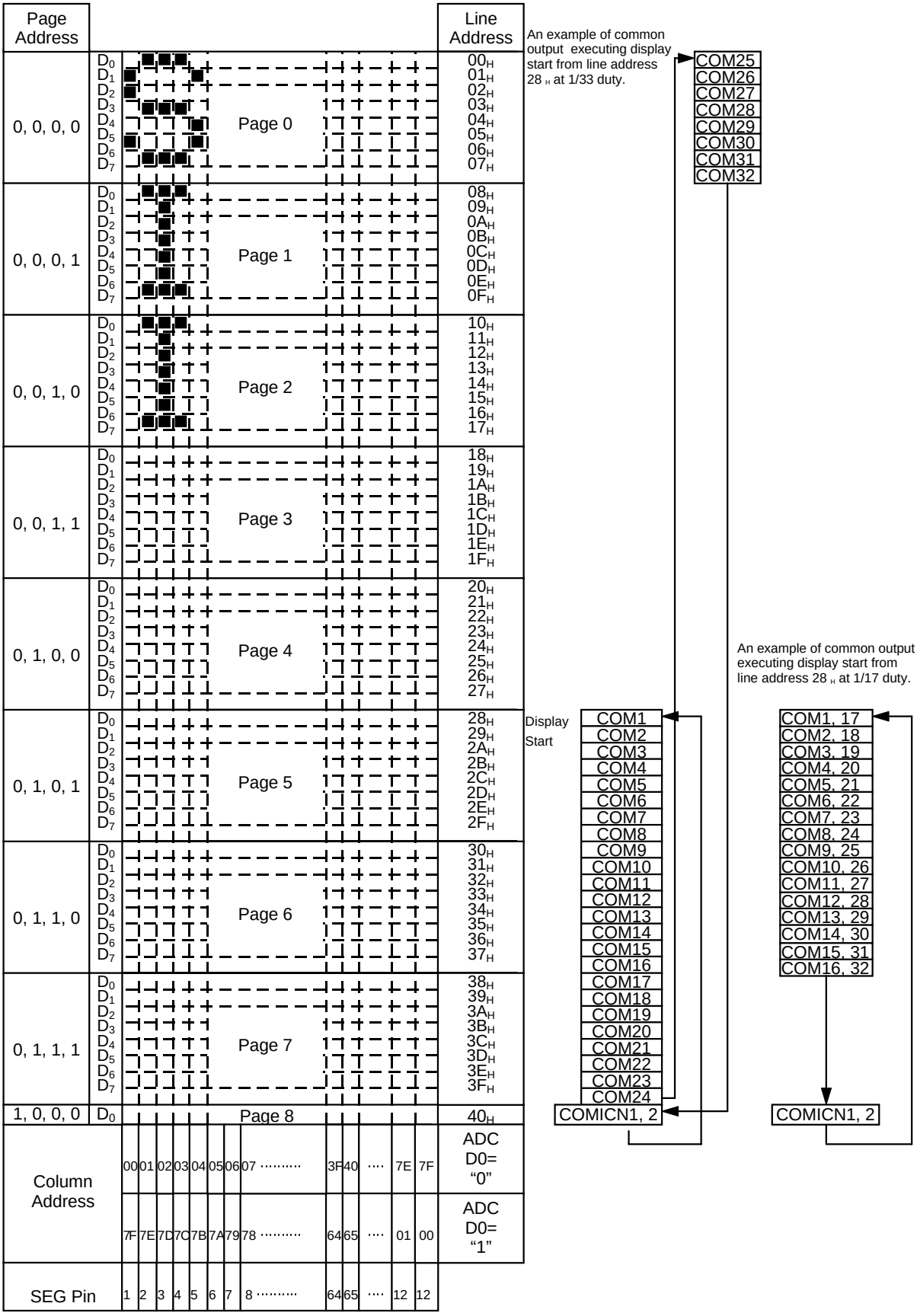


Figure 6 Display Data RAM vs Addresses

■ EXAMPLES OF LCD DRIVE OUTPUT WAVEFORM

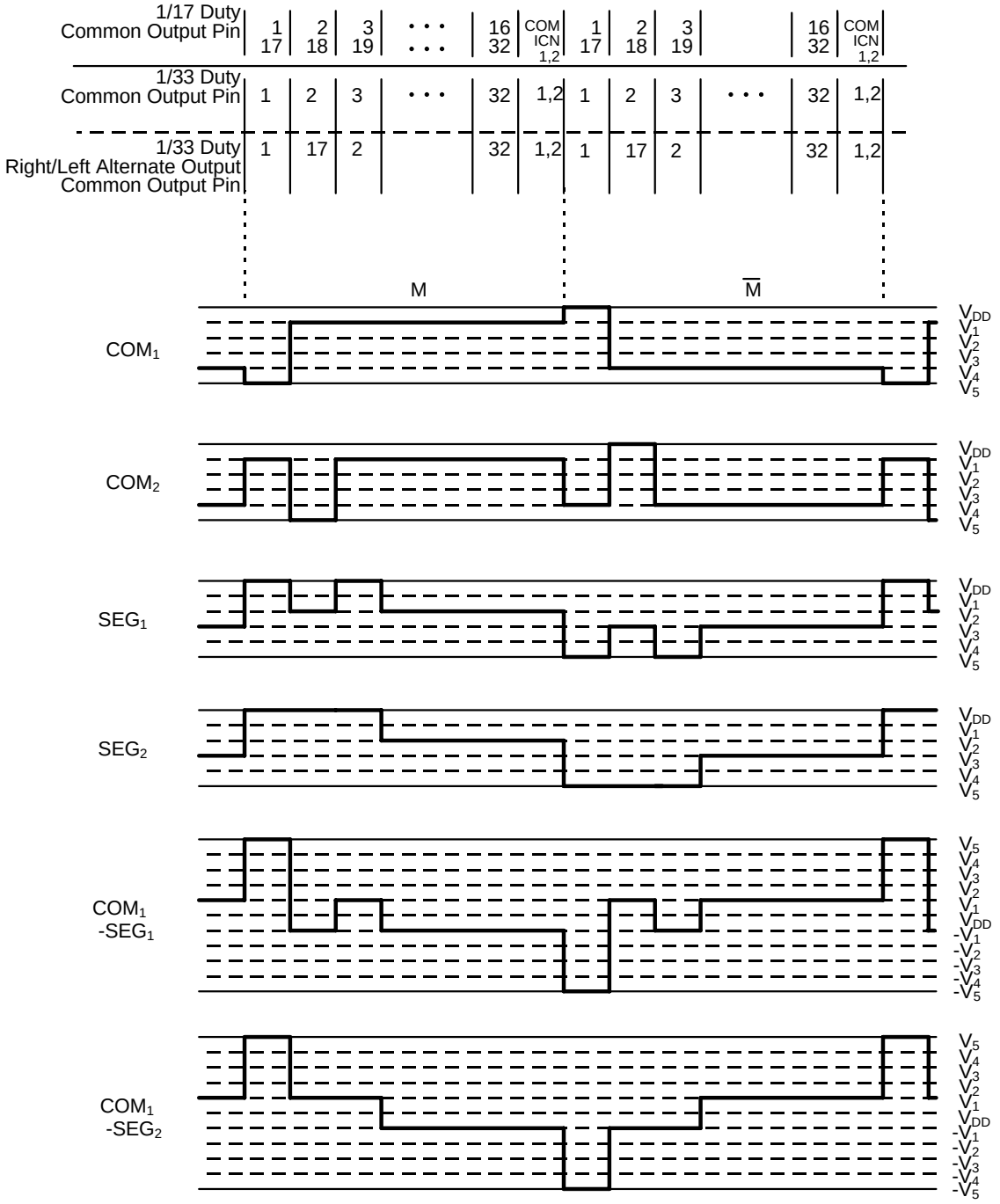
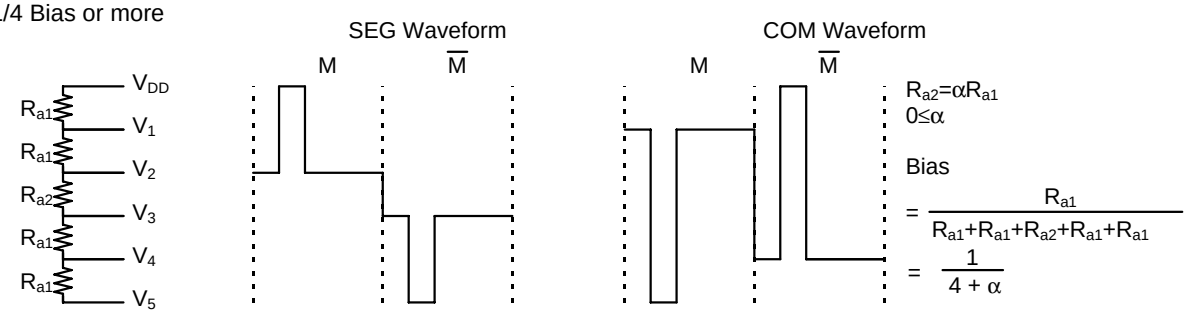


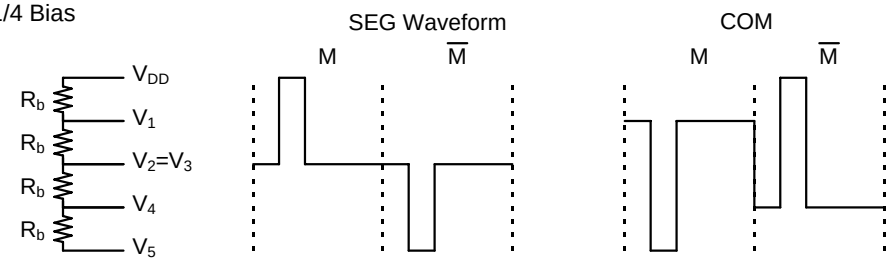
Figure 7 Examples of LCD Drive Output Waveform 1/5 Bias

■ EXAMPLES OF EXTERNAL BIAS RESISTOR CONNECTION VS LCD DRIVE WAVEFORM

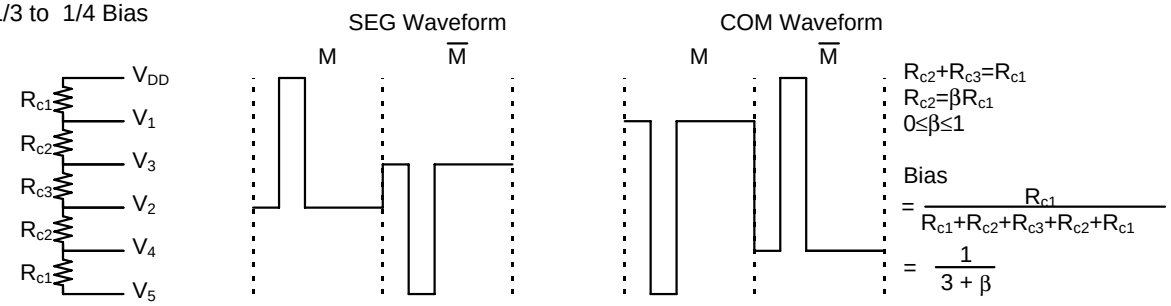
1. 1/4 Bias or more



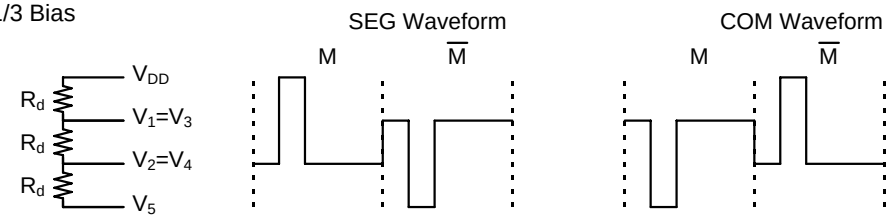
2. 1/4 Bias



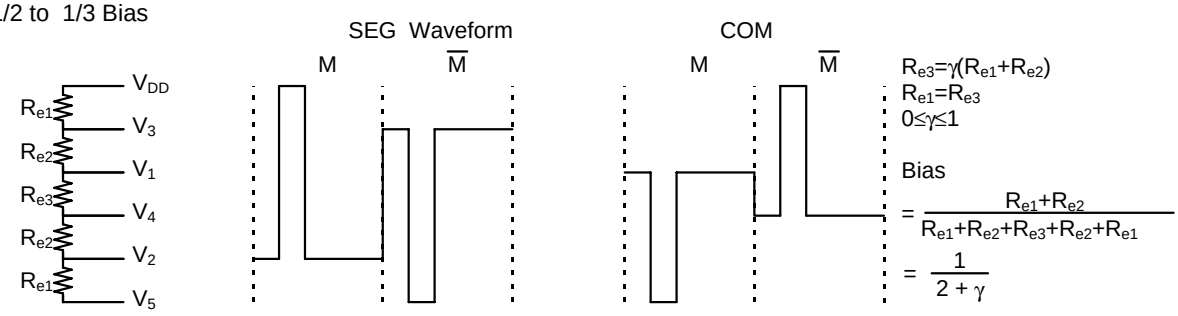
3. 1/3 to 1/4 Bias



4. 1/3 Bias



5. 1/2 to 1/3 Bias



6. 1/2 Bias

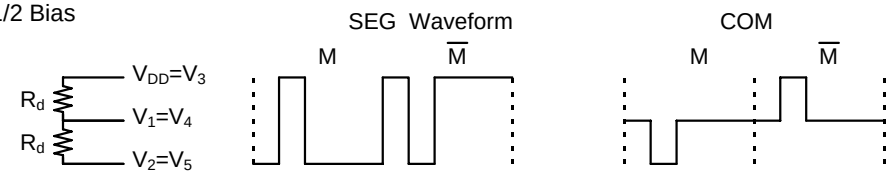


Figure 8 Examples of External Bias Resistors vs LCD Drive Waveform

■ COMMAND EXPLANATION

1. Display ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	1	1	0 1

D0:0: Regardless of the contents of the display data RAM, the LCD screen is compelled to be all-off (including the icon display).

D0:1 : The LCD screen is compelled to be normally displayed in accordance with the contents of the display data RAM.

The state is changed to the "Power Save" after turning on the Display All-Lit ON with the display OFF.

2. Display Start Line

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	Display Start Line Address					
					A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
·	·	·	·	·	·	·
·	·	·	·	·	·	·
·	·	·	·	·	·	·
1	1	1	1	1	1	$3F_H$

The line address of the display data RAM indicating the display start line is set. The display start line corresponds to COM1. The display area read from the display data RAM corresponds to the number of the lines set by the Duty select command. The line address is automatically incremented in synchronization with the common output. Changing the display start line using this command allows for page change on the display screen as well as vertical smooth scroll.

3. Page Address Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	1	Page Address			
							A3	A2	A1	A0

A3	A2	A1	A0	Page
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
·	·	·	·	·
·	·	·	·	·
0	1	1	1	7
1	0	0	0	8

The page address is set when accessing the display data RAM from the MPU. It is possible to access the display data RAM from the MPU with the page address and the column address commands. Even if the page address is changed, there is no change in the display screen during operation. Page 8 is assigned to the icon display. D0 only is valid.

4. Column Address Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	0	Column Address: Upper 3 bits		
								A6	A5	A4
0	1	0	0	0	0	0	Column Address: Lower 4 bits			
							A3	A2	A1	A0

Upper 3			Lower 4				
A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0_H
0	0	0	0	0	0	1	1_H
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	0	$7E_H$
1	1	1	1	1	1	1	$7F_H$

The column address is set when accessing the display data RAM from the MPU. When accessing the display data RAM from the MPU, the column address is incremented. When accessing the successive column address from the MPU, it is possible to access the display data without setting the column address each time. The automatic increment stops at 7FH after accessing the top column address 7FH. The page address is not incremented.

While the Read Modify Write command is being executed, a set of Column Address Setting commands is neglected.

5. Status Read

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	Status							

D7 : BUSY =0 : Can accept a command.
=1 : Internal operation or reset state. Does not accept a command.

D6 : ADC =0 : ADC Reverse
=1 : ADC Normal
Make sure that this polarity is contrary to that of the ADC Select command.

D5 : ON/OFF =0 : Display ON
=1 : Display OFF
Make sure that this polarity is contrary to that of Display ON/OFF command.

D4 : RESET =0 : Normal display operation state
=1 : Internal reset operation state with reset command.

D3 : PS =0 : Normal display operation state
=1 : Power Save state

D2 : MD =0 : Normal display operation state
=1 : Icon only display state

D1 : INVD =0 : Display Normal
=1 : Display Reverse

D0 : FDM =0 : Normal display
=1 : Display All-Lit ON

During power-save, display ON/OFF, PS and FDM are individually output.
When selecting a parallel interface, the status read can also be executed during reset operation.
When a serial interface is selected, the status read is invalid during reset operation. However, “H” is output from the SDO pin during reset operation.

6. Write Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data in the display data RAM							

The 8-bit display data is written in the display data RAM. After writing the display data, the column address is automatically incremented. To write the display data in succession after setting the 1st column address to be written by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. The icon display data is valid for only D0.

7. Read Data

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data from the display data RAM							

The 8-bit display data is read from the display data RAM. After the display data is read, the column address is automatically incremented. To read the display data in succession after setting the 1st column address to be read by the COLUMN ADDRESS SETTING command, the column address is not needed to be set each time. When reading the display data immediately after setting the COLUMN ADDRESS SETTING, dummy read is needed once.

8. ADC Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	0	0	0 1

D0 : 0 Normal Clockwise output. Column addresses 00H to 7FH correspond to segment outputs 1 to 128.

D0 : 1 Reverse Counterclockwise output. Column addresses 00H to 7FH correspond to segment outputs 128 to 1.

Normal or reverse can be selected for the correlation between the column address of the display data RAM and the segment output terminal. The ADC Select command selects normal or reverse in accordance with the relationship between the column address of the display data RAM and the segment output. This minimizes restrictions in the segment output wiring and IC assignment.

9. Display Normal/Reverse

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	1	0 1

D0 : 0 Normal Display data “1” makes the display be lit

D0 : 1 Reverse Display data “0” makes the display be lit

Lit or non-lit on each dot of the LCD panel can be reversed without rewriting the contents of the display data RAM.

The icon display is not reversed.

10. Display All-Lit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	0	1	0	0 1

The Display All-Lit ON command makes it possible to light the entire display regardless of the contents of the display data RAM. The display RAM data, however, does not change.
Through display all-lit OFF, the LCD screen returns to normal display operation and precedes the Display Normal/Reverse command.
When inputting the Display OFF command in the display all-lit ON state, it is changed to Power Save mode.

D0 : 0 Display All-Lit OFF Normal display

D0 : 1 Display All-Lit ON Forces the LCD panel to be entirely lit.

11. Duty Select, Alternate Common Output

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	0	1	0	0 1	0 1

D0 : 0 1 / 17 Duty

D0 : 1 1 / 33Duty

D1 : 0 The common is output to the common pin in a numerical order.

D1 : 1 The common is alternately output to right and left of the chip.

11.1 1/17 Duty Common Output Order

Output Order	Output in accordance with Common Pin Nos. Output pin Nos.
1	COM1, 17
2	COM2, 18
3	COM3, 19
'	'
'	'
15	COM15, 31
16	COM16, 32
17	COMICN1, 2

At 1/17 duty, the common is output according only to the pad No. Right and left alternate output are not set. Commons at right and left of the chip are simultaneously output.

11.2 1/33 Duty Common Output Order

Output Order	Output in accordance with Common Pin Nos. Output pin Nos.	Right and Left Common Alternate Output Output pin Nos.
1	COM1	COM1
2	COM2	COM17
3	COM3	COM2
'	'	'
'	'	'
16	COM16	COM9
17	COM17	COM25
'	'	'
'	'	'
31	COM31	COM16
32	COM32	COM32
33	COMICN1, 2	COMICN1, 2

12. Read Modify Write

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

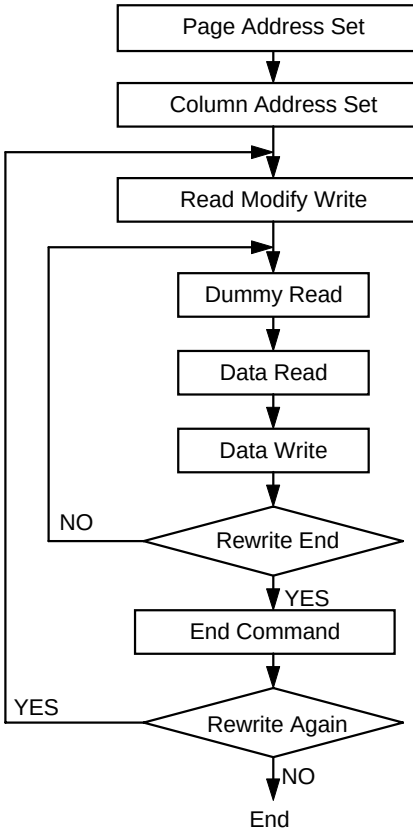
The Read Modify Write command is valid when partly altering or rewriting the display data RAM, for example the cursor indication, the blinking indication, etc. After inputting the Read Modify Write command, column address of the display data RAM is incremented only when inputting the display data write command. In Read data command, it is possible to rewrite the display data of the column address which is read, without increment of the column address. Furthermore, when reading and writing of the display data is successively executed, the successive address of the display data RAM is rewritten within the same page. A dummy read is needed when reading the display data.
The Read Modify Write command is valid until the End command is input. When inputting the End command, the column address returns to the address before the Read modify command was input.
During the Read Modify Write command operation, all commands are usable except the Column address set command.

13. End

This command cancels Read Modify Write. The column address of the display data RAM returns to the address before Read Modify Write is executed.

Note: When executing the End command during normal operation, the state returns to the column address before the Column Address command is executed.

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0



Returns to the address before executing the Read Modify Write command.

Figure 9 Command Sequence for Cursor Display

14. Reset Command

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

This command resets the register and counter of the display data RAM as follows. This does not affect the contents of the display data RAM.
After resetting, display starts according to the reset value.

- Resets the display start line register to the 1st line.
- Resets the column address counter to address 0 (00_H).
- Resets the page address counter to page 0.
- Clears the serial interface counter.
- Turns OFF the Read Modify Write.

15. Bias Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	1	0	Bias Select	

D1	D0	Bias Select
0	0	1/6.75 Bias
0	1	1/5 Bias
1	0	1/4 Bias
1	1	don't care

Equation

	1/4 Bias	1/5 Bias	1/6.75 Bias
V1	1/4×V5	1/5×V5	1/6.75×V5
V2	2/4×V5	2/5×V5	2/6.75×V5
V3	2/4×V5	3/5×V5	4.75/6.75×V5
V4	3/4×V5	4/5×V5	5.75/6.75×V5

Selects a built-in LCD bias resistor.
When the LCD power supply circuit ON/OFF command is ON, LCD drive waveform of the selected value of the bias is output.

When the LCD power supply circuit ON/OFF command is OFF, a built-in LCD bias resistor is disconnected and the command is invalid.

16. LCD Voltage Command Fine Adjustment Data Set

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	0	Fine Adjustment Data			

D3	D2	D1	D0	V5
0	0	0	0	Minimum
		⋮		
1	1	1	1	Maximum

Minutely adjusts voltage adjustment circuit output V5 with the corresponding command.

When this fine adjustment circuit is in no use, set the fine adjustment data to (0, 0, 0, 0).

17. LCD Power Supply Circuit ON/OFF

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	1	0	0	1	0	0 1

D0 : 0 LCD Power Supply Circuit OFF

D0 : 1 LCD Power Supply Circuit ON

Selects ON or OFF of a built-in LCD power supply circuit. When the LCD power supply circuit is ON, each function of the booster, LCD voltage adjustment circuit (voltage regulator, LCD voltage fine adjustment circuit), bias resistor, and voltage follower becomes valid by setting pins FNC1 and FNC2.

The LCD power supply circuit connected to pins FNC1 and FNC2 starts its operation earlier than the LCD Power Supply Circuit ON/OFF command.

18. Normal Display/ Icon Only Display

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	0	0	0 1	Boosting Control Data	

D2 : 0 Normal Display

D2 : 1 Icon Only Display

D1	D0	Boosting Frequency
0	0	f_{OSC} / 2
0	1	f_{OSC} / 4
1	0	f_{OSC} / 8
1	1	f_{OSC} / 16

Regardless of the content of the display RAM, displays icon only and the LCD panel compelled to be off.

Four kinds of boosting frequency can be set using boosting control data.
When reducing the boosting frequency, the gray scale of the icon display differs depending upon the panel size or the value of the boosting capacitor. Determine the boosting frequency by optimizing the contrast of the LCD panel experimentally. Also, take into consideration affect of noises due to boosting frequency to the system.
When executing the Icon Only Display command during Display Reverse, the icon only is displayed and other displays go off.

19. Power Save

When setting display all-OFF with the display OFF command and executing the display all-lit ON command, it changes to the Power save mode. When displaying in all-lit state and executing the Display OFF command, it is also changed to Power save mode. In Power save mode, CR oscillation stops and current consumption is reduced and has a value near that at standstill.

- The oscillating circuit and LCD power supply circuit are stopped.
- The LCD drive circuit is stopped. The Segment and Common outputs are fixed at VDD level.
- The LC display goes out.
- The contents of the display data RAM, the command and the address before the power save mode do not change.

The Power save state is canceled through the Display ON or the Display all-lit command. To change the state from the power save to the normal display, input both the Display ON and Display All-Lit OFF commands.
When using an external power supply circuit, stop the the external power supply circuit and float the LCD power supply. When using an external bias resistor in order to reduce the electric current, attach a switching transistor which cuts this current flowing through the bias resistor.

Combination of Commands		State
Display ON	Display All-Lit OFF	Normal display operation
Display ON	Display All-Lit ON	All-lit display
Display OFF	Display All-Lit OFF	All-OFF
Display OFF	Display All-Lit ON	Power save

20. Reference Voltage Temperature Compensation Coefficient Select

A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	1	*	Selection Data

* : don't care

D0	Temperature Compensation Coefficient ΔVREF(% / °C)	Reference Voltage (TYP) VREF(V) (VDD=OV)
0	-0.13	-1.6
1	+0.01	-2.2

For temperature characteristics, refer to the attached data.

$$\Delta V_{REF} = \frac{|V_{REF}(T_2)| - |V_{REF}(T_1)|}{T_2 - T_1}$$

$$T_2 > T_1$$

■ COMMANDS

Table 13 Commands

Command	Code											Description
	A0	RDX	R/WX	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	D0:0 Display OFF: Display goes out D0:1 Display ON: Normal Display
Display Start Line	0	1	0	0	1	Display start line address						Sets the line address of the display data RAM output to COM1.
Page Address Set	0	1	0	1	0	1	1	Page Address				Sets the page address of the display data RAM.
Upper 3 bits of Column Address Set	0	1	0	0	0	0	1	0	Upper 3 bits of Column Address			Sets upper 3 bits of the display data RAM Column Address
Lower 4 bits of the Column Address Set	0	1	0	0	0	0	0	Lower 4 bits of the Column Address				Lower 4 bits of display data RAM column address
Status Read	0	0	1	Status								Status Read
Display Data Write	1	1	0	Write Data in Display Data RAM								Writes data of D0 to D7 in the display data RAM.
Display Data Read	1	0	1	Read Data from Display Data RAM								Reads data from D0 to D7 from the display data RAM.
ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	Reverses upper or lower display data RAM column address D0:0 Normal D0:1 Reverse
Display Normal/Reverse	0	1	0	1	0	1	0	0	1	1	0 1	D0:0 Display Normal D0:1 Display Reverse
Display All-Lit ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	D0:0 Normal Display D0:1 Display All-Lit
Duty Selection/ Alternate Common Output	0	1	0	1	0	1	0	1	0	* 0 1	0 1 1	D0:0 1/17 Duty D0:1 1/33 Duty D1:0 Common output order: CW D1:1 Common output order:Alternate
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments display data RAM column address only during writing
End	0	1	0	1	1	1	0	1	1	1	0	Read Modify Write Release
Reset	0	1	0	1	1	1	0	0	0	1	0	Initializes display data RAM address, etc.
Bias Selection	0	1	0	0	0	1	0	1	0	D1	D0	D1,D0:0, 0 1/6.75 Bias Selection D1,D0:0, 1 1/5 Bias Selection D1,D0:1, 0 1/4 Bias Selection D1,D0:1, 1 Don't care
LCD Voltage Command Fine Adjustment Data	0	1	0	1	0	0	0	Fine Adjustment Data				Sets the LCD drive voltage adjustment circuit.
LCD Power Supply Circuit ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	D0:0 LCD power supply circuit OFF D0:1 LCD power supply circuit ON
Icon Only Display	0	1	0	1	1	0	0	0	D2	Boosting Control Data		D2:0 Normal Display D2:1 Icon Only Display Boosting control data: Selects boosting frequency
Reference Voltage Temperature Coefficient Selection	0	1	0	1	1	1	0	0	1	*	0 1	D0:0 –0.13%/°C D0:1 +0.01%/°C
Power save												Display OFF, Display all-lit ON

■ ABSOLUTE MAXIMUM RATINGS

Table 14 Absolute Maximum Ratings

V_{DD}=0.0 V

Parameter		Symbol	Ratings	Unit
Supply voltage		V_{SS}	-6.0 to +0.4	V
LCD drive voltage 1		V_5	-13.5 to +0.4	V
LCD drive voltage 2		V_1, V_2, V_3, V_4	V_5 to +0.4	V
Input voltage		V_{IN}	V_{SS}-0.4 to +0.4	V
Output voltage		V_{OUT}	V_{SS}-0.4 to +0.4	V
Operating temperature range		T_{opr}	-30 to +85	°C
Storage temperature range	Chip	T_{stg}	-55 to +125	°C
	TAB		-55 to +100	

Note 1 Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Note 2 Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 3 When connecting a bias resistor externally, set the LCD power supply voltage so that the state is changed to VSS≥V5.

■ DC CHARACTERISTICS

1. Electrical Characteristics

Table 15 Electrical Characteristics

(Unless otherwise specified : V_{DD}=0 V, V_{SS}=-5.0±0.5 V, Ta=-30 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}		-5.5	—	-2.4	V	Note 1
LCD Drive Voltage	V_5	When using an external LCD power supply	-11.0	—	-2.7	V	Note 2
	V_1, V_2		V_5	—	V_{DD}	V	
	V_3, V_4						
High-level Input voltage	V_{IH}	V_{SS}=-2.4 to -4.5V	0.2×V_{SS}	—	V_{DD}	V	Note 3
		V_{SS}=-5.0±0.5V	0.3×V_{SS}	—	V_{DD}		
Low-level Input voltage	V_{IL}	V_{SS}=-2.4 to -4.5V	V_{SS}	—	0.8×V_{SS}	V	Note 3
		V_{SS}=-5.0±0.5V	V_{SS}	—	0.7×V_{SS}		
High-level Output Voltage	V_{OH1}	I_{OH}=-0.5mA, V_{SS}=-2.4 to -4.5V	0.2×V_{SS}	—	—	V	Note 4
		I_{OH}=-1.0 mA	0.2×V_{SS}	—	—		
	V_{OH2}	I_{OH}=-50μA, V_{SS}=-2.4 to -4.5V	0.2×V_{SS}	—	—	V	OSC_2 5
		I_{OH}=-120 μA	0.2×V_{SS}	—	—		
Low-level Output Voltage	V_{OLI}	I_{OL}=0.5mA, VSS=-2.4 to -4.5V	—	—	0.8×V_{SS}	V	Note 4
		I_{OL}=1.0mA	—	—	0.8×V_{SS}		
	V_{OL2}	I_{OL}=50μA VSS=-2.4 to -4.5V	—	—	0.8×V_{SS}	V	OSC_2
		I_{OL}=120μA	—	—	0.8×V_{SS}		
Input Leakage Current	I_{ILEAK}	V_{SS}=-2.4 to -5.5V	-1.0	—	1.0	μA	Note 5
Output Leakage Current	I_{OLEAK}	V_{SS}=-2.4 to -5.5V	-3.0	—	3.0	μA	Note 6
LCD Driver ON Resistor	R_{ON}	Ta=25°C, V5=-8.0V 1/5 Bias	—	3.0	5.0	kΩ	Note 7
Standby Current	I_S		—	0.05	5.0	μA	Note 8
Operating Current	I_{SS1}	External LCD power supply is used: During LC display V5=-8.0 V Rf=1 MΩ	—	20.0	30.0	μA	Note 9
	I_{SS2}	During access: tcyc=200 kHz V_{SS}=-3.0±0.3 V	—	150	450	μA	Note 10
		During access: tcyc=200 kHz	—	300			
Oscillating Frequency	f_{OSC}	R_f=1.0 MΩ V_{SS}=-3.0 V	11	16	21	kHz	Note 11
		R_f=1.0 MΩ V_{SS}=-5.0 V	15	18	22		
Wait Time	t_R		10	—	—	μs	Note 12

2. LCD Power Supply Circuit Electrical Characteristics

Table 16 LCD Power Supply Circuit Electrical Characteristics

(Unless otherwise specified VDD=0 V, VSS=-2.4 to -5.5, Ta=-30 to 85°C)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Note
Operating Voltage	V_{SS}			-5.5	—	-2.4	V	Note 13
Boosting Output Voltage	V_{OUT}	Triple boosting: Up to V_{SS}=-3.6V Double boosting: Up to V_{SS}=-5.5V		-11.0	—		V	
LCD Supply Circuit Operating Voltage	V_5	1/4 Bias		-11.0	—	-4.0	V	Note 14
		1/5 Bias		-11.0	—	-4.5		
		1/6.7 Bias		-11.0	—	-5.5		
LCD Driver Operating Voltage	V_{LCD}			-11.0	—	-2.7	V	Note 15
Built-in LCD Circuit Current Consumption	I_{SSL}	V_{OUT}=-10.0 V Double Boosting V_{SS}=-5.0 V V5=-8.0 V 1/5 Bias Osc. Frequency: 18 kHz		-200	-90	—	µA	Note 16
External LCD Power Supply Used: LCD Driver Current Consumption	I_{V5}	V5=-8.0V 1/5 Bias		-75	-30	—	µA	Note 17
Reference Voltage	V_{REF}	Ta=25°C	ΔVREF=+0.01%/°C	-2.4	-2.2	-2.0	V	Note 18
			ΔVREF=-0.13%/°C	-1.7	-1.5	-1.3		
Reference Current	I_{REF}	Fine adjustment data (1111) Ta=25°C		1.5	2.5	4.0	µA	Note 19
LCD drive bias voltage (1/4 bias)	V_1	V5=-4.0V to -11.0V		1/4·V5-0.1	1/4·V5	1/4·V5+0.1	V	Note 20
	V_2			2/4·V5-0.1	2/4·V5	2/4·V5+0.1		
	V_3			2/4·V5-0.1	2/4·V5	2/4·V5+0.1		
	V_4			3/4·V5-0.1	3/4·V5	3/4·V5+0.1		
LCD drive bias voltage (1/5 bias)	V_1	V5=-4.5V to -11.0V		1/5·V5-0.1	1/5·V5	1/5·V5+0.1		
	V_2			2/5·V5-0.1	2/5·V5	2/5·V5+0.1		
	V_3			3/5·V5-0.1	3/5·V5	3/5·V5+0.1		
	V_4			4/5·V5-0.1	4/5·V5	4/5·V5+0.1		
LCD drive bias voltage (1/6.75 bias)	V_1	V5=-5.5V to -11.0V		1/6.75·V5-0.1	1/6.75·V5	1/6.75·V5+0.1		
	V_2			2/6.75·V5-0.1	2/6.75·V5	2/6.75·V5+0.1		
	V_3			4.75/6.75·V5-0.1	4.75/6.75·V5	4.75/6.75.V5+0.1		
	V_4			5.75/6.75·V5-0.1	5.75/6.75·V5	5.75/6.75·V5+0.1		

3. References

Table 17 References

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Note
Input Pin Capacity	C_{IN}	Ta=25°C	—	5	8	pF	Note 3

Note 1 Sharp variation in the supply voltage or input signal voltage due to strange noises may lead to a malfunction of the IC. Supply stable supply voltage and input signal voltage.
If you change the level of the supply voltage intentionally, a malfunction may occur. NEVER CHANGE the level of the supply voltage.

Note 2 When the external bias voltage is input, $V_{DD} \geq V1$, V2, V3, V4≥V5, VSS>V5. There is no limitation for determining the voltage level of V1, V2, V3, and V4.

Note 3 Pins A0, CSX, RDX, R/WX, C86, P/SX, OSC1, FNC1 and FNC2.
Pins D0 to D7 during display data write and command input.
Fully swing the levels V_{IH} and V_{IL} of the input signal within the range of power supply voltage so that the state is $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$. When the level of V_{IH} and V_{IL} is the middle level of the supply voltage, the through current flowing through the input pin and the current consumption may be increased.

Note 4 Pin s D0 to D7 during read.

Note 5 Pins A0, CSX, RDX, R/WX,C 86, P/SX, OSC1, FNC1 and FNC2.

Note 6 Pins D0 to D7 during write and high-impedance.

Note 7 ON resistance between LCD drive output pins (SEG1 to SEG128, COM1 to 32, COMICN1, and 2) and LCD drive bias voltage pins (V1, V2, V3, V4). Using the external LCD power supply, measure the resistance at a 0.1-V difference from the LCD drive output pin after applying 1/2 voltage of V5 to the LCD drive bias voltage pin.

Note 8 Power save state. When turning the input pin to "Floating," the through current flows and will eventually the power save effect may be reduced.

Note 9 Shows the current consumption during display including CR oscillation.
It does not include the current consumed by the booster, LCD supply voltage adjustment circuit, voltage regulator, LCD bias resistor when using the external LCD power supply. The LCD drive output pin is no load. The current consumed by the LCD panel and wiring capacitor is not included. Measure it without access from the MPU. The current consumed by the external LCD power supply and external bias resistor and other is not included.

Note 10 The current consumption while the checkered pattern display data are being written from the MPU. The CR oscillation is measured while the CR oscillating circuit stops. The voltage level of the input signal is the $V_{IH}=V_{DD}$ and $V_{IL}=V_{SS}$. When the input signal voltage is in the middle level, the current consumption may be increased. When the display data is written from the MPU during display, the state is changed to $I_{SS1}+I_{SS2}$.

Note 11 Shows the standard value at oscillating resistor 1 MΩ. Determine appropriate oscillating frequency so as not to be in synchronization with the frame frequency and other frequency such as the fluorescent lamps.

Note 12 Shows the wait time from when the power voltage rises to 80% of the specified voltage to when the command input becomes available.

Note 13 The operating voltage range of the booster.

Note 14 Shows the operating voltage range of the LC voltage adjustment circuit, voltage follower, and LCD bias resistor. The operating voltage range differs depending upon each bias setting value. To adjust V5 with the LCD voltage adjustment circuit, it is necessary to set the voltage within the bias voltage.
$|V_{OUT}| - |V5| \geq 0.2V$

Note 15 The operating voltage range of the LCD driver after the voltage follower functions. Also, it shows the voltage range of V1 to V5 supplied from the external LCD power supply circuit.

Note 16 Shows the value of the current consumed by the booster, LCD voltage adjustment circuit, voltage follower, LCD bias resistor, and LCD driver. It does not include the value IRREG=V5/(R1+R2+R3) of the current flowing through external resistors R1, R2, and R3. Set the command fine adjustment data to 1000. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is $I_{SSL}+I_{SS1}$.

Note 17 The built-in LCD power supply circuit stops when FNC1 and 2 are "H." Current consumption only for the LCD driver. Outputs the checkered patterns from the LCD drive output pin. The pin is measured at "Open." Current consumption of the IC during display is $IV5+I_{SS1}$.
When using the external power supply, stop the built-in power supply circuit which does not need to be operated with pins FNC1 and 2 to prevent the IC from being broken due to a shorting of the internal power supply.

Note 18 The reference voltage differs depending upon the temperature coefficient selected with the corresponding command.

Note 19 Constant current which flows into the LCD Voltage Command Fine Adjustment Circuit of the IC, for the Fine adjustment data (1111).
Increasing the Fine adjustment data by 1 bit, V5 increases by $Rb \times I_{REF} / 15$.

Note 20 For the Chips deliveries, chips are delivered after they satisfy their LCD drive bias voltages are ±0.08V in the delivery testing at 25°C.

■ TIMING CHARACTERISTICS

1. Parallel Interface

1.1 80-Family MPU Read/Write Timing Characteristics

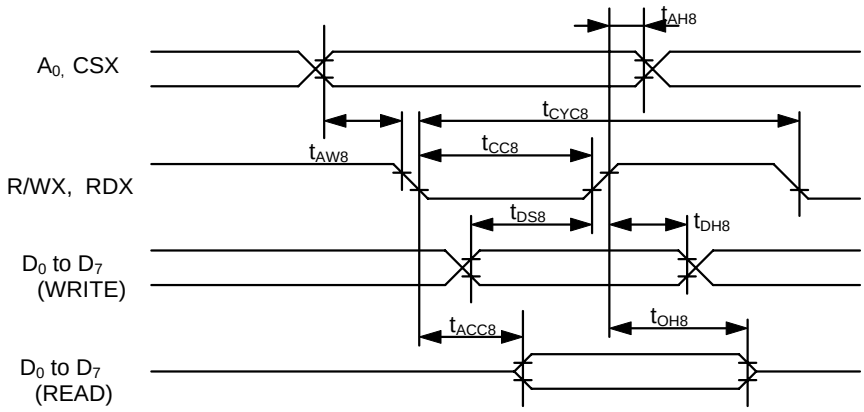


Figure 10 80-Family MPU Read/Write Timing Characteristics

Table 18 80-Family MPU Read/Write Timing Characteristics When VSS=-5V

(Ta=-30 to 85°C, V_{SS}=-5 V±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0 CSX	t_{AH8}	Address Hold Time		20	—	ns	
	t_{AW8}	Address Setup Time		20	—		
R/WX, RDX	t_{CYC8}	System Cycle Time		500	—		
	t_{CC8}	Control Pulse Width		100	—		
D_0 to D_7	t_{DS8}	Data Setup Time		80	—		
	t_{DH8}	Data Hold Time		20	—		
	t_{ACC8}	RDX Access Time	CL=15 pF		90		
	t_{OH8}	Output Disable Time	CL=15 pF	10	60		

Table 19 80-Family MPU Read/Write Timing Characteristics When VSS=-3V

(Ta=-30 to 85°C, V_{SS}=-3 V±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0 CSX	t_{AH8}	Address Hold Time		40	—	ns	
	t_{AW8}	Address Setup Time		40	—		
R/WX, RDX	t_{CYC8}	System Cycle Time		1000	—		
	t_{CC8}	Control Pulse Width		200	—		
D_0 to D_7	t_{DS8}	Data Setup Time		160	—		
	t_{DH8}	Data Hold Time		40	—		
	t_{ACC8}	RDX Access Time	CL=15 pF		180		
	t_{OH8}	Output Disable Time	CL=15 pF	10	120		

Note • Rise/fall time of the input signal is 15 nsec or less.
• Timing is specified at 20% or 80% of the signal waveform.

1.2 68-Family MPU Read/Timing Characteristics

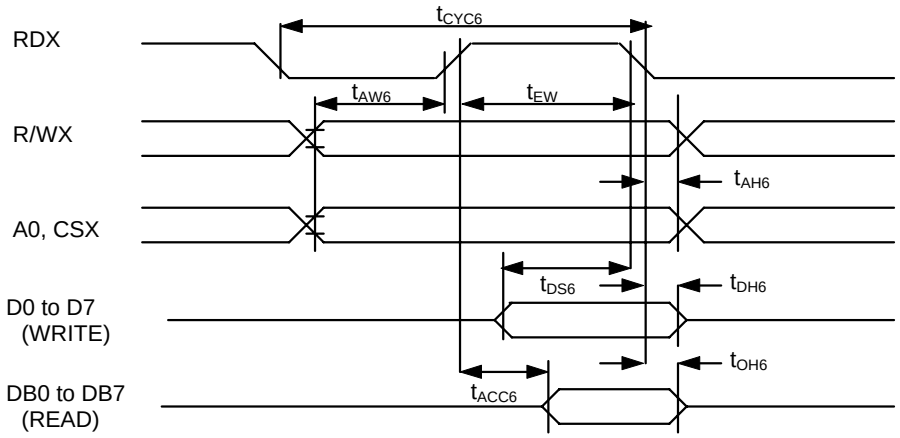


Figure 11 68-Family MPU Read/Write Timing

Table 20 68-Family MPU Read/Write Timing Characteristics When VSS=-5V

(Ta=-30 to 85°C, V_{SS}=-5 V±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0 CSX, R/WX	t_{CYC6}	System Cycle Time		500	—	ns	
	t_{AH6}	Address Hold Time		20	—		
	t_{AW6}	Address Setup Time		20	—		
D_0 to D_7	t_{DS6}	Data Setup Time		80	—		
	t_{DH6}	Data Hold Time		20	—		
	t_{ACC6}	Access Time	CL=15 pF		90		
	t_{OH6}	Output Disable Time	CL=15 pF	10	60		
E	t_{EW}	Enable Pulse Width	READ	100	—		
			WRITE	80	—		

Table 21 68-Family MPU Read/Write Timing Characteristics When VSS=-3V

(Ta=-30 to 85°C, V_{SS}=-3 V±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
A_0 CSX, R/WX	t_{CYC6}	System Cycle Time		1000	—	ns	
	t_{AH6}	Address Hold Time		40	—		
	t_{AW6}	Address Setup Time		40	—		
D_0 to D_7	t_{DS6}	Data Setup Time		160	—		
	t_{DH6}	Data Hold Time		40	—		
	t_{ACC6}	Access Time	CL=15 pF		180		
	t_{OH6}	Output Disable Time	CL=15 pF	10	120		
E	t_{EW}	Enable Pulse Width	READ	200	—		
			WRITE	160	—		

Notes • Rise/fall time of the input signal is 15 nsec or less.
• Timing is specified at 20% of 80% or the signal waveform.

2. Serial Interface

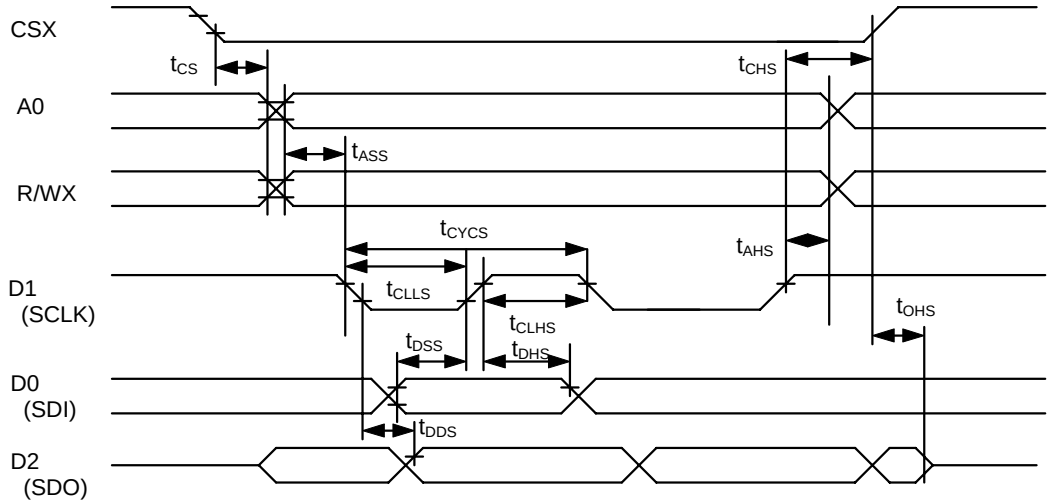


Figure 12 Serial Interface Read/Write Timing Characteristics

Table 22 Serial Interface Timing Characteristics When VSS=-5V

(Ta=-30 to 85°C, V_{SS}=-5 V±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
CSX	tCSS	Chip Select Setup Time		50		ns	
	tCHS	Chip Select Hold Time		400			
A0, R/WX	tASS	Address Setup Time		120			
	tAHS	Address Hold Time		200			
D0 (SDI)	tDSS	Data Setup Time		120			
	tDHS	Data Hold Time		50			
D1 (SCLK)	tCYCS	Clock Cycle Time		500			
	tCLLS	Clock L Time		200			
	tCLHS	Clock H Time		200			
D2 (SDO)	tDDS	Data Delay Time	CL=15 pF		90		
	tOHS	Data Disable Time	CL=15 pF	10	60		Note 1

Table 20 Serial Interface Timing Characteristics When VSS=-3V

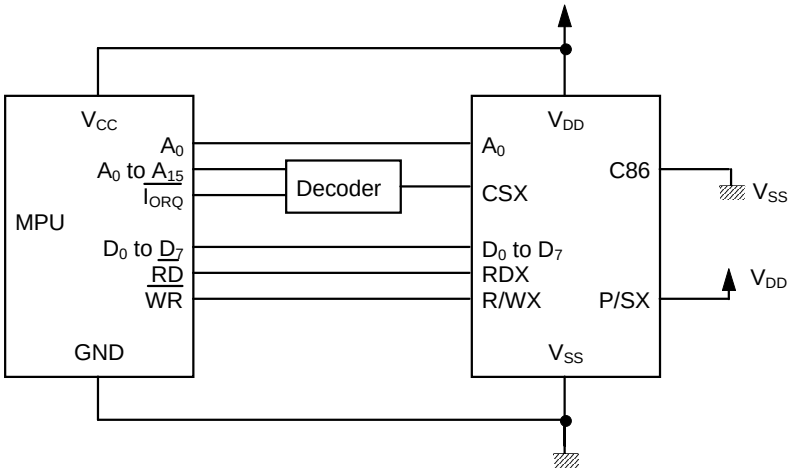
(Ta=-30 to 85°C, V_{SS}=-3v±10%)

Signal	Symb.	Designation	Conditions	Min.	Max.	Unit	Note
CSX	tCSS	Chip Select Setup Time		100		ns	
	tCHS	Chip Select Hold Time		800			
A0, R/WX	tASS	Address Setup Time		240			
	tAHS	Address Hold Time		400			
D0 (SDI)	tDSS	Data Setup Time		240			
	tDHS	Data Hold Time		100			
D1 (SCLK)	tCYCS	Clock Cycle Time		1000			
	tCLLS	Clock L Time		400			
	tCLHS	Clock H Time		400			
D2 (SDO)	tDDS	Data Delay Time	CL=15 pF		180		
	tOHS	Data Disable Time	CL=15 pF	10	120		Note 1

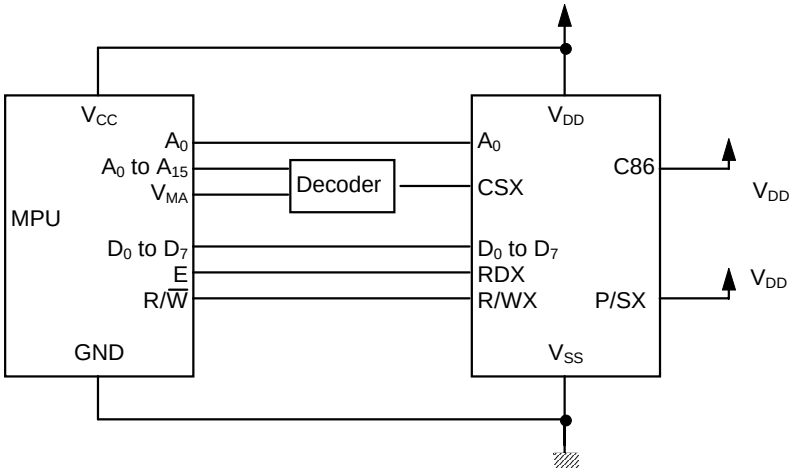
Note 1: D2(SDO) is high-impedance at the rising edge of the CSX.
Note 2: Rise/fall time of the input signal is 15 sec. or less.
Note 3: Timing is specified at 20% or 80% of the signal waveform.

■ EXAMPLES OF CONNECTION TO MPU

80-Family MPU



68-Family MPU



Serial Interface

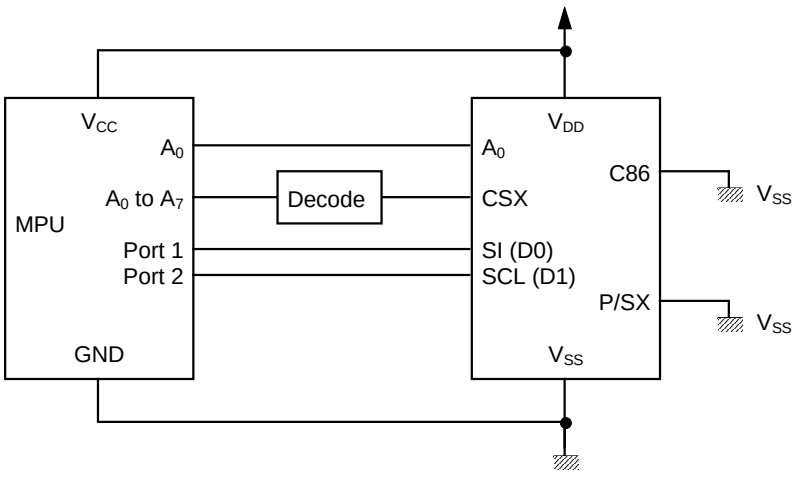
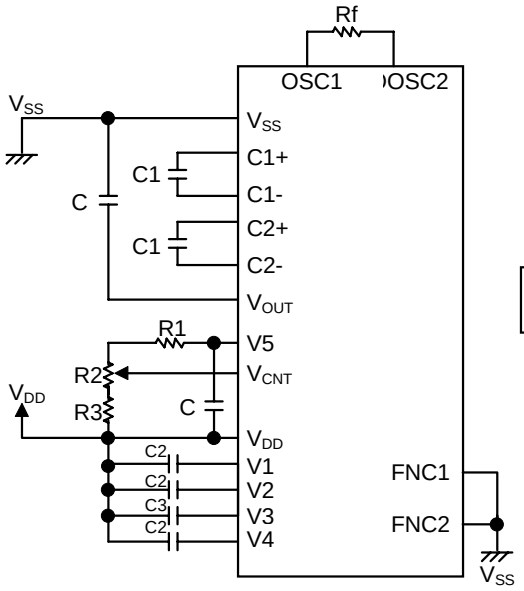


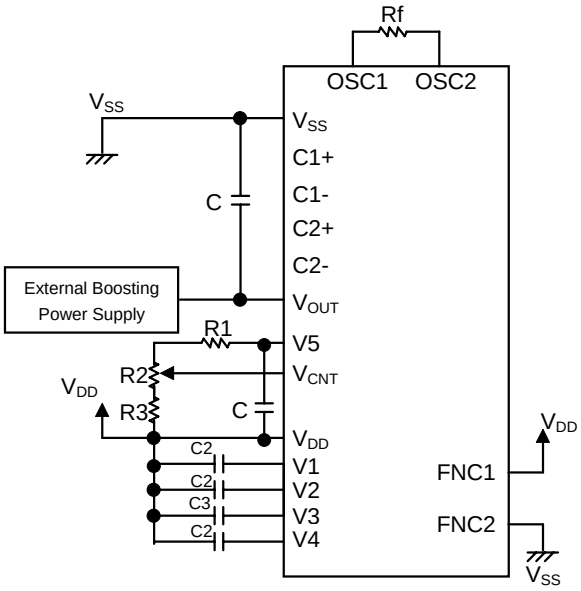
Figure 13

■ EXAMPLES OF APPLICATION CIRCUITS OF LCD POWER SUPPLY

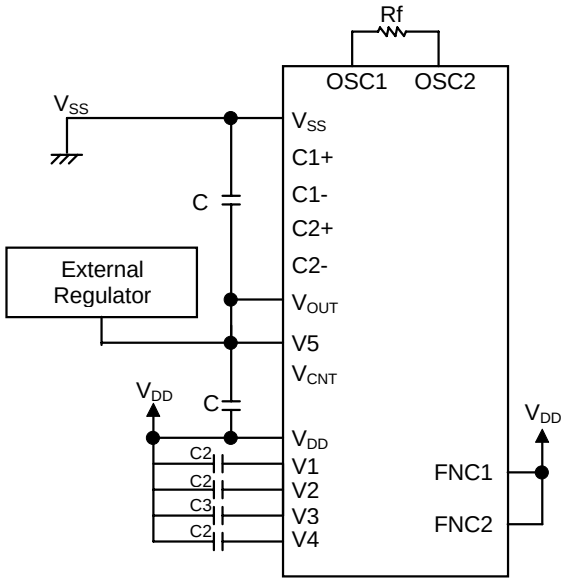
- When Using a Built-in LCD Power Supply Circuit (Triple Boosting)



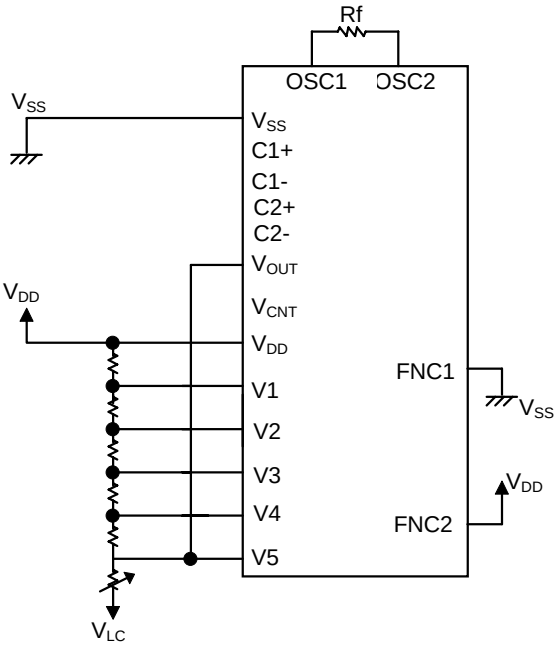
- When Using an External Boosting Power Supply



- When Using an External Regulator



- When Using an External LCD Power Supply



Reference
C : 1.0 µF
C1 : 0.47 µF
C2 : 0.1 µF
C3 : 0.01 µF Capacitor C3 connected to V3 pin is recommended 0.01µF.

Figure 14

- Booster Capacitor Connection

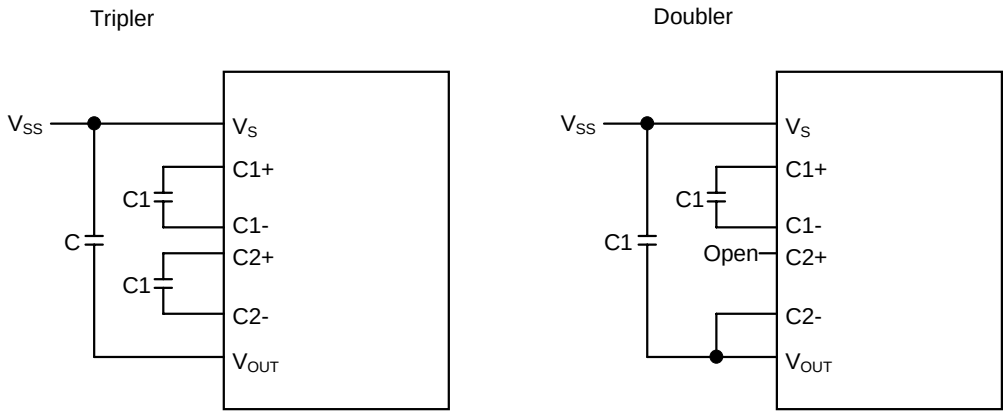


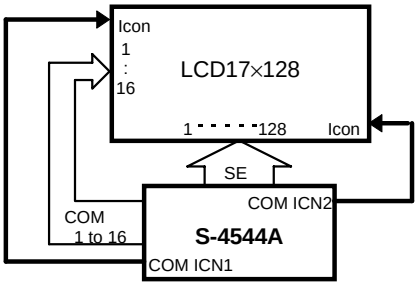
Figure 15

Reference
C : 1.0 µF
C1 : 0.47 µF

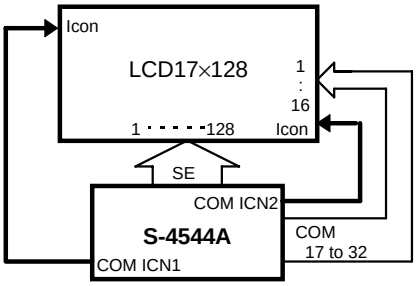
■ EXAMPLES OF CONNECTION TO LCD PANELS

1. 1/17 Duty 17×128 Panel

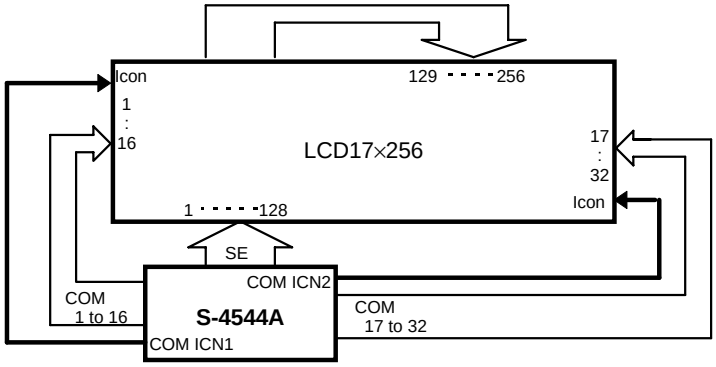
- COM1 to 16 are used:



- COM17 to 32 are used:

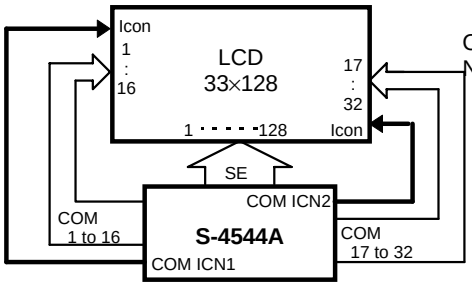


2. 1/33 Duty 17×256 Panel



3. 1/33 Duty 33×128 Panel

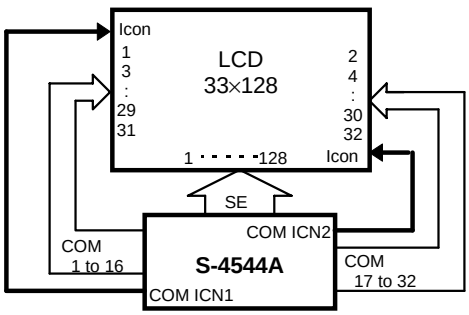
3.1 Normal Common Output



Output in a numerical order of common pin Nos.

3.2 Common Right/Left Alternate Output

Uneven-Numbered Common



Even-Numbered Common Line

Figure 16 Examples of Connection to LCD Panels