HAMAMATSU

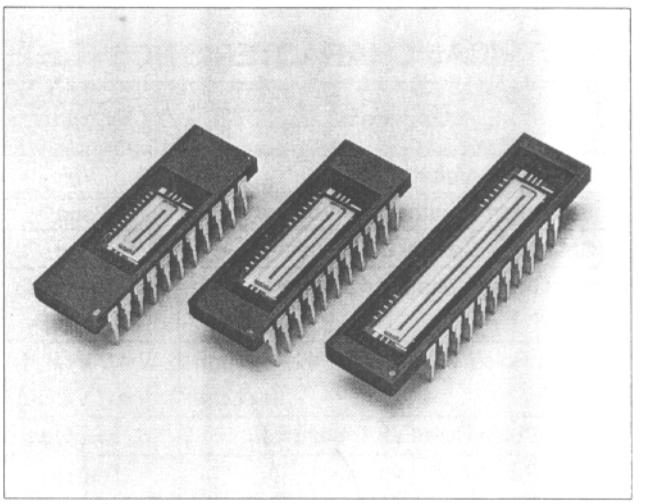
TECHNICAL DATA

CURRENT OUTPUT TYPE MOS LINEAR IMAGE SENSORS S3902, S3903 SERIES

High UV Sensitivity, 0.5mm Pixel Height, Excellent Photometric Capabilities, Low Power Consumption

FEATURES

- **Medium wide photosensitive area**
  Pixel pitch : 50μm (S3902), 25μm (S3903)
  Pixel height : 0.5mm
- **High UV sensitivity with good stability**
- **Excellent photometric capabilities**
  Low dark current and high saturation charge
  Good linearity
  Wide dynamic range
- **Low power consumption : less than 1mW**
- **Start pulse and clock pulses are CMOS logic compatible**



APPLICATIONS

- **Multichannel spectrophotometry**
- **Image readout systems**

DESCRIPTION

By applying NMOS technology to the manufacture of self-scanning linear photodiode arrays, Hamamatsu can offer higher performance and increased flexibility to photometric instrument manufacturers. The new design achieves high UV sensitivity without deterioration even with extended UV exposure. Application is simplified because of low power consumption and a single video output line. All members of the series are pin compatible.

The S3902 and S3903 series MOS linear image sensors feature good linearity over a wide dynamic range and have low power consumption. They have a photosensitive area with a pixel height of 0.5mm and a pixel pitch of 50μm (S3902) or 25μm (S3903). Each series is available with three different number of pixels; 128, 256 and 512 for the S3902 series, 256, 512 and 1024 for the S3903 series.

Figure 1: Equivalent Circuit

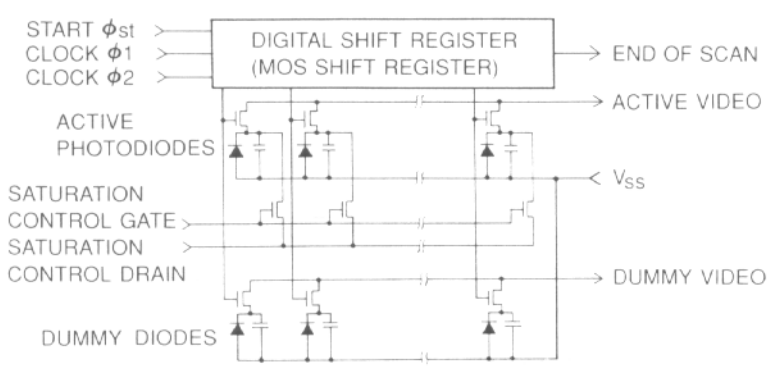
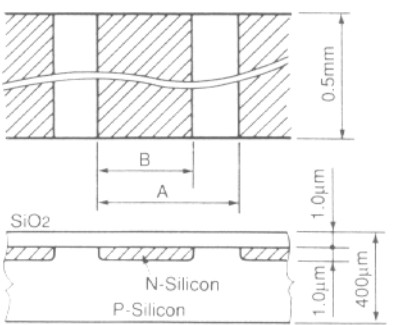


Figure 2: Sensor Geometry



S3902: A=50μm, B=45μm
S3903: A=25μm, B=20μm

MAXIMUM RATINGS

Parameters	Symbols	S3902, S3903 Series	Units
Supply Clock Amplitude	$V\phi$	15	V
Operating Temperature ①	Topr	–40 to +65	°C
Storage Temperature	Tstg	–40 to +85	°C

① No dew

ELECTRICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3902 Series			S3903 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Video Bias Voltage ①	V_b	1.5	$V\phi$–3.0	$V\phi$–2.5	1.5	$V\phi$–3.0	$V\phi$–2.5	V
Saturation Control Gate Voltage	V_{scg}	—	0	—	—	0	—	V
Saturation Control Drain Voltage	V_{scd}	—	V_b	—	—	V_b	—	V
Start Pulse Voltage (ϕst) ① -High	$V_{\phi S}$ (H)	4.5	$V\phi$	10	4.5	$V\phi$	10	V
-Low	$V_{\phi S}$ (L)	0	—	0.4	0	—	0.4	V
Clock Pulse Voltage (ϕ1, ϕ2) -High	Vϕ1, Vϕ2(H)	4.5	5	10	4.5	5	10	V
-Low	Vϕ1, Vϕ2(L)	0	—	0.4	0	—	0.4	V
Start Pulse Rise/Fall Times (ϕst)	$t_{r\phi S}$, $t_{f\phi S}$	—	—	500	—	—	500	ns
Start Pulsewidth (ϕst)	$t_{pw\phi S}$	200	—	—	200	—	—	ns
Clock Pulse Rise/Fall Times (ϕ1, ϕ2)	$t_{r\phi 1}$, $t_{r\phi 2}$, $t_{f\phi 1}$, $t_{f\phi 2}$	—	—	500	—	—	500	ns
Clock Pulsewidth (ϕ1, ϕ2)	$t_{pw\phi 1}$, $t_{pw\phi 2}$	200	—	—	200	—	—	ns
Start Pulse (ϕst) and Clock Pulse (ϕ2) Overlap	$t_{\phi ov}$	200	—	—	200	—	—	ns
Clock Pulse Space	X_1, X_2	0	—	—	0	—	—	ns
Data Rate ②	f	0.1	—	2000	0.1	—	2000	kHz
Video Delay Time (50% of saturation) ②	t_{vd}	—	70 (-128Q) –		—	80 (-256Q) –		ns
		—	110 (-256Q) –		—	120 (-512Q) –		ns
		—	140 (-512Q) –		—	160 (-1024Q) –		ns
Clock Pulse Line Capacitance (ϕ1, ϕ2) at 5V bias	Cϕ	—	21 (-128Q) –		—	27 (-256Q) –		pF
		—	36 (-256Q) –		—	50 (-512Q) –		pF
		—	67 (-512Q) –		—	100 (-1024Q) –		pF
Saturation Control Gate Line Capacitance (V_{scg}) at 5V bias	C_{scg}	—	12 (-128Q) –		—	12 (-256Q) –		pF
		—	20 (-256Q) –		—	24 (-512Q) –		pF
		—	35 (-512Q) –		—	45 (-1024Q) –		pF
Video Line Capacitance at 2V bias	C_V	—	7 (-128Q) –		—	10 (-256Q) –		pF
		—	11 (-256Q) –		—	16 (-512Q) –		pF
		—	20 (-512Q) –		—	30 (-1024Q) –		pF
Power Consumption	P	—	—	1	—	—	1	mW

① Vϕ is supply clock amplitude.
② Measured with a C4069 driver/amplifier circuit.

ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Parameters	Symbols	S3902 Series			S3903 Series			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel Pitch		—	50	—	—	25	—	μm
Pixel Height		—	0.5	—	—	0.5	—	mm
Photodiode Dark Current ①	I_D	—	0.08	0.15	—	0.04	0.08	pA
Photodiode Capacitance ①	C_{ph}	—	4	—	—	2	—	pF
Spectral Response Range (10% of peak)	λ	200 to 1000			200 to 1000			nm
Peak Sensitivity Wavelength	λp	—	600	—	—	600	—	nm
Saturation Exposure ① ②	E_{sat}	—	180	—	—	180	—	mlx•s
Saturation Charge ①	Q_{sat}	—	10	—	—	5	—	pC
Sensitivity Uniformity (50% of saturation, excluding first and last elements)		—	—	±3	—	—	±3	%

① Video bias voltage: 2.0V, Supply clock amplitude: 5.0V
② 2856 k Tungsten lamp

Figure 3: Typical Spectral Response

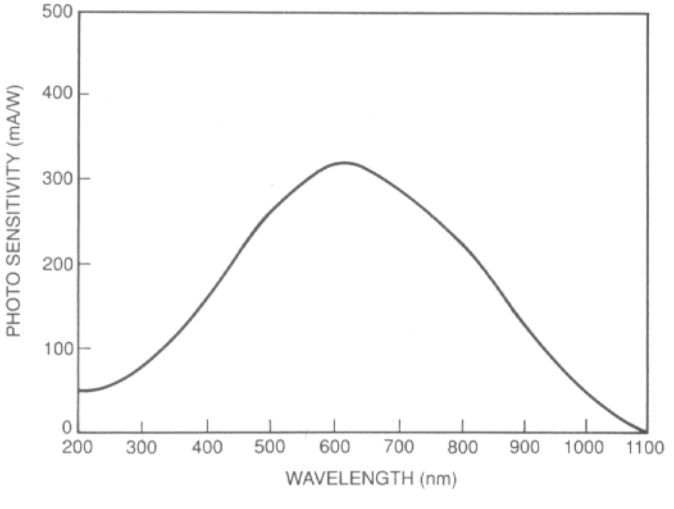
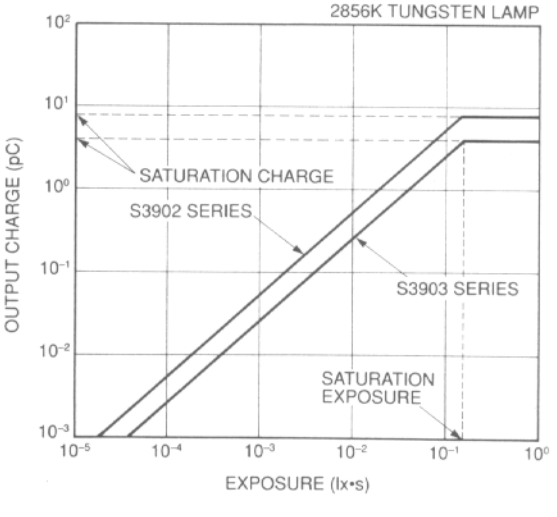
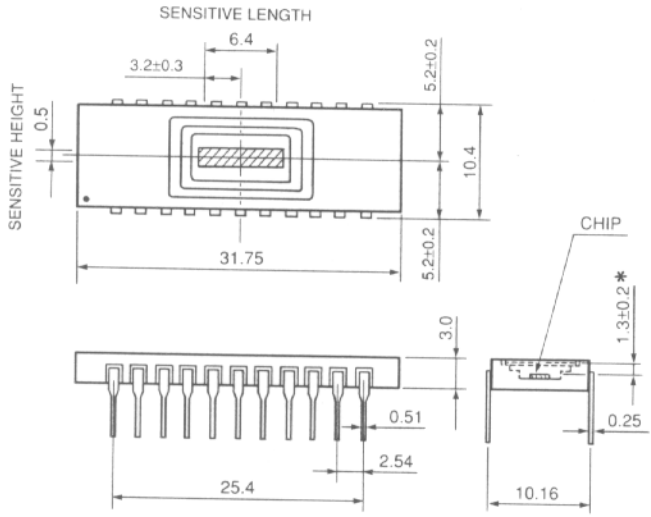


Figure 4: Output Charge vs. Exposure

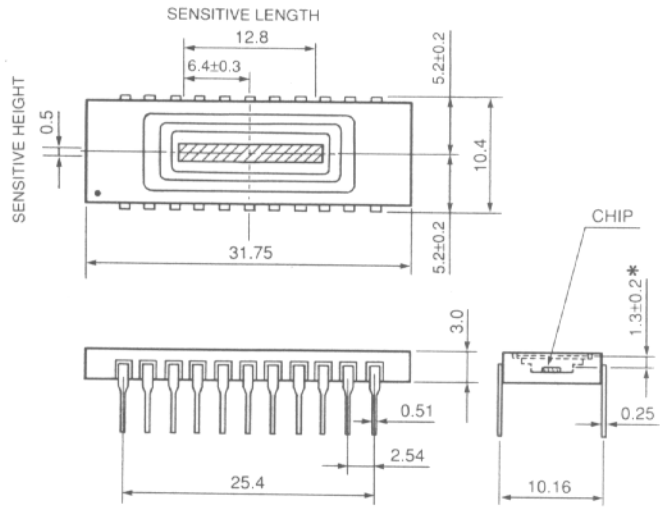


DIMENSIONAL OUTLINES (Unit: mm)

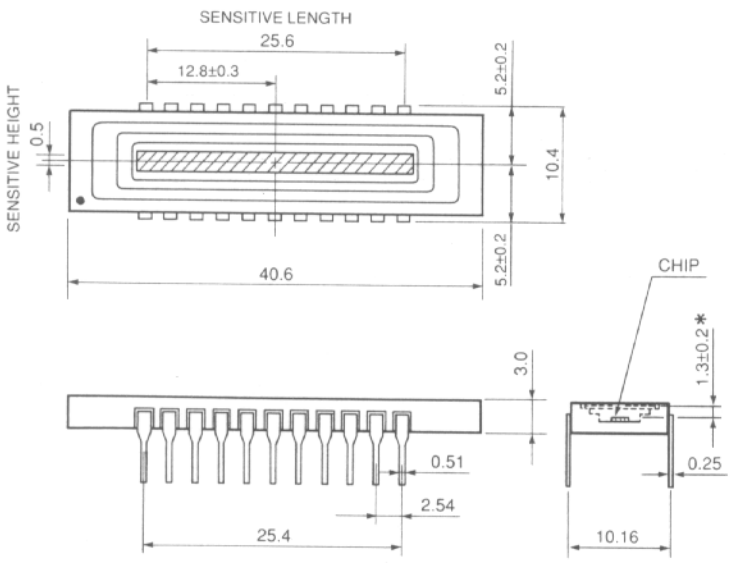
S3902–128Q
S3903–256Q



S3902–256Q
S3903–512Q



S3902–512Q
S3903–1024Q



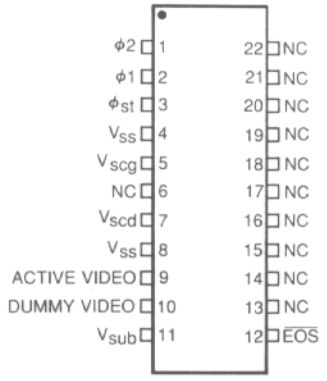
* Optical distance from the outer surface of the quartz window to the chip surface.

• Mechanical Specifications

Parameters	S3902 –128Q	S3902 –256Q	S3902 –512Q	S3903 –256Q	S3903 –512Q	S3903 –1024Q	Units
Number of Pixels	128	256	512	256	512	1024	—
Ceramic Length	31.75		40.6	31.75		40.6	mm
Number of Pins	22			22			—
Window Material ①	Quartz			Quartz			—
Net Weight	3.0		3.5	3.0		3.5	g

① Fiber optic window is available

PINOUT AND RECOMMENDED OPERATING CONDITIONS



V_{SS}, V_{sub} and NC should be grounded.

Terminals	Input or Output	Description
$\phi 1$, $\phi 2$	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. As the video output signal is obtained synchronized with the rise of $\phi 2$, the video data rate is equal to the clock pulse frequency.
ϕst	Input (CMOS logic compatible)	Pulse to start operation of the MOS shift register. The time interval between start pulses is equal to the signal accumulation time.
V_{SS}	Passive node	Connected to the anode of each photodiode. This should be grounded.
V_{scg}	Input	Used for restricting blooming. This should be set at the base line of each input pulse and is normally the ground level.
V_{scd}	Input	Used for restricting blooming. This shoud be biased at a voltage equal to the video bias at all times.
ACTIVE VIDEO	Output	Video output signal. A positive voltage should be applied to the video line which connects the photodiode cathodes so that each photodiode is reverse-biased. It is recommended that the video bias be 2V when the amplitude of $\phi 1$, $\phi 2$ and ϕst is at 5V.
DUMMY VIDEO	Output	This has the same structure as the active video, but is not connected to the photodiodes, so only spike noise is output. It should be biased at a voltage equal to the active video line. When in use otherwise, it should be open circuited.
V_{sub}	Passive node	Connected to the silicon substrate. This should be grounded.
$\overline{EOS}$	Output (CMOS logic compatible)	This should be pulled up to 5V using a 10kΩ resistor. Negative polarity. The end of scan signal is obtained synchronized with $\phi 2$ right after the last photodiode is addressed.
NC		No connection. These should be grounded.

DRIVER CIRCUIT

• Driver Circuit

No DC supply voltage is required for driving the S3902 and S3903 series MOS linear image sensors. The V_{SS}, V_{sub} and all NC terminals should be grounded, however. Driving the MOS shift register requires a start pulse (ϕst) and two-phase clock pulses (ϕ1, ϕ2). The polarities of ϕst, ϕ1 and ϕ2 are positive and these pulses are CMOS logic compatible.

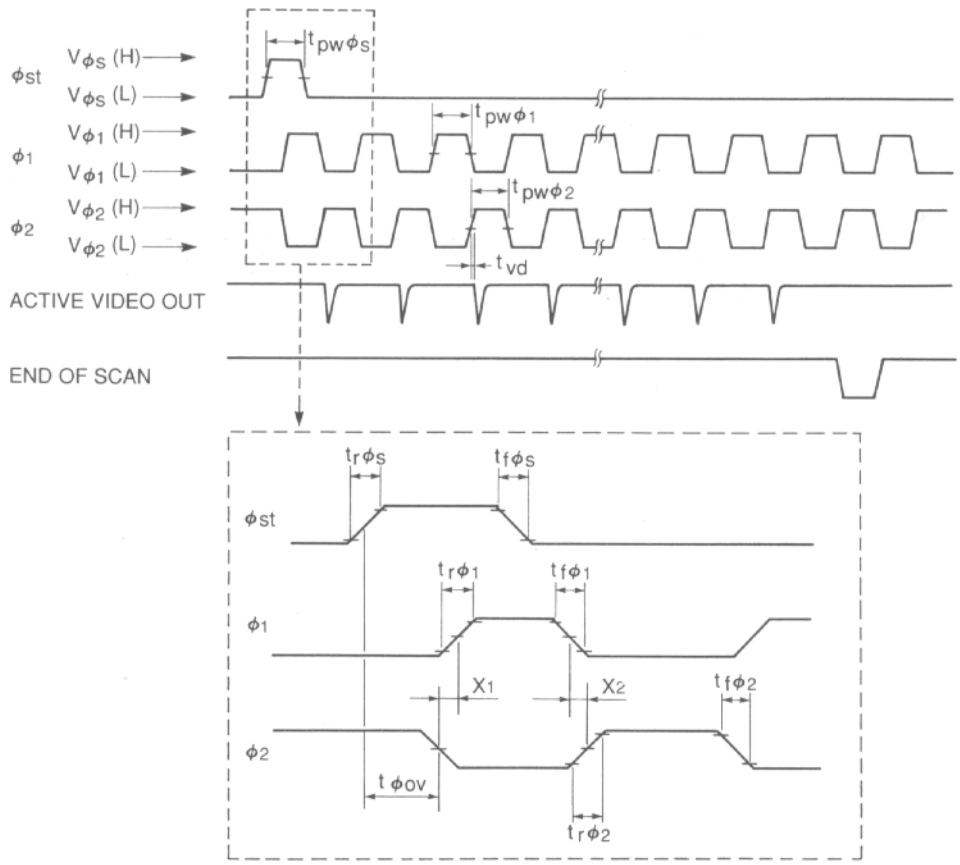
ϕ1 and ϕ2 can be either fully separated or in the complementary relation. However, the overlap should not exist at the rise or fall edge between ϕ1 and ϕ2. In other words, ϕ1 and ϕ2 must not be at the high level at the same time. The pulsewidth of ϕ1 and ϕ2 must be longer than 200 ns. Since the photodiode signal is obtained at the rise of every ϕ2, the clock pulse frequency determines the video data rate.

The amplitude of ϕst should be equal to that of ϕ1 and ϕ2. The shift register starts to read out the signal with the high level of ϕst, so the time interval of each ϕst determines the signal accumulation time. The pulsewidth of ϕst must also be longer than 200ns and must be overlapped with ϕ2 for at least 200ns. Moreover, in order to start the shift register normally, ϕ2 must be changed only once from the high level to the low level during the high level of ϕst. The timing diagram for each pulse is shown in Figure 5.

• End of Scan ($\overline{EOS}$)

By wiring the $\overline{EOS}$ terminal to 5V using a pull-up resistor of 10kΩ, the end of scan signal is obtained, synchronized with ϕ2 right after the last photodiode is addressed.

Figure 5: Timing Diagram for Drive Circuit



• Signal Readout Circuit

Signal readout methods consist of the current-detection mode (current-voltage conversion mode) using a resistive load and the current-integration mode using a charge amplifier. In either method, a positive bias must be applied to the video line because the photodiode anodes of a MOS linear image sensor are at 0V (V_{SS}). Figure 6 shows the video bias voltage margin. Higher supply clock amplitude allows larger video bias and saturation charge. Conversely, if the video bias is set at a low level with higher supply clock amplitude, the fall time of the video output waveform can be shortened. It is recommended that the video bias be set at 2V when the amplitude of ϕ1, ϕ2 and ϕst is 5V.

To obtain a good output linearity, the current-integration mode is suggested. In this mode, immediately before each photodiode is addressed, the integration capacitance is reset at the reference voltage level, and when the address switch is turned on, the signal charge is accumulated in the integration capacitance. Figure 7 shows an example of the current-integration circuit and the pulse timing. To obtain a stable output, the rise edge of the reset pulse should be delayed by at least 50 ns from the fall edge of $\phi 2$.

Hamamatsu provides driver/amplifier circuits; the C4070 for the current-integration mode and the C4069 for the current-voltage conversion mode. In addition, the C4091 pulse generator is available, which supplies these driver/amplifier circuits with a master start pulse and a master clock pulse.

Figure 6: Video Bias Voltage Margin

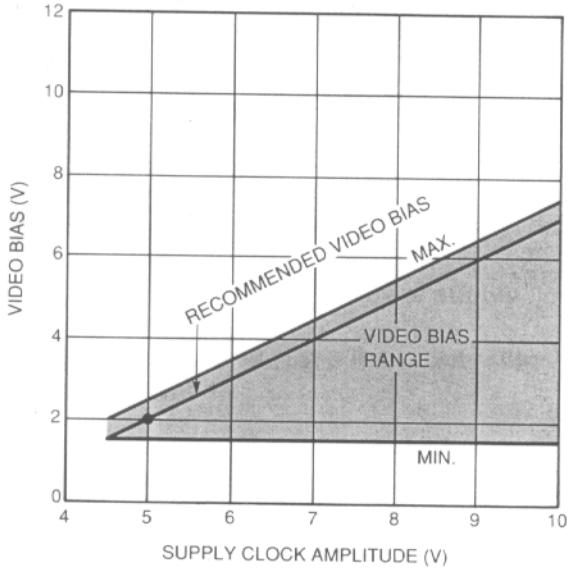
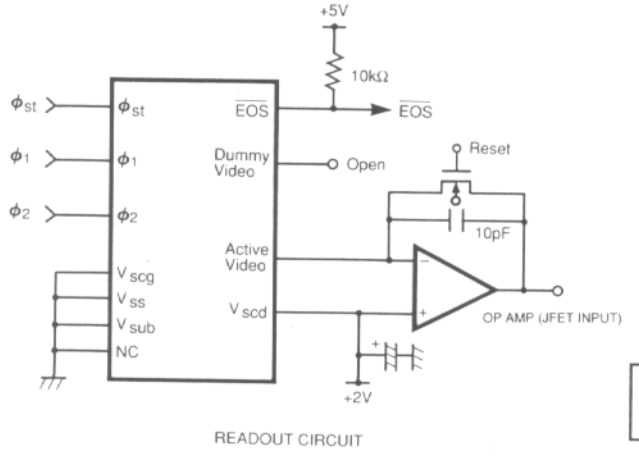
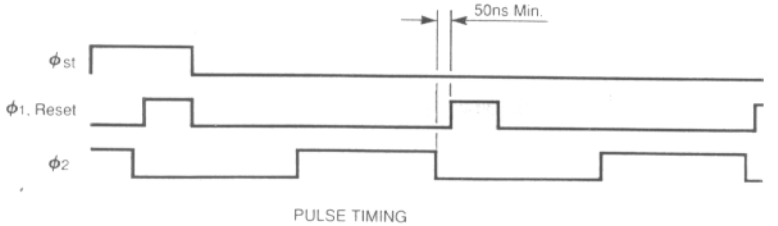


Figure 7: Recommended Readout Circuit and Timing Diagram



READOUT CIRCUIT

$$V_{output}\,[V] = \frac{\text{OUTPUT CHARGE [C]}}{10 \times 10^{-12}\,[F]}$$



PULSE TIMING

• Operation for Anti-blooming

When light higher than the saturation exposure strikes the sensitive area, even partially, the photodiode in a MOS linear image sensor cannot accumulate a signal charge exceeding the saturation charge amount. The excess charge begins to overflow into the video line, thus causing deterioration of the signal purity. In order to eliminate this phenomenon, the saturation control drain should be set at a voltage equal to the video bias, and the gate should be grounded. Under normal operating conditions, the MOS linear image sensor will show an excellent antiblooming characteristic.

When a MOS linear image sensor is used at a light level lower than the saturation exposure, the same bias condition is applicable.

However, under extremely high contrast conditions, a voltage equal to the video bias should be applied to the saturation control drain. Also, a bias voltage (less than 1V) should be applied to the saturation control gate. The larger the bias voltage for the saturation control gate, the higher the saturation control function will be. However, a larger bias voltage also causes a decrease in the saturation charge amount.

APPENDIX

1) **Operation for all photodiodes reset:**
In normal operation, the charge accumulated in the photodiode is reset when the signal is read out. For the S3902 and S3903 series, the signal charge can be reset at a line other than the signal readout. This is done by adding an appropriate pulse to the saturation control gate. The amplitude of this pulse should be equal to $\phi 1$, $\phi 2$ and ϕst, and the pulsewidth should be longer than 5μs.

When the saturation control gate is set at the high level, all photodiodes are reset simultaneously at the potential of the saturation control drain. (Therefore, the saturation control drain should be set at the same potential as the video bias, and is typically 2V.) On the contrary, when the saturation control gate is set at the low level, the signal charge accumulates in the photodiode without a reset being carried out.

2) **Dummy video:**
The S3902 and S3903 series have a dummy video line to eliminate the spike noise in the video output waveform. A video signal with lower spike noise can be obtained by the differential amplification of the active video line and the dummy video line outputs. But, in a normal operation, the dummy video line needs not to be used. Leave it unconnected.