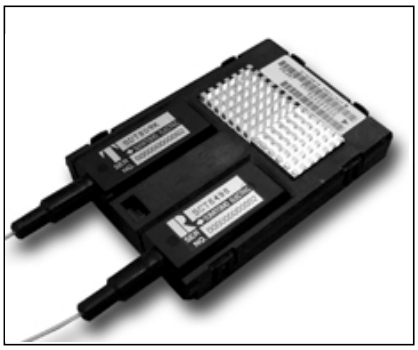
Specification: TS-S00D049A
December, 2000

Advanced Specification

SDG1202 Series OC-48 Optical Transceiver

with Mux / Demux (16x155.52Mb/s)



Features

- **2.488Gbps High Speed Optical I/F**
- **SONET / SDH Compliant**
- **155.52Mbps LVPECL I/F**
- **Pigtailed Compact Package**
- **Single +3.3V Operation**
- **Optical Transmitter Disable**
- **LD Bias Current Monitor**
- **Optical Receiver Loss of Signal Alarm**
- **Multi Source Product**

General Description

The SDG1202 2.5Gb/s Optical Transceiver is a fully integrated SONET OC-48 photonic layer transceiver including serialization and deserialization function of section layer of SONET/SDH. The SDG1202 converts a 16bit 155.52Mb/s parallel electrical data stream to a 2.48832Gb/s optical data signal and a 2.48832Gb/s optical data signal to a 16bit 155.52Mb/s parallel electrical data stream. This SONET/SDH compliant Optical Interface is suitable for SONET/SDH equipment as well as other high-speed data communication equipment. The 16bit LVPECL interface is compatible with CMOS Framer and Mapper chipset.

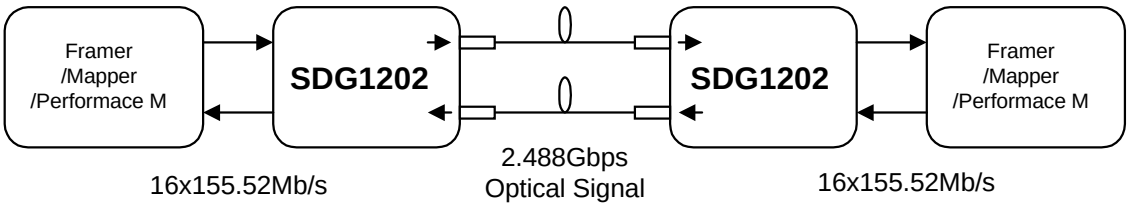


Figure 1. Application Block Diagram

1. SDG1202 Functional Block Diagram

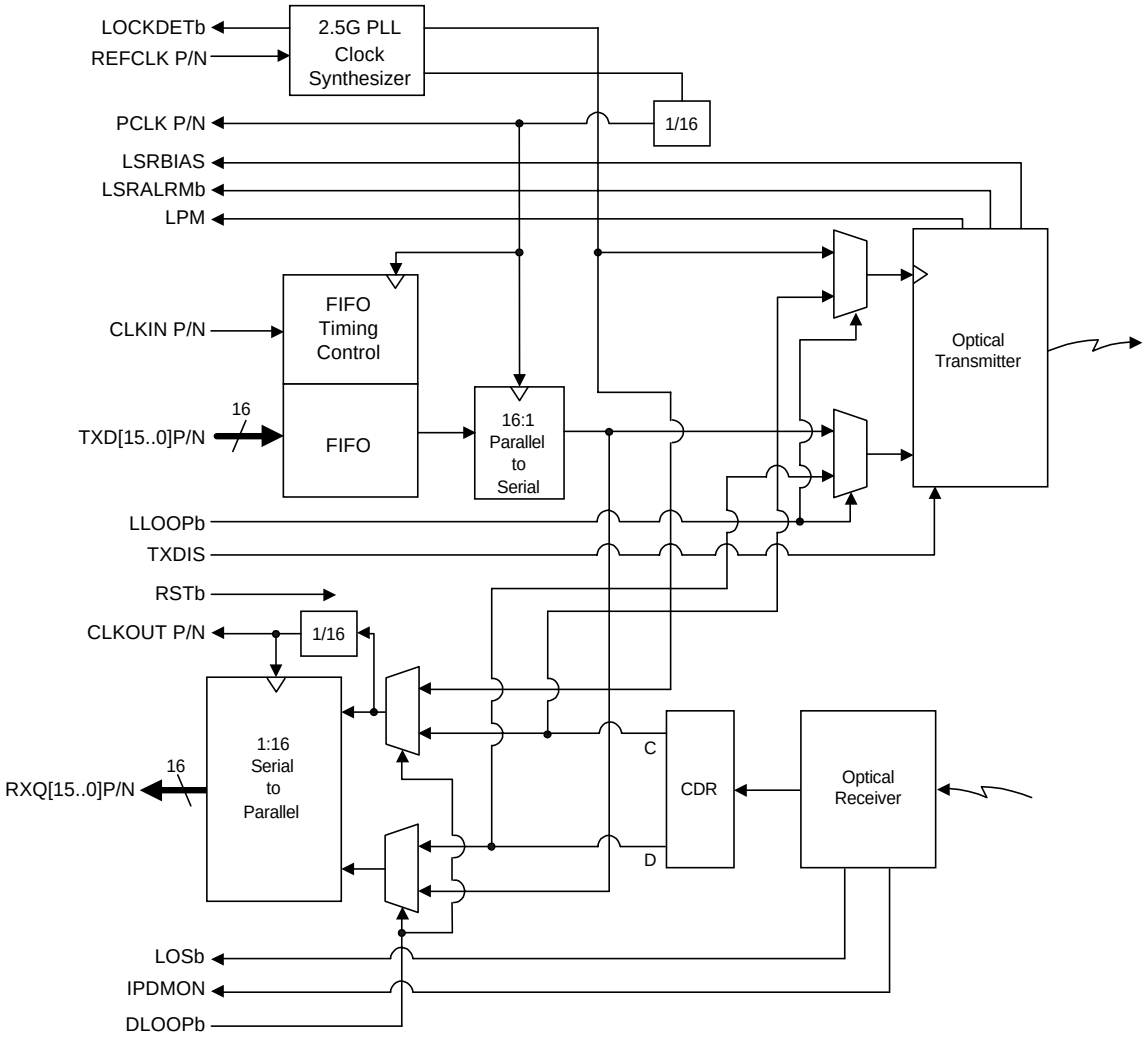
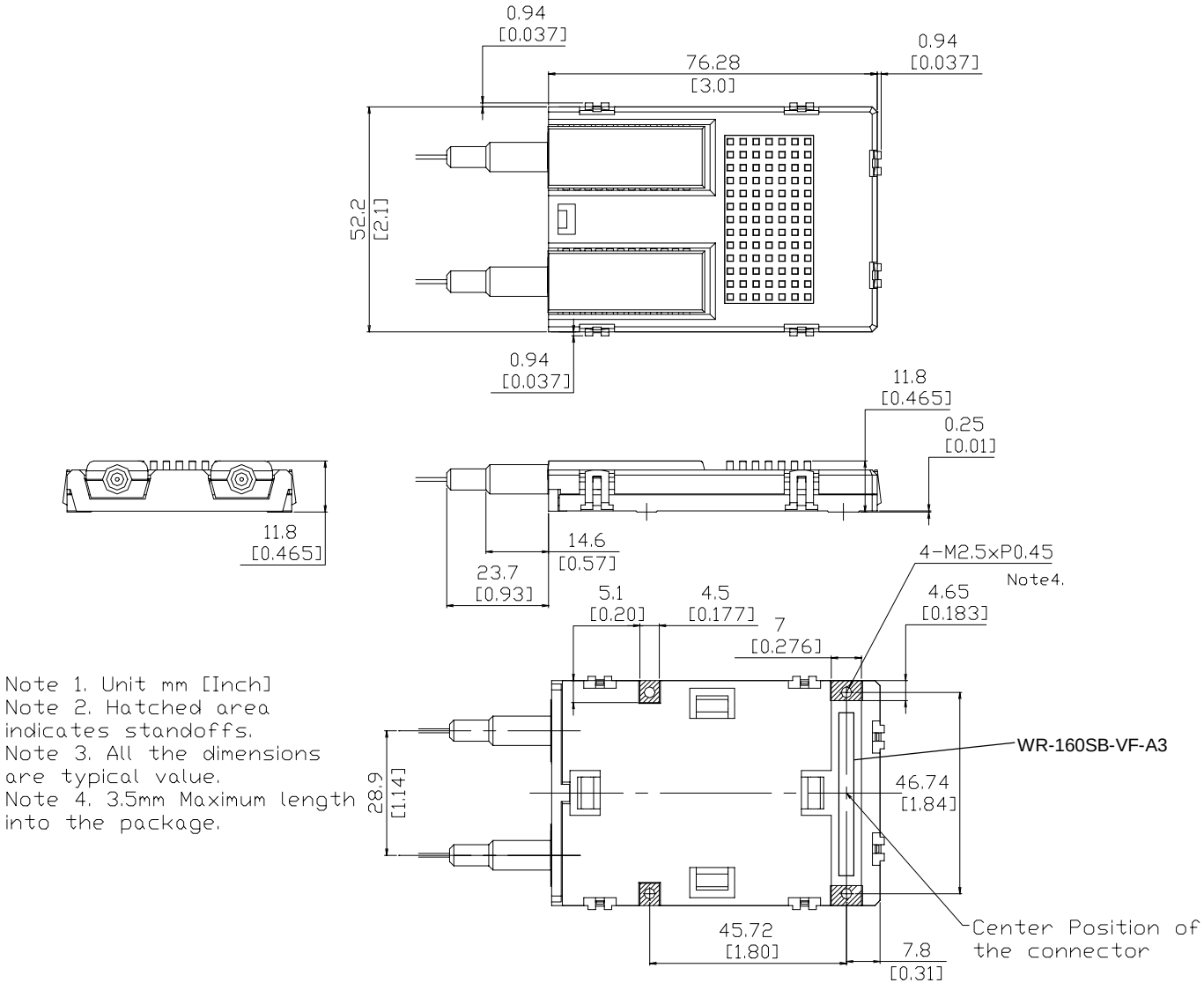


Figure 2. SDG1202 Functional Block Diagram

2. Package Dimension



Note 1. Unit mm [Inch]
Note 2. Hatched area indicates standoffs.
Note 3. All the dimensions are typical value.
Note 4. 3.5mm Maximum length into the package.

Figure 3. Package Dimension

Board Connector: 160-PIN JAE Connector P/N : WR-160SB-VF-A3
Mates with WR-160PB-VF50-A3

Table 1. Fiber Pigtail and Optical Connector

Parameter	Min	Typ	Max	Unit
Fiber Type		Single Mode Fiber		
Outer Jacket Diameter		0.9		mm
Fiber Clad Diameter		125		μm
Mode Field Diameter		9.5		μm
Fiber Bending Radius	25.4			mm
Connector Insertion Loss			0.5	dB
Connector Optical Reflectance			-45	dB

3. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Storage Temperature	Tst	-40	+85	degC	
Operating Case Temperature	Topc	TBD	TBD	degC	
Operating Ambient Temperature	Topa1	0	+70	degC	1
Operating Ambient Temperature	Topa2	0	TBD	degC	2
Supply Voltage with respect to GND	Vccmdm	0	+3.6	V	
	Vcctx	0	+3.6	V	
	Vccrx	0	+3.6	V	
Voltage on LVPECL Input	Vlvpi	0	Vccmdm	V	
Source Current on LVPECL Output	Ilvpo	0	24	mA	
Voltage on LVTTL Input	Vlvti	0	Vccmdm	V	

Note:

1: with 1m/s air flow

2: without air flow

4. Pin Assignment and Description

80	NC	160	NC
79	NC	159	NC
78	NC	158	NC
77	NC	157	NC
76	NC	156	NC
75	GND	155	GND
74	RXQ00N	154	RXQ01N
73	RXQ00P	153	RXQ01P
72	RXQ02N	152	RXQ03N
71	RXQ02P	151	RXQ03P
70	GND	150	GND
69	RXQ04N	149	RXQ05N
68	RXQ04P	148	RXQ05P
67	RXQ06N	147	RXQ07N
66	RXQ06P	146	RXQ07P
65	GND	145	GND
64	RXQ08N	144	RXQ09N
63	RXQ08P	143	RXQ09P
62	RXQ10N	142	RXQ11N
61	RXQ10P	141	RXQ11P
60	GND	140	GND
59	RXQ12N	139	RXQ13N
58	RXQ12P	138	RXQ13P
57	RXQ14N	137	RXQ15N
56	RXQ14P	136	RXQ15P
55	GND	135	GND
54	NC	134	NC
53	NC	133	NC
52	NC	132	NC
51	GND	131	NC
50	GND	130	CLKOUTN
49	GND	129	CLKOUTP
48	Vccrx	128	Vccrx
47	GND	127	GND
46	GND	126	GND
45	NC	125	NC
44	Vccmdm	124	Vccmdm
43	Vccmdm	123	Vccmdm
42	GND	122	GND
41	NC	121	NC
40	NC	120	GND
39	NC	119	LOSb
38	DLOOPb	118	LLOOPb
37	NC	117	NC
36	LSRBIAS	116	NC
35	LSRALRMb	115	TXDIS
34	LPM	114	NC
33	GND	113	NC
32	Vcctx	112	Vcctx
31	Vcctx	111	Vccmdm
30	GND	110	GND
29	Vccmdm	109	GND
28	Vccmdm	108	PCLKN
27	GND	107	PCLKP
26	LOCKDETb	106	GND
25	CLKINN	105	TXD00N
24	CLKINP	104	TXD00P
23	GND	103	GND
22	TXD01N	102	TXD02N
21	TXD01P	101	TXD02P
20	TXD03N	100	TXD04N
19	TXD03P	99	TXD04P
18	GND	98	GND
17	TXD05N	97	TXD06N
16	TXD05P	96	TXD06P
15	TXD07N	95	TXD08N
14	TXD07P	94	TXD08P
13	GND	93	GND
12	TXD09N	92	TXD10N
11	TXD09P	91	TXD10P
10	TXD11N	90	TXD12N
9	TXD11P	89	TXD12P
8	GND	88	GND
7	TXD13N	87	TXD14N
6	TXD13P	86	TXD14P
5	TXD15N	85	REFCLKN
4	TXD15P	84	REFCLKP
3	GND	83	GND
2	IPDMON	82	RSTb
1	NC	81	NC

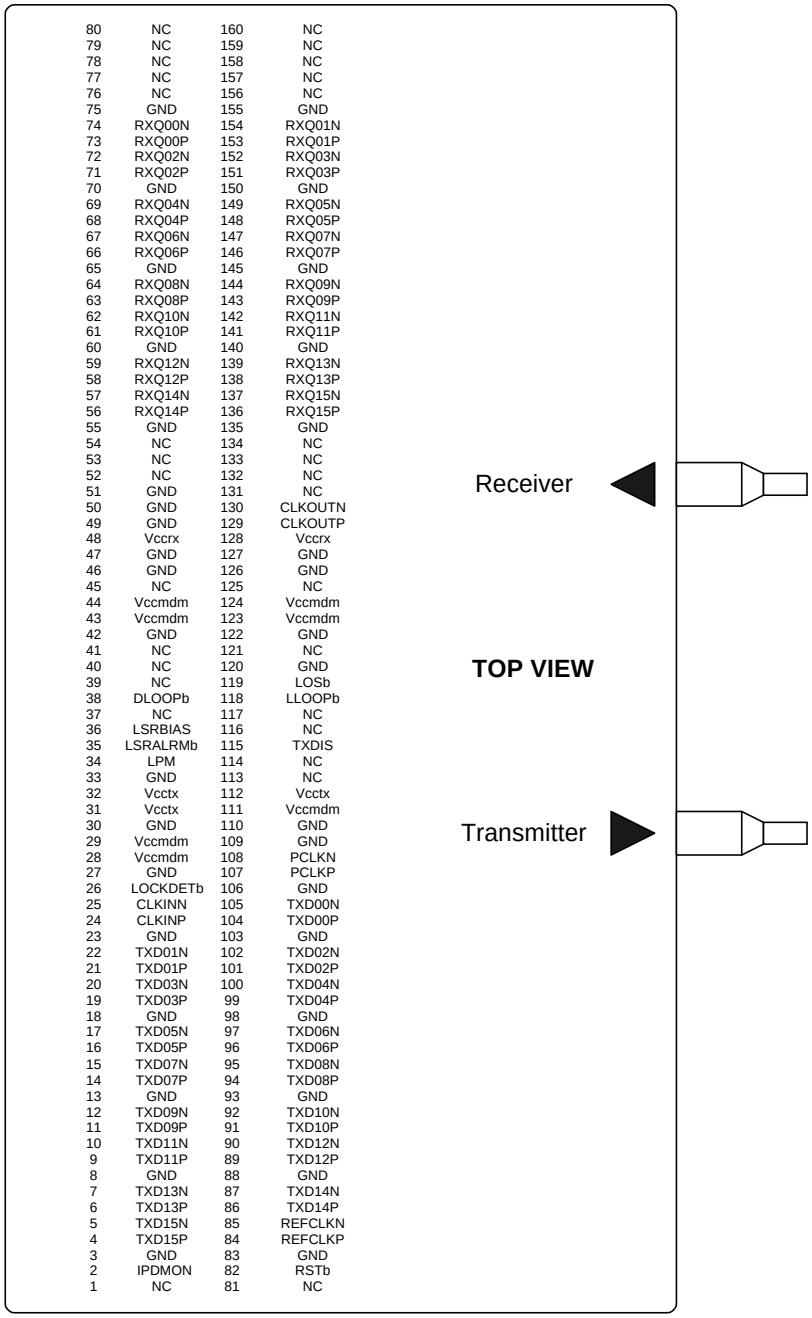


Figure 4. Pin Assignment

Table 3. Pin Assignment and Description (Transmitter Side)

Pin Name	I/O	Description	Pin #
TXD00 P/N	I	Transmitter parallel data input, Differential LVPECL, TXD15 P/N is the Most Significant Bit and transmitted first followed by the subsequent bits with the TXD00 P/N (Least Significant Bit), sampled on rising edge of CLKINP.	104/105
TXD01 P/N			21/22
TXD02 P/N			101/102
TXD03 P/N			19/20
TXD04 P/N			99/100
TXD05 P/N			16/17
TXD06 P/N			96/97
TXD07 P/N			14/15
TXD08 P/N			94/95
TXD09 P/N			11/12
TXD10 P/N			91/92
TXD11 P/N			9/10
TXD12 P/N			89/90
TXD13 P/N			6/7
TXD14 P/N			86/87
TXD15 P/N			4/5
CLKIN P/N	I	Transmitter parallel clock input, Differential LVPECL.	24/25
REFCLK P/N	I	Reference Clock for 2.5G PLL CSU, Differential LVPECL, Internally biased and terminated and Internally ac-coupled.	84/85
LPM	O	Transmitter Output Power Monitor Voltage	34
LSRALRMb	O	Transmitter Alarm, LVTTL, Low when Optical Output Power has degraded 3dB from its nominal power	35
LSRBIAS	O	Laser Bias Current Monitor Voltage	36
PCLK P/N	O	155MHz, Parallel Byte Clock Output, Differential LVPECL	107/108
LOCKDETb	O	LOCKDETb, Goes low when CSU PLL is locked	26
TXDIS	I	Transmitter Disable, LVTTL, Shut off when High	115

Table 3. Pin Assignment and Description (Receiver Side)

Pin Name	I/O	Description	Pin #
RXQ00 P/N	O	Receiver parallel data output, Differential LVPECL, RXQ15 P/N is the Most Significant Bit and received first followed by the subsequent bits with RXQ00 P/N(Least Significant Bit), updated on the falling edge of CLKOUTP	73/74
RXQ01 P/N			153/154
RXQ02 P/N			71/72
RXQ03 P/N			151/152
RXQ04 P/N			68/69
RXQ05 P/N			148/149
RXQ06 P/N			66/67
RXQ07 P/N			146/147
RXQ08 P/N			63/64
RXQ09 P/N			143/144
RXQ10 P/N			61/62
RXQ11 P/N			141/142
RXQ12 P/N			58/59
RXQ13 P/N			138/139
RXQ14 P/N			56/57
RXQ15 P/N			136/137
CLKOUT P/N	O	Receiver Parallel Clock Out. Differential LVPECL	129/130
LOSb	O	Loss of Signal, LVTTL	119
IPDMON	O	Input Power Monitor Current, Analog This pin should be connected to +3.3V when it is not used.	2

Table 3. Pin Assignment and Description (Supply and Common)

Pin Name	I/O	Description	Pin #
RSTb	I	Master Reset, Active Low	82
DLOOPb	I	Diagonostic Loopback Enable,LVTTL, Active Low	38
LLOOPb	I	Line Loopback Enable, LVTTL, Active Low	118
Vccmdm	Supply	+3.3V power supply for Digital Circuit	28, 29, 43, 44, 111, 123, 124
Vcctx	Supply	+3.3V power supply for Transmitter	31, 32, 112
Vccrx	Supply	+3.3V power supply for Receiver	48, 128
GND	GND	Ground	3, 8, 13, 18, 23, 27, 30,33, 42, 46, 47, 49, 50, 51, 55, 60, 65, 70, 75, 83, 88, 93, 98, 103, 106, 109, 110, 120, 122,126, 127, 135, 140, 145, 150, 155
NC	-	Not connected internally, reserved for future options	1, 37, 39, 40, 41, 45, 52, 53, 54, 76, 77, 78, 79, 80, 81, 113, 114, 116, 117, 121, 125, 131, 132, 133, 134, 156, 157, 158, 159, 160

5. Electrical Interface

5-1. DC Characteristics

Table 4. DC Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
Supply Voltage		Vcc33	3.135	3.3	3.465	V	
Supply Current	(Vccmdm)	Iccmdm			TBD	mA	1
	(Vcctx)	Icctx			TBD	mA	1
	(Vccrx)	Iccrx			TBD	mA	1
Total Power Consumption		Ptotal		4.5	6.5	W	
LVPECL Input Voltage	(low)	Vilvpl	Vcc-2.00		Vcc-1.40	V	2
	(high)	Vilvph	Vcc-1.25		Vcc-0.55	V	2
LVPECL diff. Input Swing		dVindiff	500		2000	mV	
LVPECL Output Voltage	(low)	Volvpl	Vcc-1.88		Vcc-1.44	V	2, 3
	(high)	Volvph	Vcc-1.09		Vcc-0.83	V	2, 3
LVPECL diff. Output Swing		dVoutdiff	1000		1600	mV	3
LVTTL Output Voltage	(low)	Vottll			0.5	V	
	(high)	Vottlh	2.4			V	
LVTTL Input Voltage	(low)	Vilvttll	0		0.8	V	
	(high)	Vilvttlh	2		3.465	V	
IPDMON Current		Ipdmon		0.7A/W		A/μW	
LD bias Mon Voltage		Vldbmon	19	20	21	V/A	4

Note:

1. Output Current is not included.
2. Shall be applied for both single-ended and differential LVPECL Input,
   Differential LVPECL Input shall have same DC characteristics as single-ended LVPECL.
3. w/ 50ohm AC coupled load
4. Vldbmon=20x(LD bias current)

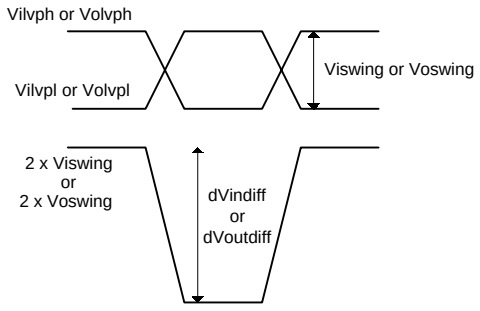


Figure 5. Definition of dV

5-2. Transmitter AC Characteristics

Table 5. Transmitter AC Timing Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
CLKIN Frequency		Fclkin		155.520		MHz	
CLKIN Tolerance		dFclkin	-50		+50	ppm	
REFCLK Input Jitter		Jitterin			-140	dBc/ Hz	1
CLKIN Duty Cycle		dcin	40		60	%	
CLKIN Acquisition Time		Tpllaqs			TBD	ms	2
CLKIN Rise/Fall Time		Trc/Tfc			1.5	ns	
TXD Rise /Fall Time		Trd/Tfd			1.5	ns	
Skew drift CLKIN vs PCLK		Tsd	-5		5	ns	3
CLKIN/TXD Alignment	setup	Tiset	1.5			ns	4
	hold	Tihold	0.5			ns	4
TXDIS Response Time	Off	Ttxoff			100	µs	
	On	Ttxon			3	ms	

Note:

1: when 50kHz

2: Please refer to Figure 6.

3: After the FIFO is initialized.

4: with respect to the falling edge of CLK_IN

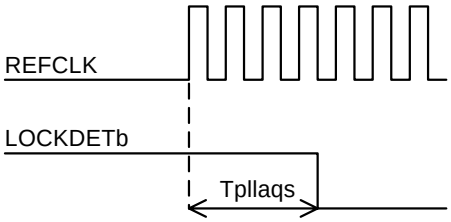


Figure 6. PLL Acquisition Timing

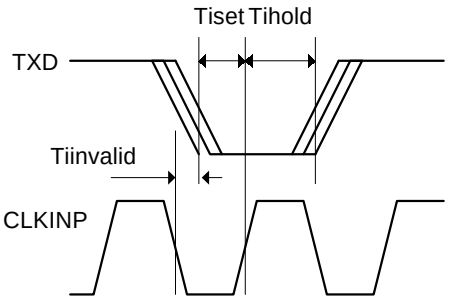


Figure 7. Transmitter Input Timing

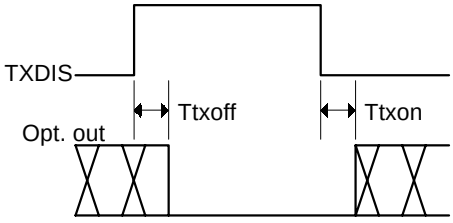


Figure 8. Transmitter Disable Response

5-3. Receiver AC Characteristics

Table 6. Receiver AC Timing Characteristics

Parameter		Sym.	Min	Typ	Max	Unit	Note
CLKOUT Frequency		Fclko		155.520		MHz	
CLKOUT Tolerance		dFclko	-100		+100	ppm	1
CLKOUT Duty Cycle		dco	45		55	%	
CLK Acquisition Time		Tpllaqs		TBD	TBD	ms	2
CLKOUT Rise/Fall Time		Trc/Tfc			1.5	ns	
RXQ Rise /Fall Time		Trd/Tfd			1.5	ns	
CLKOUT/RXQ Alignment	invalid	Toinvalid	-1.8		+1.8	ns	3
	setup	Toset	2.2			ns	4
	hold	Tohold	2			ns	4
LOSb Response Time		Tlightoff	2.3		100	µs	
		Tlighton	2.3		100	µs	

Note:

1: Depends on an optical input signal.

2: After receiving optical signal.

3: with respect to the falling edge of CLK_OUT

4: with respect to the rising edge of CLK_OUT

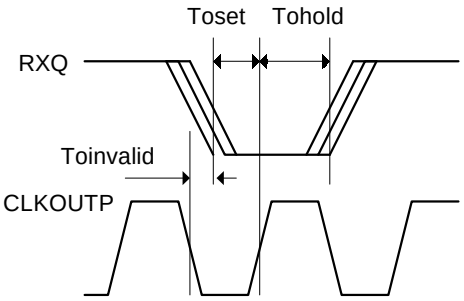


Figure 9. Receiver Output Timing

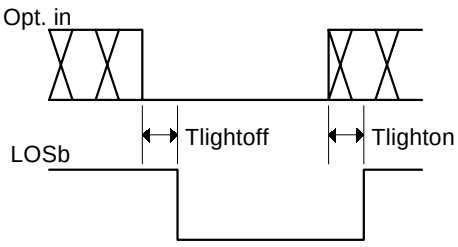


Figure 10. LOSb Response Time

6. Optical Interface

6-1. Transmitter Optical Interface Characteristics

Table 7. Transmitter Optical Interface

Parameter	Sym.	Min	Typ	Max	Unit	Note
Center Wavelength	Lc	1265		1360	nm	1, 2, 3, 4
Center Wavelength	Lc	1500		1580	nm	1, 5
Spectral Width RMS	dL	0		4.0	nm	1, 2
Spectral Width -20dB	dL			1	nm	1, 3, 4, 5
Side Mode Suppression Ratio	SSR	30			dB	1, 3, 4, 5
Optical Output Power ave.	Po	-10		-3	dBm	1, 2
Optical Output Power ave.	Po	0		-5	dBm	1, 3
Optical Output Power ave.	Po	-2		+3	dBm	1, 4, 5
Disabled Output Power	Pooff			-45	dBm	
Extinction Ratio	Er			8.2	dB	1
Optical Pulse Mask	-	Compliant with GR-253			-	6
Jitter Generation rms	Tjgrms	0		0.01	UIrms	7, 8
p-p	Tjgpp	0		0.1	UIp-p	7, 8

Note

1: 2.48832Gbps, PRBS 2^23-1

2: Applied for SR / I-16 application (1.3μmFP-LD)

3: Applied for IR-1 / I-16.1 application (1.3μm DFB-LD)

4: Applied for LR-1/ L-16.1 application (1.3μm DFB-LD)

5: Applied for LR-2 /L-16.2 application (1.55μm DFB-LD)

6: Refer to Figure.11.

7: Measured with a bandpass filter having a high-pass cutoff frequency of 12kHz and
a low-pass cutoff frequency of 20MHz

8: Input jitter shall not exceed the specified value in Table 5.

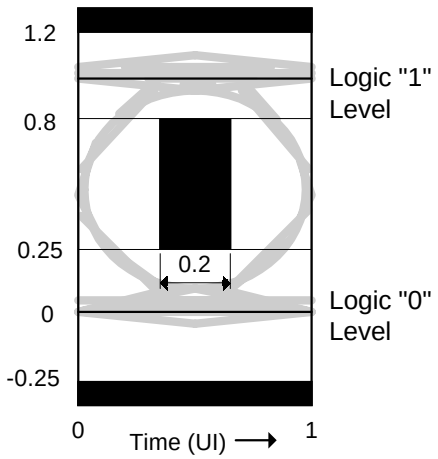


Figure 11. Transmitter Pulse Mask

6-2. Receiver Optical Interface Characteristics

Table 8. Receiver Optical Interface

Parameter		Sym.	Min	Typ	Max	Unit	Note
Input Center Wavelength		Lc	1265		1360	nm	1,2,3,4
Input Center Wavelength		Lc	1500		1580	nm	5
Optical Input Power		Pin	-18		0	dBm	1,2,3
Optical Input Power		Pin	-28		-9	dBm	1,4,5
Receiver Power Penalty		Rpo			1		1,2,3,4
Receiver Power Penalty		Rpo			2		1, 5
Optical Reflectance		ORLr			-27	dB	
Jitter Tolerance		-	Compliant with GR-253 and ITU-T G958			-	6
LOS Input Power Level	->LOS	Plosd			-22	dBm	1,2,3,7
	LOS->	Plosa			-22	dBm	1,2,3,8
LOS Input Power Level	->LOS	Plosd			-30	dBm	1,4,5,7
	LOS->	Plosa			-30	dBm	1,4,5,8

Note:

1: 2.48832Gb/s, PRBS 2^23-1, BER<1x10^-10

2: Applied for SR / I-16 application (1.3μmFP-LD)

3: Applied for IR-1 / I-16.1 application (1.3μm DFB-LD)

4: Applied for LR-1/ L-16.1 application (1.3μm DFB-LD)

5: Applied for LR-2 /L-16.2 application (1.55μm DFB-LD)

6: 1dB power penalty with 15UIp-p from 10Hz to 600Hz, 1.5UIp-p from 6kHz to 100kHz and 0.15UIp-p from 1MHz and above.

7: Decreasing light input

8: Increasing light input

7. Recommended User Interface

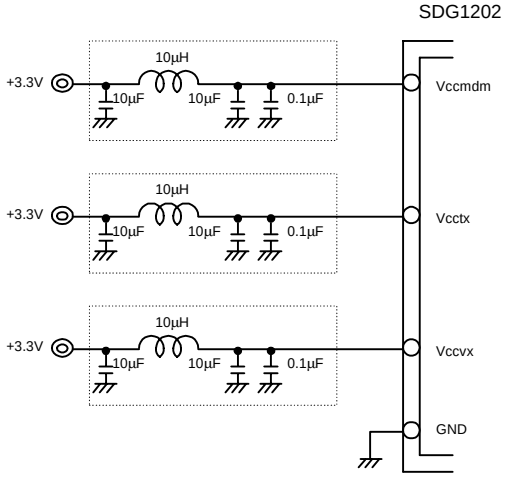


Figure 12. Power Supply Line

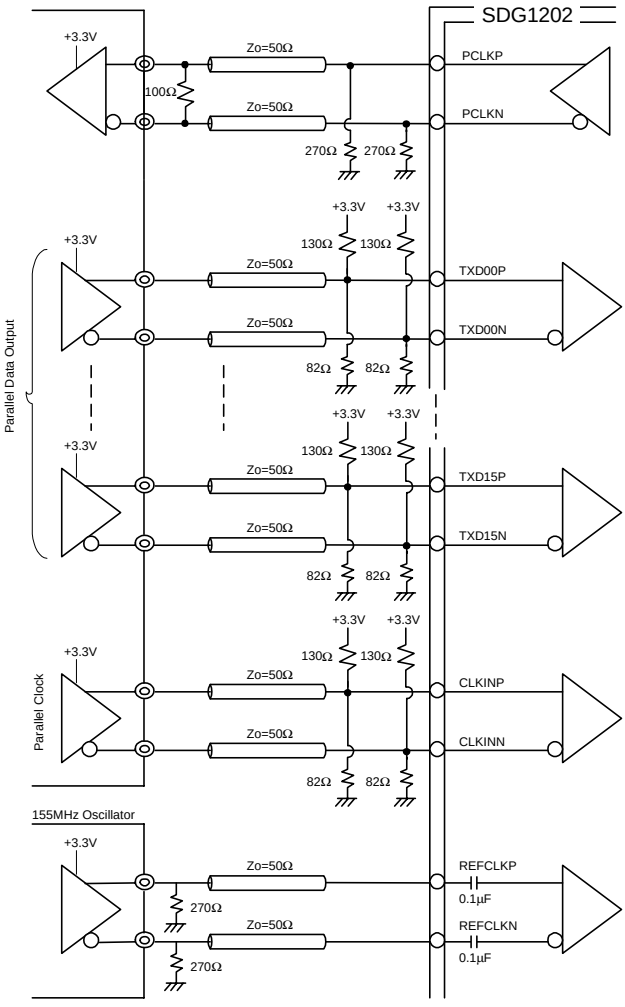


Figure 13. Data and Clock Input

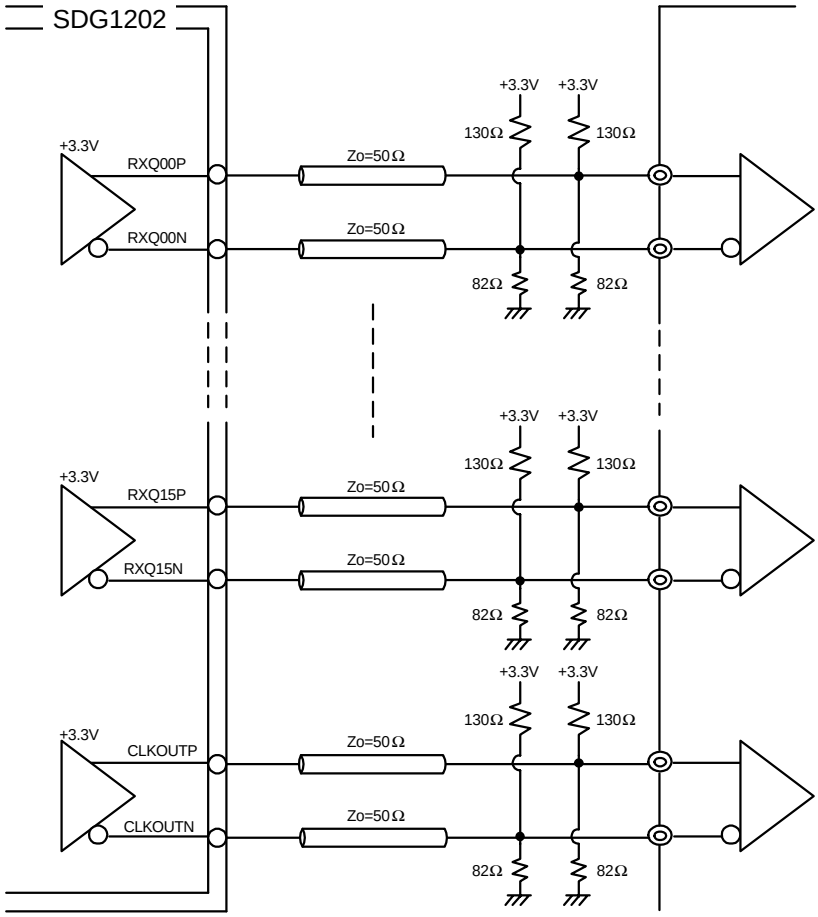


Figure 14. Data and Clock Output

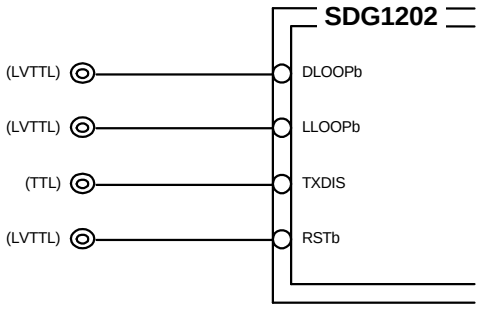


Figure 15. Command Input

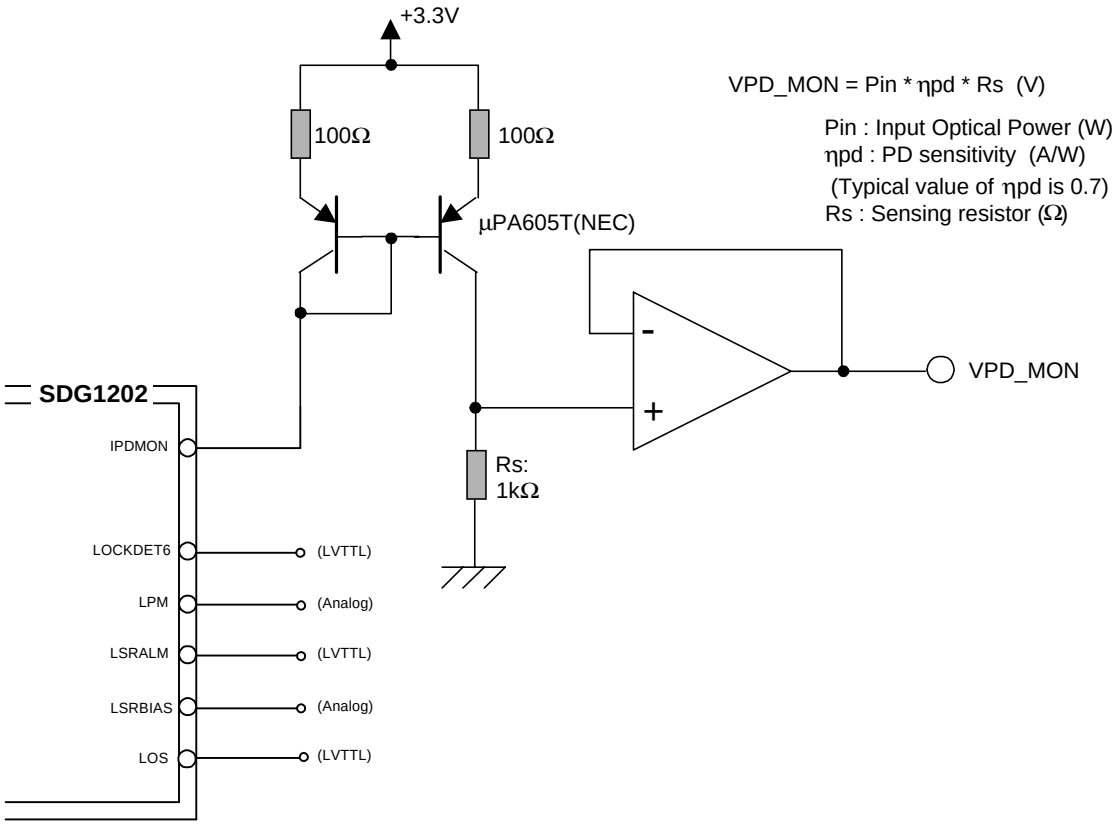
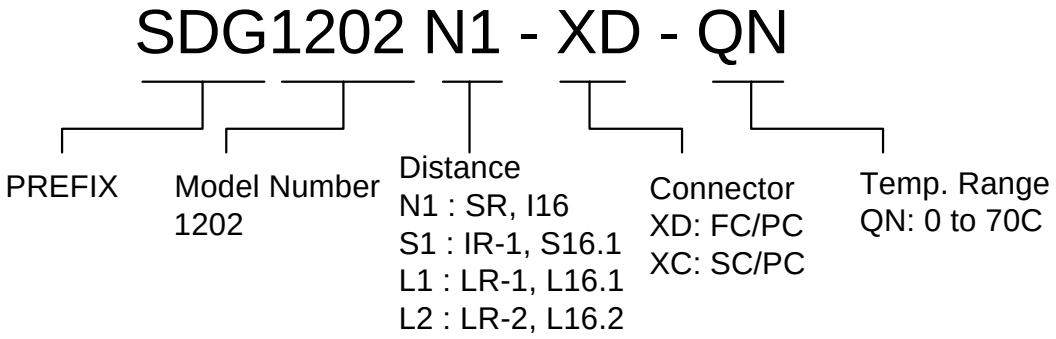


Figure 16. Monitoring Function

8. Part Numbering Information



9. For More Information

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