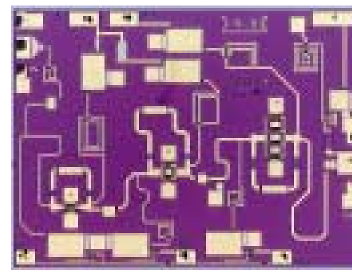
RMWB12001
12 GHz Buffer Amplifier MMIC

Description

The RMWB12001 is a 3-stage GaAs MMIC amplifier designed as an 8.5 to 12 GHz Buffer Amplifier for use in the LO chain of point to point radios, point to multi-point communications, LMDS, and other millimeter wave applications. In conjunction with other Raytheon amplifiers, multipliers and mixers it forms part of a complete 23 and 26 GHz transmit/receive chipset. The RMWB12001 utilizes Raytheon's 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of medium power amplifier applications.

Features

- 4 mil substrate
- Small-signal gain 25 dB (typ.)
- 3 dB compressed Pout 21 dBm (typ.)
- Voltage detector included to monitor Pout
- Chip size 2.2 mm x 1.7 mm



Maximum Ratings

Parameter	Symbol	Value	Unit
Positive DC Voltage (+4 V Typical)	Vd	+6	Volts
Negative DC Voltage	Vg	-2	Volts
Simultaneous (Vd - Vg)	Vdg	8	Volts
Positive DC Current	I_D	207	mA
RF Input Power (from 50 Ω source)	P_{IN}	+8	dBm
Operating Baseplate Temperature	T_C	-30 to +85	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R_{jc}	120	°C/W

Electrical Characteristics (At 25°C), 50 Ω system, Vd=+4 V, Quiescent Current Idq=96 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	8.5		12	GHz
Gate Supply Voltage (Vg) (Note 1)		-0.2		V
Gain Small Signal (Pin=-15 dBm)	23	25		dB
Gain Variation Vs Frequency		3.0		dB
Power Output Saturated (Pin=-1 dBm)	18	21	23	dBm
Drain Current Saturated (Pin=-1 dBm)		120	220	mA
Power Added Efficiency (PAE) at Psat		26		%
Input Return Loss (Pin=-15 dBm)		-12		dB
Output Return Loss (Pin=-15 dBm)		-10		dB
DC detector voltage at Pout=20 dBm		0.5		V

Note 1: Typical range of gate voltage is -0.7 to -0.1V to set Idq of 96 mA.

Raytheon reserves the right to update or change specifications without notice.

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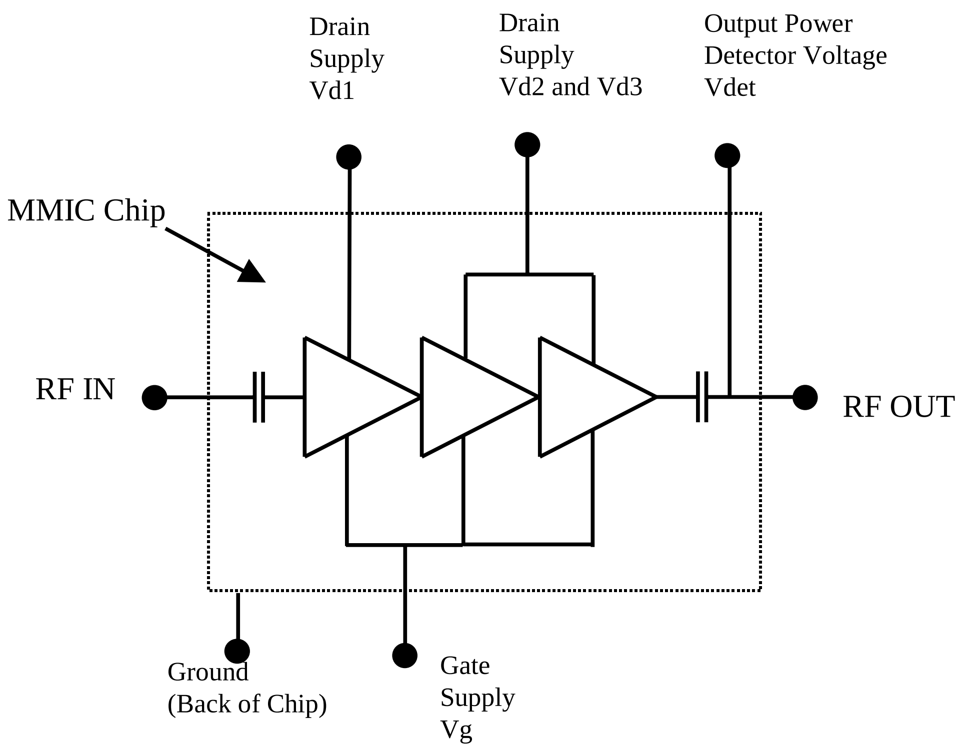
Functional Block Diagram



Note: Detector delivers > 0.1V DC into 3kΩ load resistor for >+20dBm output power.
If output power level detection is not desired, do not connect to detector bond pad.

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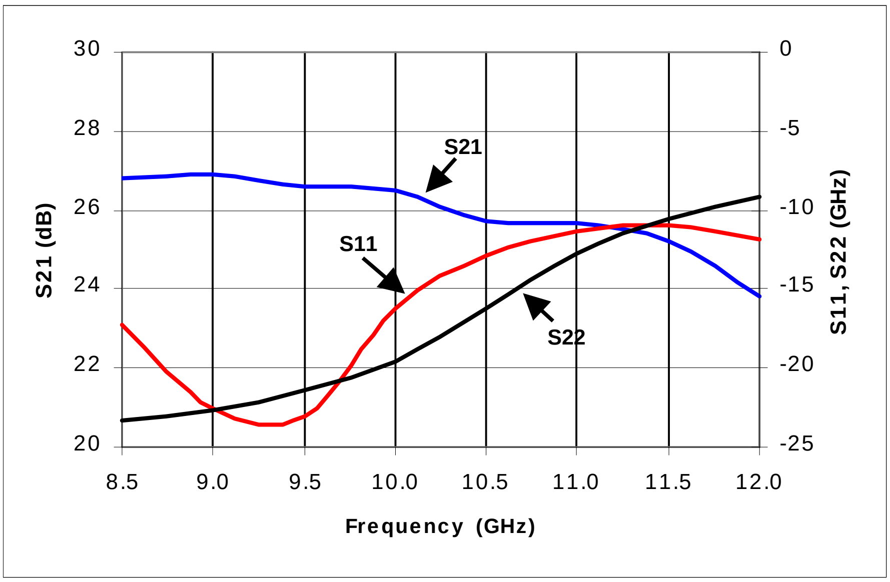
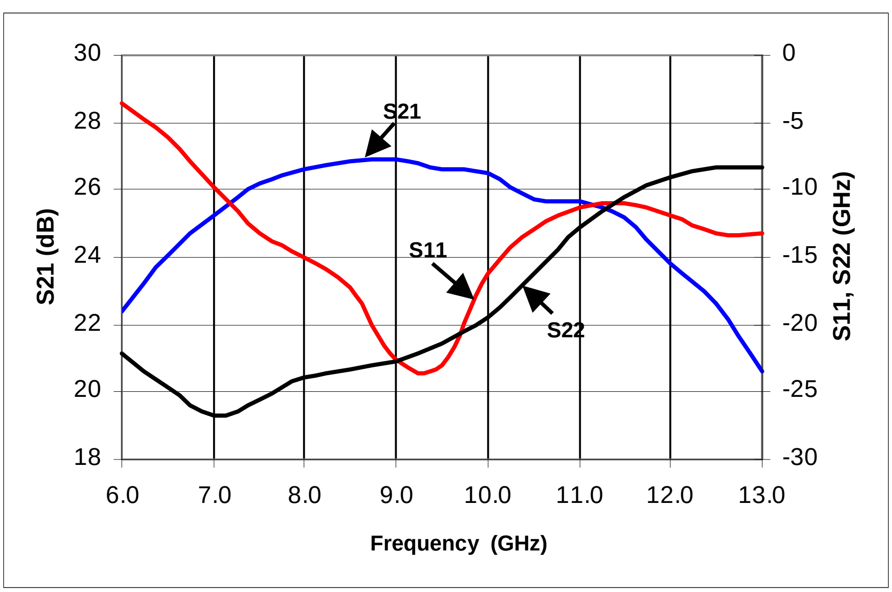
Performance Data

RMWB12001 12 GHz BA, Typical Small Signal Performance
On-Wafer Measurements, Vd=4 V, Idq= 96 mA



RMWB12001 12 GHz BA, Typical Small Signal Performance
On-Wafer Measurements, Vd=4 V, Idq= 96 mA



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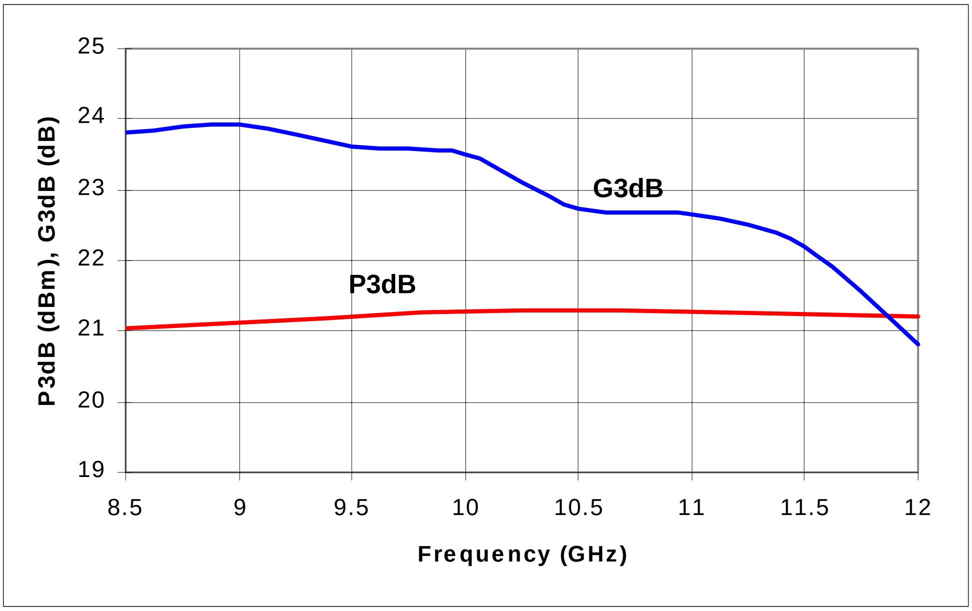
Performance Data

RMWB12001 12 GHz BA,
Power Output and Gain at 3 dB Compression Vs. Frequency and Temperature
On-Wafer Measurements, Vd=4 V, Idq= 96 mA, T=25 °C



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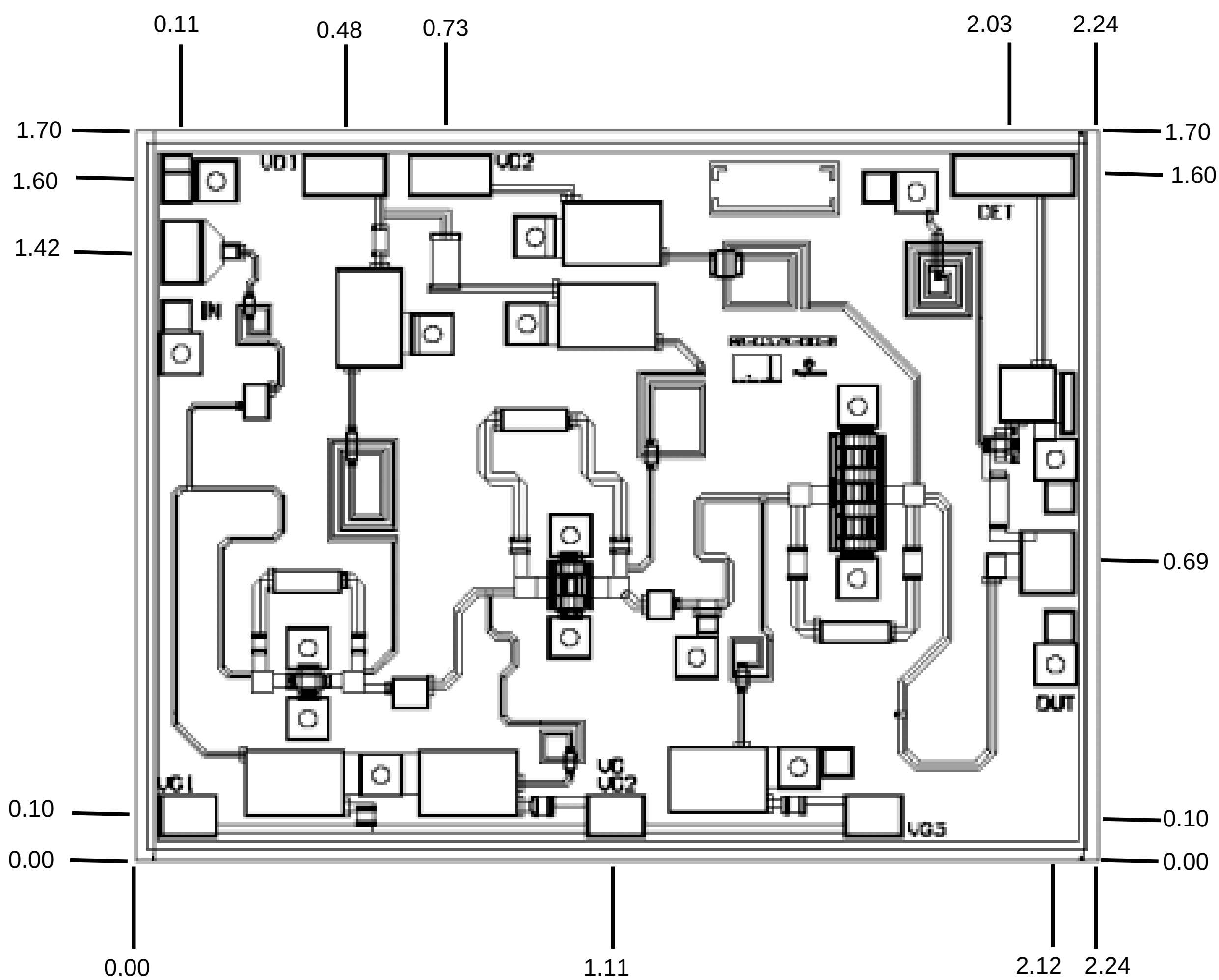
Application Information

Caution: **This is an ESD sensitive device**

Chip Layout and Bond Pad Locations
Chip Size is 2.24 mm x 1.70 mm Typical. Back of chip is RF and DC ground



Dimensions in mm

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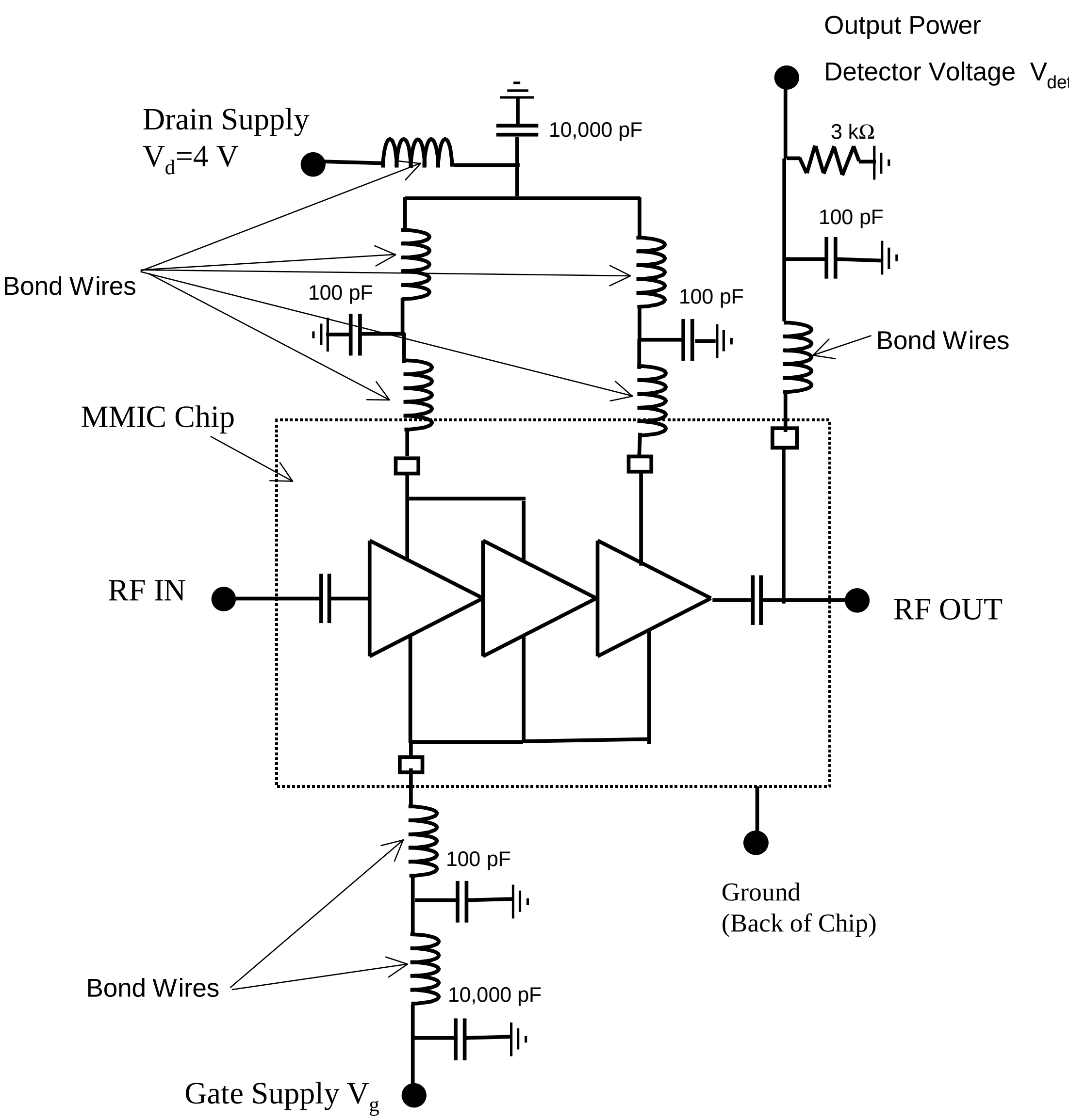
Application Information

Recommended Application Schematic Circuit Diagram



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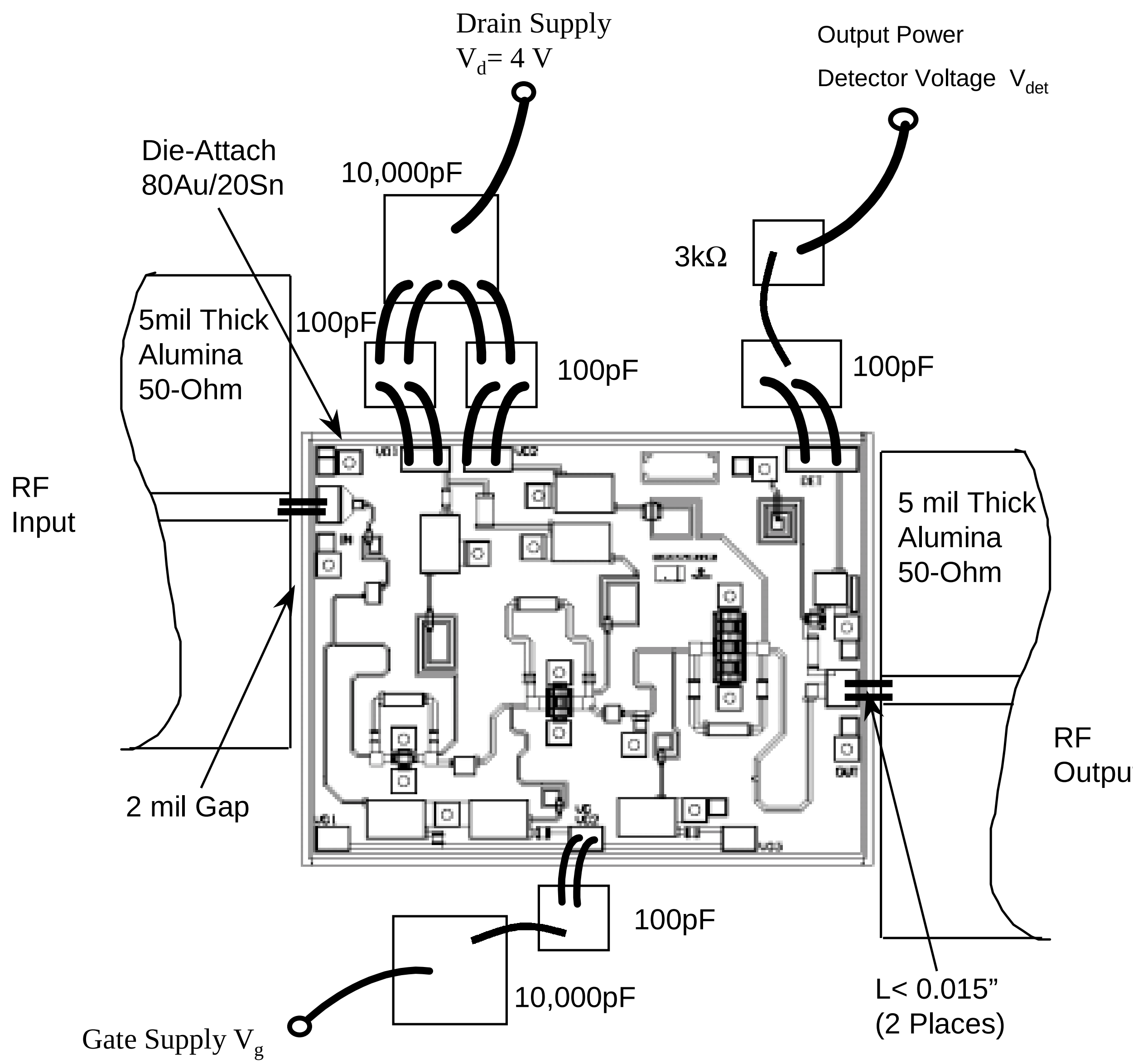
Recommended Assembly Diagram



Note: Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

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CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012” long corresponding to a typically 2 mil between the chip and the substrate material.

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Application Information

Recommended Procedure for Biasing and Operation

Caution: This is an ESD sensitive device

Caution: Loss of gate voltage (Vgs) while drain voltage (Vds) is present may damage the amplifier chip.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier.
Slowly apply negative gate bias supply voltage of -1.5 V to Vgs.

Step 3: Slowly apply positive drain bias supply voltage of +4 V to Vds.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq=96 mA.

Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:
(i) Turn off RF input power, (ii) Turn down and off drain voltage (Vds), (iii) Turn down and off gate bias voltage (Vgs).