RMLA3565-53
Wideband Low Noise MMIC Amplifier

Description

The Raytheon RMLA3565-53 is a single bias wideband low noise MMIC amplifier that meets the following specifications over the 3.5 - 6.5 GHz frequency range. The MMIC requires no external matching circuits and no external gate bias supply. To provide low noise, high linearity, and low current this device uses Raytheon's advanced 0.25 µm PHEMT process.

Features

- 18.0 dB Gain
- 1.35 dB Noise Figure
- Single Positive Bias
- Small Outline Quad Package

Performance Characteristics

Parameter	Min	Typ	Max	Unit
Frequency Range	3.5		6.5	GHz
Gain (Small Signal)	17.0	18.0		dB
Gain Variation vs Temp		-0.013		dB/°C
Noise Figure		1.35	1.9	dB
Input/Output Return Loss		-10.0	-5.0	dB
Power Out, P-1dB	8.0	9.0		dBm
IP3 @ 5.5GHz,-8dBm Out		21.0		dBm
Idd		70.0	90.0	mA
Vdd		4.0	6.0	V
Case Operating Temp	-35		+95	°C
Thermal Resistance		77.5		°C/W

Notes:
Operated at 25 °C and Vdd=4.0V.
25 °C does not apply to "Case Operating Temperature".

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Positive Drain DC Voltage	V_{dd}	6.5	V
RF Input Power (from 50Ω source)	P_{IN}(CW)	0	dBm
Drain Current	I_{dd}	110	mA
Channel Temperature	T_{ch}	175	°C
Operating Case Temperature	T_{Case}	-40 to 100	°C
Storage Temperature Range	$T_{Storage}$	-40 to 110	°C
Soldering Temperature	T_{solder}	220	°C

Characteristic performance data and specifications are subject to change without notice.

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Figure 1. Functional Block Diagram

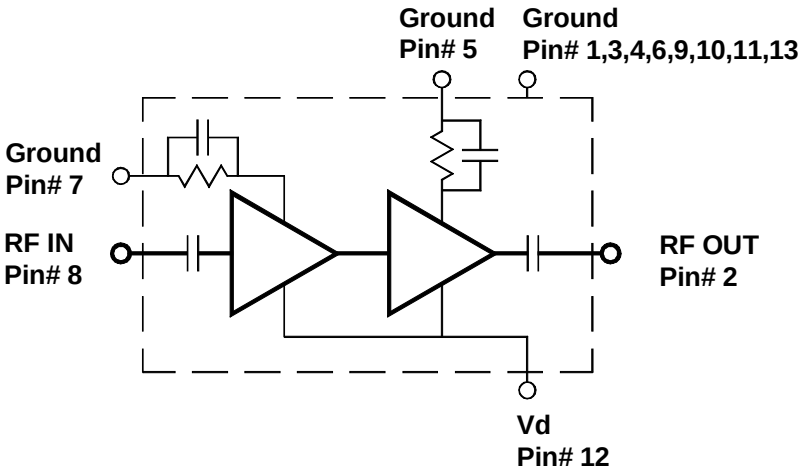
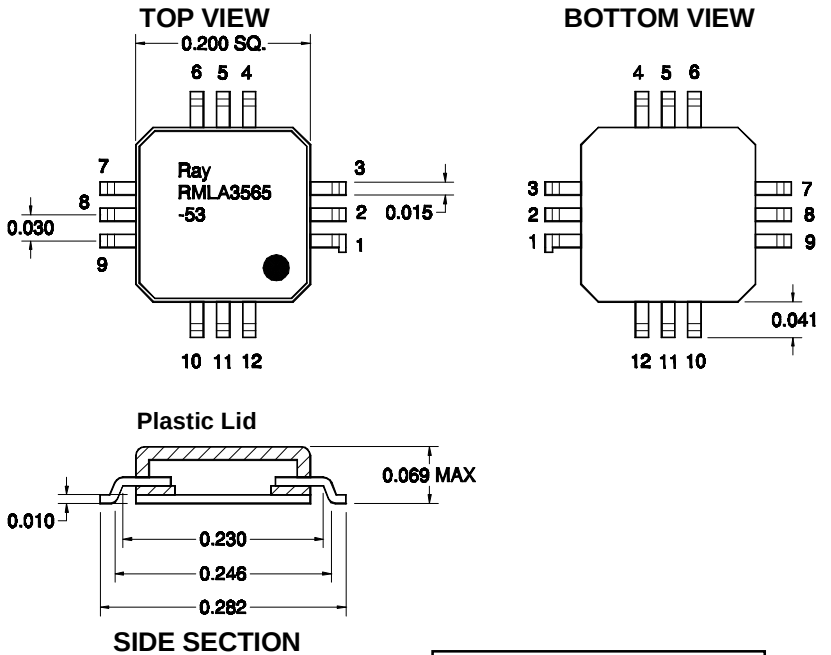


Figure 2. Outline Dimensions



Pin#	Description
1	GND
2	RF Out
3	GND
4	GND
5	GND
6	GND
7	GND
8	RF In
9	GND
10	GND
11	GND
12	Vd
13	GND
	(Package Base)

Dimensions in INCHES

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

The following briefly describes a procedure for evaluating the high efficiency PHEMT amplifier packaged in a surface mount package. It may be noted that the chip is a fully monolithic single ended two stage amplifier for 3.5 to 6.5 GHz applications. Figure 1 shows the functional block diagram of the packaged product.

Test Fixture

Figure 2 shows the outline and pin-out descriptions for the packaged device. A typical test fixture schematic showing external bias components is shown in figure 3. Figure 4 shows typical layout of an evaluation board corresponding to the schematic diagram. A typical performance obtained from the test fixture is shown in figure 5. The following should be noted:

(1) Package pin designations are as shown in figure 2.
(2) Vd is the Drain Voltage (positive) applied at the pins of the package
(3) Vdd is the positive supply voltage at the evaluation board terminal

Test Procedure for the evaluation board (RMLA3565-53-TB)

The following sequence of procedure must be followed to properly test the power amplifier:

Step 1: Turn off RF input power.
Step 2: Use GND terminal of the evaluation board for DC supplies.
Step 3: Apply drain supply voltages of +4.0 V to evaluation board terminals Vdd.
Step 4: After the bias condition is established, RF input signal may now be applied.
Step 5: Follow turn-off sequence of:
(i) Turn off RF Input Power (ii) Turn down and off Vdd

Figure 3. Schematic for a Typical Test Evaluation Board (RMLA3565-53-TB)

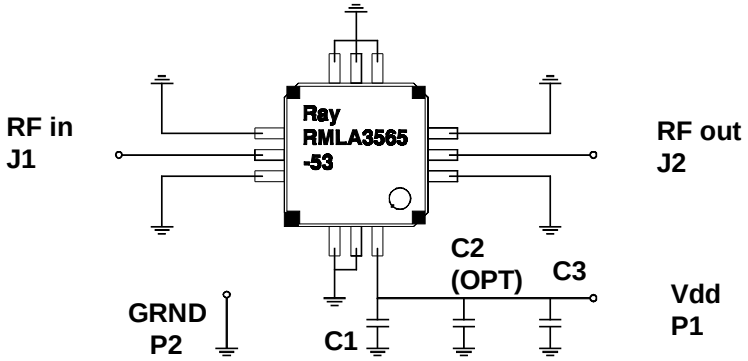

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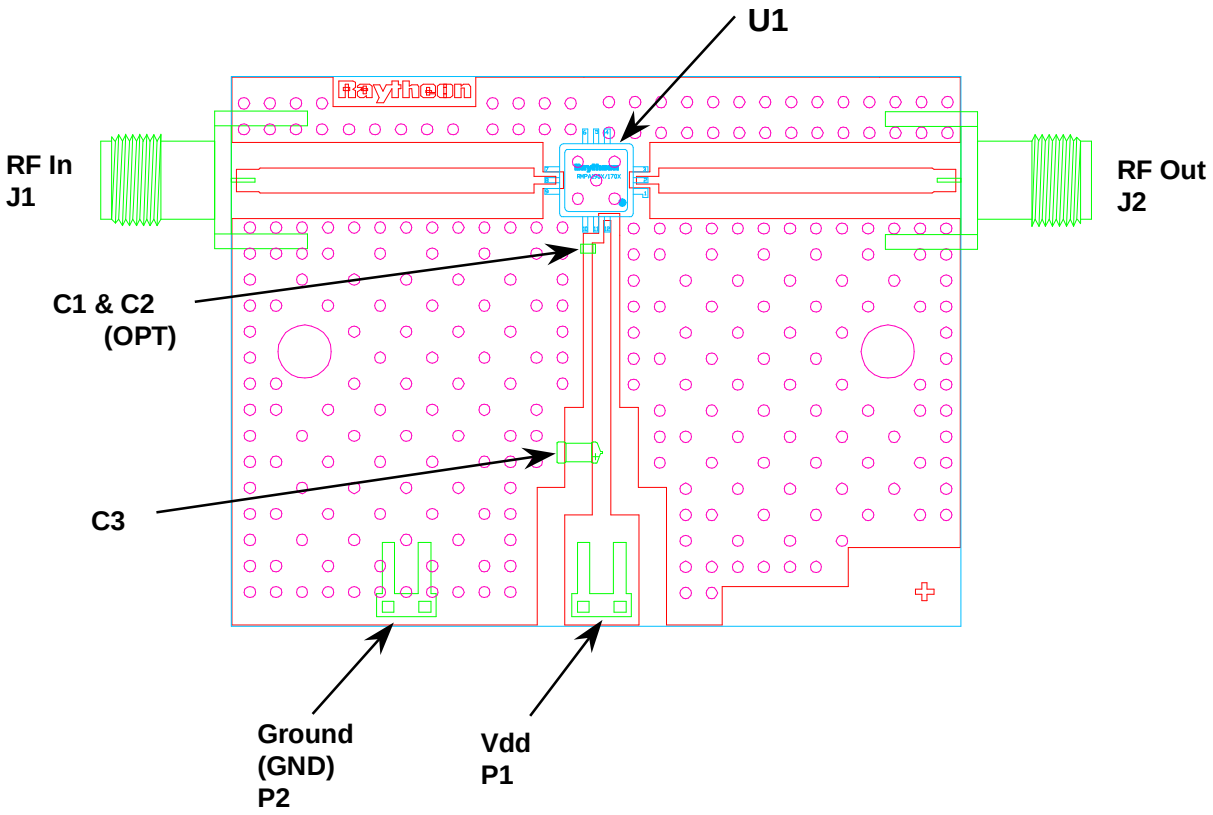
Figure 4. Layout and Assembly of Test Evaluation Board (RMLA3565-53-TB)



PARTS LIST for Test Evaluation Board (RMPA2450-53-TB), (G654220<-change)

PART	VALUE	SIZE(L"xW")	Vendors
C1	330 pF	.04" x .02"	AVX, Murata, Novacap,
C2	1000 pF	.04" x .02"	AVX, Murata, Novacap
C3	4.75 uF	.14"x .11"	Sprague, ATC, AVX, Murata,
U1	RMLA3565-53	.28" x .28" x .07	Raytheon
P1, P2	Terminal		Samtec
J1, J2	SMA Connectors		E.F. Johnson
Board	RO4003(Rogers)	1.99x1.50x.032	Raytheon Dwg# ??????

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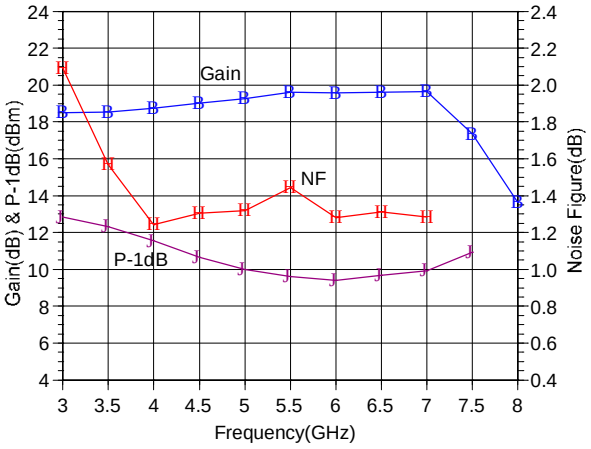
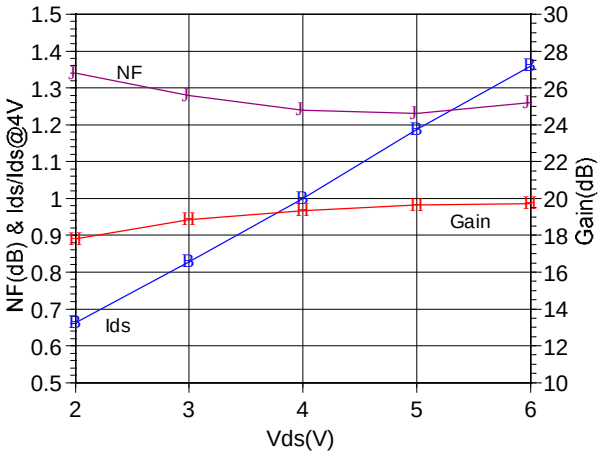
Figure 5. Typical Performance

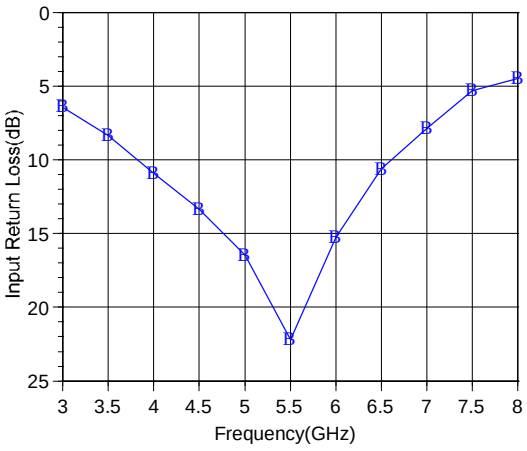
Gain, Power, and Noise Figure
Vds=4.0V, Ids=65.5mA



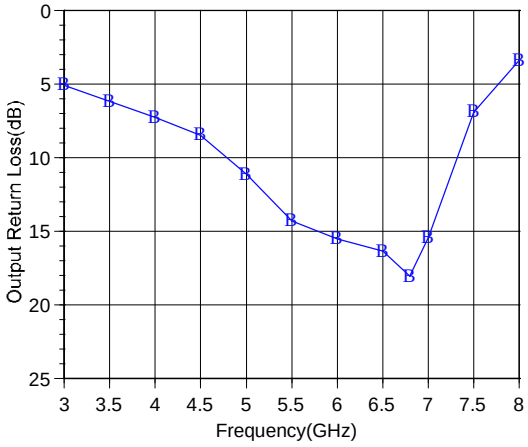
Noise Figure, Gain, & Ids vs. Vds
Frequency = 5.0GHz



Input Return Loss
Vds=4.0V, Ids=65.5mA



Output Return Loss
Vds=4.0V, Ids=65.5mA



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