RC7144

133MHz Spread Spectrum Motherboard Integrated Clock/Buffer

Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- Supports up to 150MHz
- I^2C programmable
- Two copies of CPU clock with one free running
- One copy 24MHz clock
- One copy 48MHz clock
- One copy IOAPIC
- Two copy REF 14.318MHz clock (3.3V)
- Six copies PCI clock
- Thirteen copies of SDRAM clock with one free running
- PCI/CPU stop capability

Description

The RC7144 is a clock synthesizer for motherboard applications. It meets the requirements for the 133MHz 13x/zx chipset. The clock frequencies can be set with the 4 select pins or can be set via the I^2C interface.

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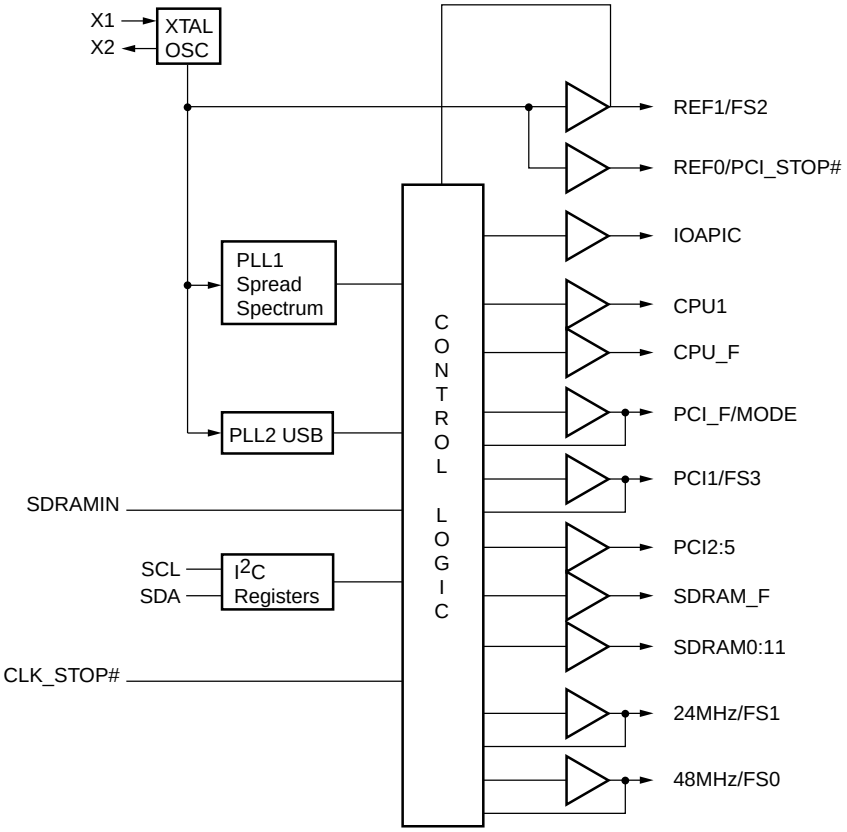
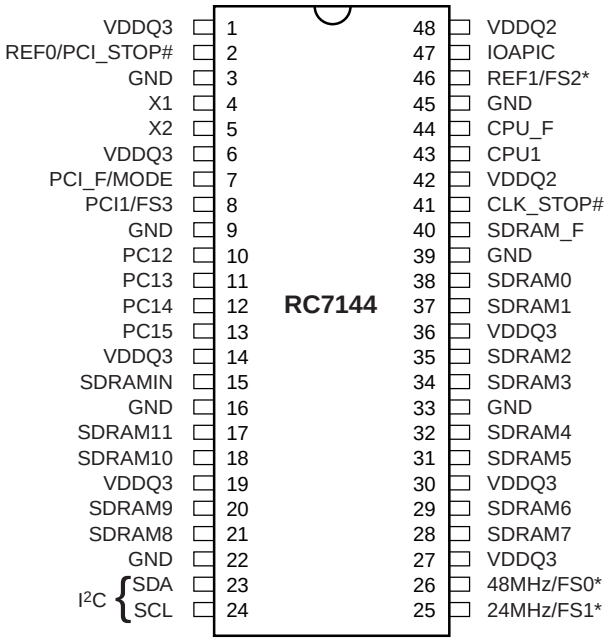
Block Diagram



Preliminary Specification describes products that are not in full production at the time of printing. Specifications are based on design goals and limited characterization. They may change without notice. Contact Fairchild Semiconductor for current information.

Pin Assignments



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Pin Description

Pin Name	Pin #	Pin Type	Pin Function
V_{DDQ3}	1, 6, 14, 19, 27, 30, 36	PWR	**Power connection:** Power supply for core logic, PLL circuitry SDRAM outputs, PCI outputs, reference, 48 & 24 MHz outputs. Connect to 3.3 Volts.
REF0/ PCI_STOP#	2	OUT/IN	**I/O Dual function REF0 & PCI_STOP#:** Function determined by MODE pin. When high, this pin is an output with 14.31818 MHz of reference clock. When MODE is low, PCI_STOP# stops all the PCI clocks.
GND	3, 9, 16, 22, 33, 39, 45	PWR	**Ground connection:** Connect all ground pins to the common system ground plane.
X1	4	IN	**Crystal Connection:** An input connection for an external 14.318 MHz crystal. 18 pF internal cap.
X2	5	OUT	**Crystal Connection or External Reference Frequency:** This pin has dual functions. It can be used as an external 14.318 MHz crystal connection or as an external reference frequency input.
PCI_F/MODE	7	OUT/IN	**Fixed PCI clock output:** Upon power up MODE input will be latched, which will enable or disable REF0.
PCI1/FS3	8	OUT/IN	**PCI clock output:** Upon power up FS3 input will be latched, which will set clock frequencies as frequency selection table. This pin has internal pull down.
PCI2:5	10, 11, 12, 13	OUT	**PCI clock output 2 through 5:** These five PCI clock outputs are controlled by the PCI_STOP# control pin.
SDRAM_IN	15	IN	**Buffered input pin:** The signal provided to this input pin is buffered to 13 outputs.
SDRAM0:11; SDRAM_F	17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38, 40	OUT	**SDRAM Clock Ouputs:** SDRAM0:11 clock are determined by FS0: FS3. SDRAM_F is a free running clock which is not controlled by the I^2C.
SDA	23	IN/OUT	Data pin for I^2C circuitry.
SCL	24	IN	Clock pin for I^2C circuitry.
24MHz/FS1	25	OUT/IN	**24 MHz clock output:** 24 MHz is provided in normal operation. In standard systems, this output can be used as the clock input for Super I/O chip. Upon power up FS1 input will be latched, which will set clock frequencies as frequency selection table.
48MHz/FS0	26	OUT/IN	**48 MHz clock output:** 48 MHz is provided in normal operation. In standard systems, this output can be used as the reference for universal Serial Bus. Upon power up FS0 input will be latched, which will set clock frequencies as frequency selection table.
CLK_STOP#	41	IN	**CLK_STOP# Input:** When 0, this pin stops the CPU outputs after completing a full clock cycle. This pin does not effect CPU_F.
V_{DDQ2}	42, 48	PWR	Power supply for IOAPIC & all CPU outputs. Connect to 2.5 or 3.3 Volts.
CPU1, CPU_F	43, 44	OUT	**CPU output clocks:** V_{DDQ2} controls output Voltage. Stopped when CLK_STOP# is 0. CPU_F is not affected by CLK_STOP#.
REF1/FS2	46	OUT/IN	**Reference Clock output:** 14.31818 MHz reference output. Upon power up FS2 input will be latched, which will set clock frequencies as frequency selection table.
IOAPIC	47	OUT	**IOAPIC clock:** Provides 14.31818 MHz fixed clock. V_{DDQ2} contols the output Voltage.

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Frequency Selection Table

Input Address				CPU (MHz)	PCI (MHz)
FS3	FS2	FS1	FS0		
1	1	1	1	133.3	33.3
1	1	1	0	124	31
1	1	0	1	150	37.5
1	1	0	0	140	35
1	0	1	1	105	35
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	40
0	1	1	1	100	33.3
0	1	1	0	133.3	44.43
0	1	0	1	112	37.3
0	1	0	0	103	34.3
0	0	1	1	66.8	33.4
0	0	1	0	83.3	41.7
0	0	0	1	75	37.5
0	0	0	0	124	41.3

Power Management Control

Mode	PCI_STOP#	PCI	REF0	PCI_F
0	0	Stopped	Disable	Running
0	1	Running	Disable	Running
1	X	Running	Running	Running

CLK_STOP#	CPU	CPU_F	REF1, 24/48MHZ, SDRAM 0:11
0	Stopped	Running	Running
1	Running	Running	Running

Functional Description

I/O Pin Operation

Dual Purpose I/O pins such as pin 8 FS3/PCI1, act as a logic input upon power up. This allows the determination of assigned device function. For example, FS3 along with the other three select pins will determine the clock frequencies as shown in the table. A short time after power up, the logic state is latched and the pin becomes a clock output pin. For example, pin 8 becomes a PCI clock output. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm “strapping” resistor is connected between the I/O pin and VDD or VSS (ground). A connection to ground sets a “0” bit and a connection to VDD sets a “1” bit. See Figure 1.

Upon power up, the first 2mS of operation is used for input logic selection. The clock output pins are tri-stated, allowing the output strapping resistor on the I/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2mS period, the established logic “0” or “1” condition of the I/O pin is then latched. Next the output buffer is enabled which converts the I/O pin into an operating clock output. The 2mS timer is started when VDD (3.3V) reaches 2.0V. The input bits can only be reset by turning the VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of outputs is 20 ohms (nominal) which is minimally affected by the 10kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the I/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

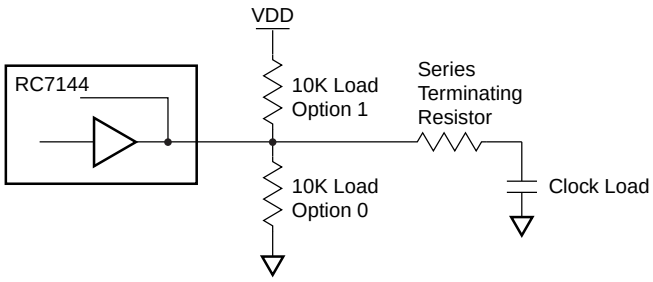

Figure 1. Input Logic Selection through Resistor Load Option

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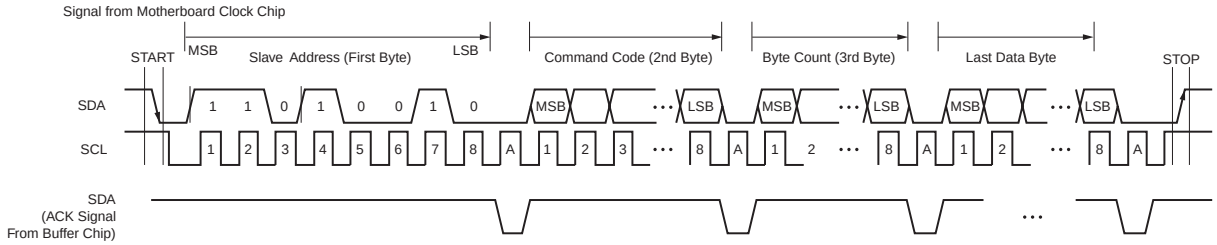
I²C Interface Information

The RC7144 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7144 initializes with default register settings therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDA and SCL. In motherboard applications, SDA and SCL are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 1 summarizes the control functions of the serial data interface.

Table 1. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections other than the 100MHz provided upon power-on. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Spread Spectrum Enabling	Turns spread spectrum on or off.	EMI reduction.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock ouputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 6.	Production PCB testing.
Reserved	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

RC7144 I²C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDA at every 8th bit. The 8 bit data from SDA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

I²C Register Operation

The RC7144 is programmed by writing 10 bytes of eight bits each. See Table 2 for byte order.

Table 2. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7144 to accept the bits in Data Bytes 0-6 or internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7144 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don't Care	Unused by the RC7144, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7144, therefore, bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Refer to Table 3	The data bits in these bytes set internal RC7144 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3		
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

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Writing Data Bytes

Each bit of the 8 data bytes controls a particular device function except for the “reserved bits”. These must be preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 3 for bit descriptions of Data Bytes 1-4.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 4 shows the mode select for byte 0, Bit 1and 0.

Table 3. Data Bytes 0–7 Serial Configuration Map

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 0						
7	-	-	Spread Mode	Center	Down	0
6	-	-	FS 2	-	-	0
5	-	-	FS 1	-	-	0
4	-	-	FS 0	-	-	0
3	-	-	Hardware/Software Frequency Select	Hardware	Software	0
2	-	-	FS3	-	-	0
1–0	-	-	Bit 1 Bit 0 Function (see Table 4) 0 0 Normal Operation 0 1 Reserved 1 0 Spread Spectrum on 1 0 All Outputs Tristated			00
Data Byte 1						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Test Mode	Test Mode	Normal	1
3	40	SDRAM_F	Clock Output Disabled	Low	Active	1
2	-	-	Reserved	-	-	0
1	43	CPU1	Clock Output Disabled	Low	Active	1
0	44	CPU_F	Clock Output Disabled	Low	Active	1
Data Byte 2						
7	-	-	Reserved	-	-	0
6	7	PCI_F	Clock Output Disabled	Low	Active	1
5	-		Reserved	-	-	0
4	13	PCI5	Clock Output Disabled	Low	Active	1
3	12	PCI4	Clock Output Disabled	Low	Active	1
2	11	PCI3	Clock Output Disabled	Low	Active	1
1	10	PCI2	Clock Output Disabled	Low	Active	1
0	8	PCI1	Clock Output Disabled	Low	Active	1
Data Byte 3						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	26	48 MHz	Clock Output Disabled	Low	Active	1
4	25	24MHz	Clock Output Disabled	Low	Active	1
3	-	-	Reserved	-	-	0

Table 3. Data Bytes 0–7 Serial Configuration Map (Continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
2	21, 20, 18, 17	SDRAM8:11	Clock Output Disabled	Low	Active	1
1	32, 31, 29, 28	SDRAM4:7	Clock Output Disabled	Low	Active	1
0	38, 37, 35, 34	SDRAM0:3	Clock Output Disabled	Low	Active	1
Data Byte 4						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0
Data Byte 5						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	47	IOAPIC	Clock Output Disabled	Low	Active	1
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	46	REF1	Clock Output Disabled	Low	Active	1
0	2	REF0	Clock Output Disabled	Low	Active	1
Data Byte 6						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0
Data Byte 7						
7	-	-	Reserved	-	-	0
6	-	-	Reserved	-	-	0
5	-	-	Reserved	-	-	0
4	-	-	Reserved	-	-	0
3	-	-	Reserved	-	-	0
2	-	-	Reserved	-	-	0
1	-	-	Reserved	-	-	0
0	-	-	Reserved	-	-	0

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Table 4. Select Function for Data Byte 0, Bits 0:1

Function	Input Conditions		Output Conditons				
	Data Byte 0						
	Bit 1	Bit 0	CPU	PC1	IOAPIC REF0:1	48 MHz	24 MHz
Normal Operation	0	0	NOTE 1	NOTE 1	14.318 M	48 M	24 M
Spread Spectrum	1	0	±0.5%	±0.5%	14.318 M	48 M	24 M
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Table 5. Frequency Selection Table Through I^2C Programming

Input Conditons					
Data Byte 0, Bit 3 = 1					
Bit 2 FS3	Bit 6 FS2	Bit 5 FS1	Bit 4 FS0	CPU (MHz)	PCI (MHz)
1	1	1	1	133.3	33.3
1	1	1	0	124	31
1	1	0	1	150	37.5
1	1	0	0	140	35
1	0	1	1	105	35
1	0	1	0	110	36.7
1	0	0	1	115	38.3
1	0	0	0	120	40
0	1	1	1	100	33.3
0	1	1	0	133.3	44.43
0	1	0	1	112	37.3
0	1	0	0	103	34.3
0	0	1	1	66.8	33.4
0	0	1	0	83.3	41.7
0	0	0	1	75	37.5
0	0	0	0	124	41.3

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Table 6. Test Mode

Function	Input Condition Data Byte4	CPU	PCI	REF, IOAPIC	48MHz	24MHz
Normal	1	Note 1	Note 1	14.318	48	24
Test Mode	0	X1	CPU/2 or 3	X1	X1/2	X1/4

Note:
1. See table 5 for frequency selection.

Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to ground	-0.5 to 7.0	V
T_{STG}	Storage Temperature	-65 to 150	^{o}C
T_B	Ambient Temperature	-55 to 125	^{o}C
T_A	Operating Temperature	0 to 70	^{o}C
ESD_{PROT}	Input ESD Protection	2 (min)	kV

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Electrical Characteristics—Common Parameters

T_A = 0°C to 70°C; Supply Voltage 3.3V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		V_{SS}-0.3		0.8	V
V_{IH}	Input High Voltage		2.0		V_{DD}+0.3	V
I_{IL}	Input Low Current	V_{IN}=0; inputs with no pull-up resistors	-5		5	µA
		V_{IN}=0; inputs with pull-up resistors			-25	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-5		-5	µA
C_{IN}	Input Capacitance[1]	All except X1 and X2.			5	pF
		X1 and X2 Pins. X2 unconnected.		18		pF
C_{OUT}	Output Capacitance[1]				6	pF
LIN	Input Pin Inductance[1]				7	nH
V_{TH}	Crystal Input Threshold[1]	V_{DD}=3.3V		1.5		V
I_{DD}	Supply Current	Freq=100M: C_L max. on all outputs		300		mA
I_{DDL}		V_{DD}=2.5V 0.5%; Freq-100M		24		mA
T_{STAB}	Clock Stabilization[1]	From V_{DD}=3.3V to 1% Target			3	mS
$T_{CPU-PCI}$	Skew[1]	V_{DDL}=2.5V; V_{DD}=3.3V; CPU V_{TH}=1.25V, PCI V_{TH}=1.5V	1.5		4	nS

Note:

1. Guaranteed by design, not subject to 100% production testing.

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Electrical Characteristics—CPU Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.0			V
I_{OL}	Output Low Current	V_{OL}=1.2 V	27		93	mA
I_{OH}	Output High Currents	V_{OH}=1.2 V	-101		-25	mA
T_R	Rise Time[1]	0.4 to 2.0 V: C_L=20 pF	0.4		1.6	nS
T_F	Fall Time[1]	2.0 to 0.4 V; C_L=20 pF	0.4		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.25 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.25 V; C_L=20 pF			200	pS
T_{SK}	Skew[1]	V_{TH}=1.25 V; C_L=20 pF			175	pS
Z_O	AC Output Impedance[1]			20		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—IOAPIC Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.0			V
I_{OL}	Output Low Current	V_{OL}=1.25 V	27		93	mA
I_{OH}	Output High Currents	V_{OH}=1.2 V	-101		-25	mA
T_R	Rise Time[1]	0.4 to 2.0 V: C_L=20 pF	0.4		1.6	nS
T_F	Fall Time[1]	2.0 to 0.4 V; C_L=20 pF	0.4		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.25 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.25 V; C_L=20 pF			500	pS
Z_O	AC Output Impedance[1]			15		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

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Electrical Characteristics—PCI Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	26		139	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-189		-31	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=30 pF	0.5		2.0	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=30 pF	0.5		2.0	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=30 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
T_{SK}	Skew[1]	V_{TH}=1.5 V; C_L=30 pF			500	pS
Z_O	AC Output Impedance[1]			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—REF Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	25		76	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-94		-27	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=20 pF	1		4	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=20 pF	1		4	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=20 pF	45		55	%
T_{JIT}	Jitter (Cycle-cycle)[1]	V_{TH}=1.5 V; C_L=20 pF			500	pS
Z_O	AC Output Impedance[1]			30		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

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Electrical Characteristics—48/24 MHz Outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=1.5 V	25		76	mA
I_{OH}	Output High Currents	V_{OH}=1.5 V	-94		-27	mA
F_{ACCU}	Frequency Accuracy[1]				167	ppm
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=20 pF	1		4.0	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=20 pF	1		4.0	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=20 pF	45		55	%
Z_O	AC Output Impedance[1]			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Electrical Characteristics—SDRAM outputs

T_A=0°C to 70°C; Supply Voltage V_{DD}=3.3V±5%; V_{DDL}=2.5V±5% (unless otherwise stated)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OL}	Output Low Voltage	I_{OL}=1 mA			0.5	V
V_{OH}	Output High Voltage	I_{OH}=-1 mA	2.4			V
I_{OL}	Output Low Current	V_{OL}=0.4 V	53			mA
I_{OH}	Output High Currents	V_{OH}=2.0 V			-54	mA
T_R	Rise Time[1]	0.4 to 2.4 V: C_L=30 pF	0.5		1.6	nS
T_F	Fall Time[1]	2.4 to 0.4 V; C_L=30 pF	0.5		1.6	nS
D_T	Duty Cycle[1]	V_{TH}=1.5 V; C_L=30 pF	45		55	%
T_{JIT}	Jitter (Cycle to Cycle)[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
T_{SK}	Skew[1]	V_{TH}=1.5 V; C_L=30 pF			250	pS
Z_O	AC Output Impedance[1]			40		Ω

Note:

1. Guaranteed by design, not subject to 100% production testing.

Preliminary Information

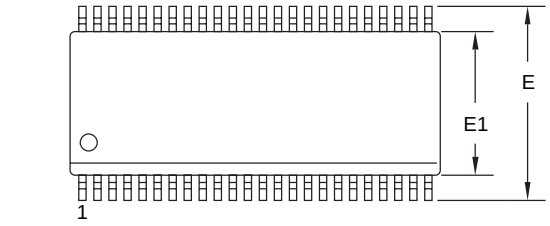
Mechanical Dimensions

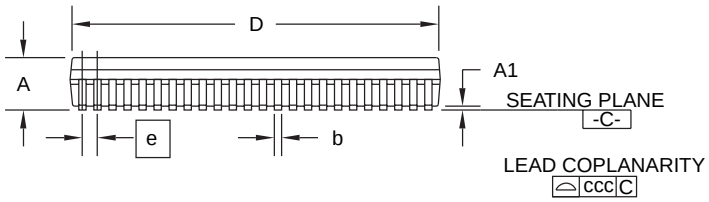
48 pin SSOP

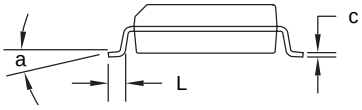
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.095	.110	2.41	2.79	
A1	.008	.016	0.20	0.41	
b	.008	.0135	0.20	0.34	5
c	.005	.010	0.13	0.25	5
D	.620	.630	15.75	16.00	2, 4
E	.395	.420	10.03	10.67	
E1	.291	.299	7.39	7.59	2
e	.025 BSC		0.64 BSC		
L	.020	.040	0.51	1.02	3
N	48		48		6
a	0°	8°	0°	8°	
ccc	---	.004	---	0.13	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC7144	48 pin SSOP

Preliminary Information

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