RT54SX-S
RadTolerant FPGAs for Space Applications

Special Features for Space

- First Actel FPGA Designed Specifically for Space Applications
- Up to 2,012 Additional SEU Hardened Flip-Flops Eliminate Software TMR Necessity (LETth > 40, GEO SEU Rate < 10^{-10} upset/bit-day)
- Up to 100krad (Si) Total Ionizing Dose (TID) Parametric Performance Supported with Lot-Specific Test Data
- Single Event Latch-Up Immune
- Flexible I/O Accommodates 2.5V, 3.3V, and 5.0V Input Signals
- Pin Compatibility Allows Prototyping with Commercial SX-A FPGAs, and Mission Implementation with Radiation-Tolerant RT54SX-S
- Deterministic Power-Up
- No Sequencing Required for Supply Voltages at Power-Up
- Cold Sparing Capability
- Devices Available from TM1019.5-tested Pedigreed Lots
- 5.0V CMOS Input Trip Point Option

Standard Features

- Very Low Power Consumption (Up to 68 mW at Standby)
- Configurable I/O Support for 3.3V/5.0V PCI, LVTTL, TTL Levels, and CMOS
- 2.5V, 3.3V, and 5.0V Mixed Voltage Operation
- 5.0V Input Tolerance and 5.0V Drive Strength
- Hot-Swapping Capability
- QML Certified Devices
- Secure Programming Technology Prevents Reverse Engineering and Design Theft
- Configurable Weak Resistor Pull-up or Pull-down for Tristated Outputs at Power-Up
- 100% Circuit Resource Utilization with 100% Pin Locking
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Dedicated JTAG Reset (TRST) Pin
- Deterministic, User-Controllable Timing
- JTAG Boundary Scan Testing In Compliance with IEEE Standard 1149.1
- CMOS Latch-Up Immunity
- 0.25µm Metal-to-Metal Antifuse Process Generation

Leading Edge Performance

- 250 MHz System Performance
- 8.9 ns Clock-to-Out (Pin-to-Pin)
- 310 MHz Internal Performance

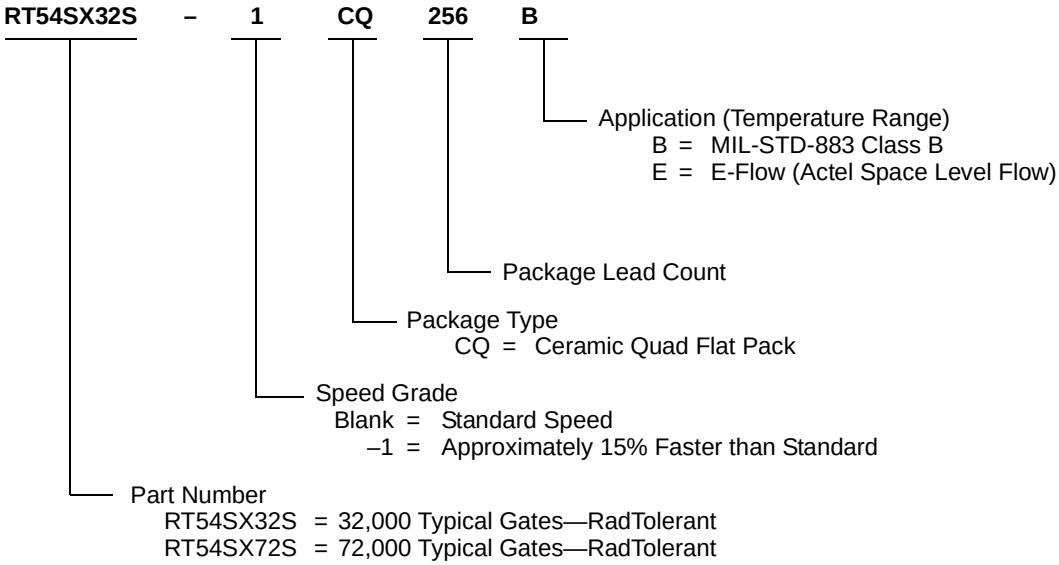
Specifications

- 48,000 to 108,000 Available System Gates
- Up to 360 User-Programmable I/O Pins (package dependent)

RT54SX-S Product Profile

Device	RT54SX32S	RT54SX72S
Capacity		
Typical Gates	32,000	72,000
System Gates	48,000	108,000
Logic Modules	2.880	6,036
Combinatorial Cells	1,800	4,024
SEU Hardened Register Cells (Dedicated Flip-Flops)	1,080	2,012
Maximum Flip-Flops	1,980	4,024
Maximum User I/Os	227	212
Clocks	3	3
Quadrant Clocks	0	4
Clock-to-Out	8.9 ns	11.0 ns
Input Set-Up (External)	–1.3 ns	–3.3 ns
Speed Grades	Std, –1	Std, –1
Package (by pin count)		
CQFP	208, 256	208, 256

Ordering Information



Product Plan G15

	Speed Grade		Application	
	Std	–1*	B	E
RT54SX32S Devices				
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P
RT54SX72S Devices				
208-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P
256-Pin Ceramic Quad Flat Pack (CQFP)	P	P	P	P

Contact your Actel sales representative for product availability.

*Applications: B = MIL-STD-883 Class B Availability: P = Planned * Speed Grade: –1 = Approx. 15% Faster than Standard*
E = E-flow (Actel Space Level Flow)

Ceramic Device Resources

Device	User I/Os (including clock buffers)	
	CQFP 208-Pin	CQFP 256-Pin
RT54SX32S	173	227
RT54SX72S	170	212

Package Definitions *(Contact your Actel sales representative for product availability.)*
CQFP = Ceramic Quad Flat Pack

Radiation Survivability

The RadTolerant SX-S devices have varying total dose radiation survivability. The ability of these devices to survive radiation effects is both device and lot dependent. The user must evaluate and determine the applicability of these devices to their specific design and environmental requirements.

Total dose results are summarized in two ways. The first summary is indicated by the maximum total dose level achieved before the device fails to meet an individual performance specification, but remains functional. For Actel FPGAs, the parameter that first exceeds the specification is I_{CC} (standby supply current). The second summary is indicated by the maximum total dose achieved prior to the functional failure of the device.

Actel provides total dose radiation test data on each pedigreed lot offered for sale. Reports are available on our website or from Actel's local sales representative. Listings of available lots and devices can also be provided.

For a radiation performance summary, see *Radiation Performance of Actel Products* at http://www.actel.com/hirel. This summary also shows single event upset (SEU) and single event latch-up (SEL) testing that has been performed on Actel FPGAs.

All radiation performance information is provided for information purposes only and is not guaranteed. Total dose effects are lot-dependent, and Actel does not guarantee that future devices will continue to exhibit similar radiation characteristics. In addition, actual performance can vary widely due to a variety of factors, including but not limited to, characteristics of the orbit, radiation environment, proximity to the satellite exterior, the amount of inherent shielding from other sources within the satellite and actual bare die variations. For these reasons, it is solely the responsibility of the user to determine whether the device will meet the requirements of the specific design.

QML Certification

Actel has achieved full QML certification demonstrating that quality management procedures, processes, and controls are in place and comply with MIL-PRF-38535, the performance specification used by the Department of Defense for monolithic integrated circuits. QML certification is a good example of Actel's commitment to supplying the highest quality products for all types of high-reliability, military, and space applications.

Many suppliers of microelectronics components have implemented QML as their primary worldwide business system. Appropriate use of this system not only helps in the implementation of advanced technologies, but also allows for high quality, reliable, and cost-effective logistics support throughout QML products' life cycles.

RT54SX-S—A New Design for Space Applications

The architecture of the RT54SX-S devices is an enhanced version of Actel's SX-A device architecture. For more information about the SX-A device architecture, see the "Background on the Family Architecture" section on page 5.

Featuring SEU hardened D-flip-flops that offer the benefits of Triple Module Redundancy (TMR), the RT54SX-S family is a unique product offering for space applications. The RT54SX-S devices are manufactured using a 0.25µm technology at the Matsushita (MEC) facility in Japan. These devices offer levels of radiation survivability far in excess of typical CMOS devices.

SEU Hardened DFF Description

In order to meet the stringent SEU requirements of a LETth greater than 40MeV-gm/cm^2, the internal design of the R-cell was modified without changing the functionality of the cell. Figure 1 shows basic R-cell functionality.

A simplified representation of how the D-flip-flop in the R-cell is implemented in the SX-A architecture is shown in Figure 2. The flip-flop consists of a master and a slave latch gated by opposite edges of the clock. Each latch is constructed by feeding back the output to the input stage. The potential problem in a space environment is that either of the latches can change state when hit by a particle with enough energy.

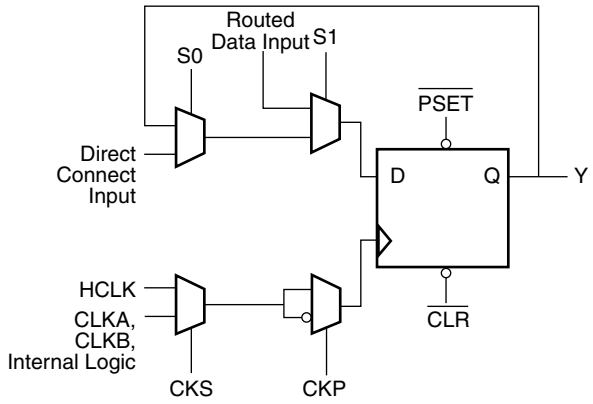


Figure 1 • R-Cell

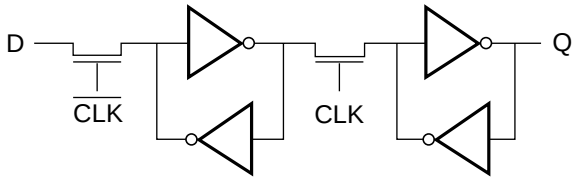


Figure 2 • R-Cell Implementation: RT54SX-S

To achieve the SEU requirements the D-flip-flop in the RT54SX-S R-cell is enhanced (Figure 3). Both the master and the slave latches are implemented with three latches. The feedback path of each of the three latches is voted with the outputs of the other two latches. If one of the three latches is struck by an ion and starts to change state, the voting with the other two latches prevents the change from feeding back and permanently latching. Care was taken in the layout to ensure that a single ion strike could not affect more than one latch.

Figure 4 is a simplified schematic of the test circuitry that has been added to test the functionality of all the components of the flip-flop. The inputs to each of the three latches are independently controllable so the voting circuitry in the feedback paths can be exhaustively tested. This testing is performed on an unprogrammed array during wafer sort, final test and post burn-in test. This test circuitry cannot be used to test the flip-flops once the device has been programmed.

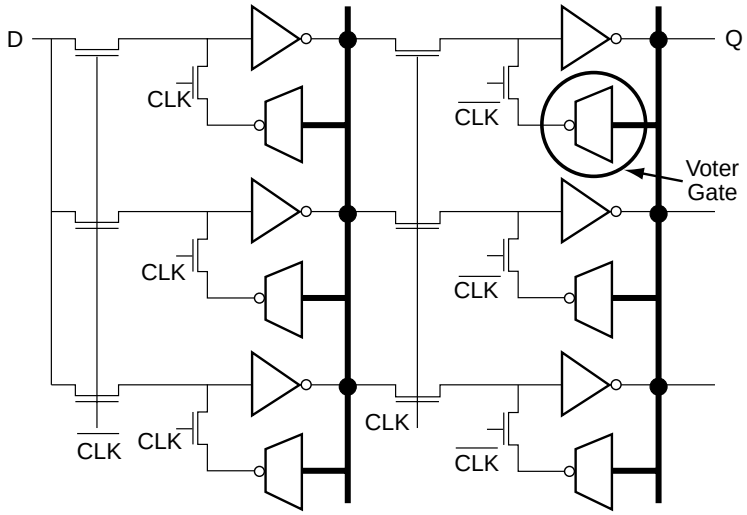


Figure 3 • *R-Cell Implementation—Voter Gate: RT54SX-S*

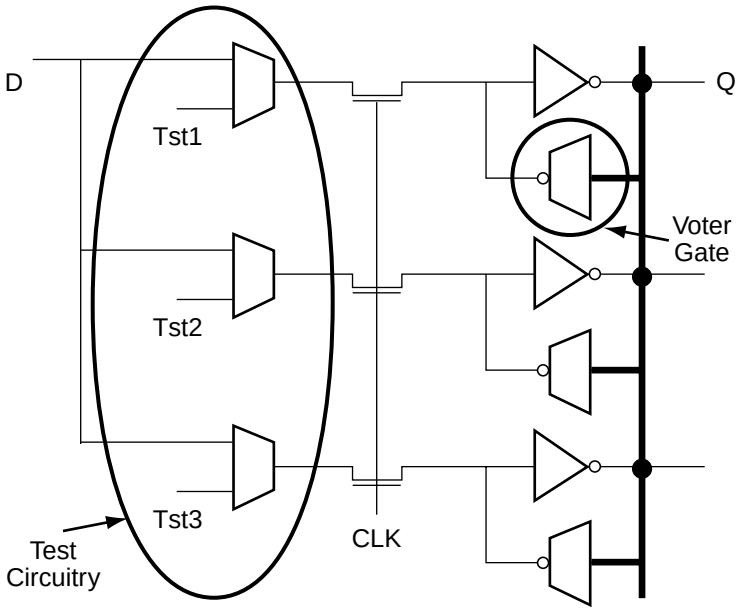


Figure 4 • *R-Cell Implementation—Voter Gate and Test Circuitry*

Background on the Family Architecture

The RT54SX-S architecture was designed to satisfy next-generation performance and integration requirements for production-volume designs in a broad range of high reliability applications.

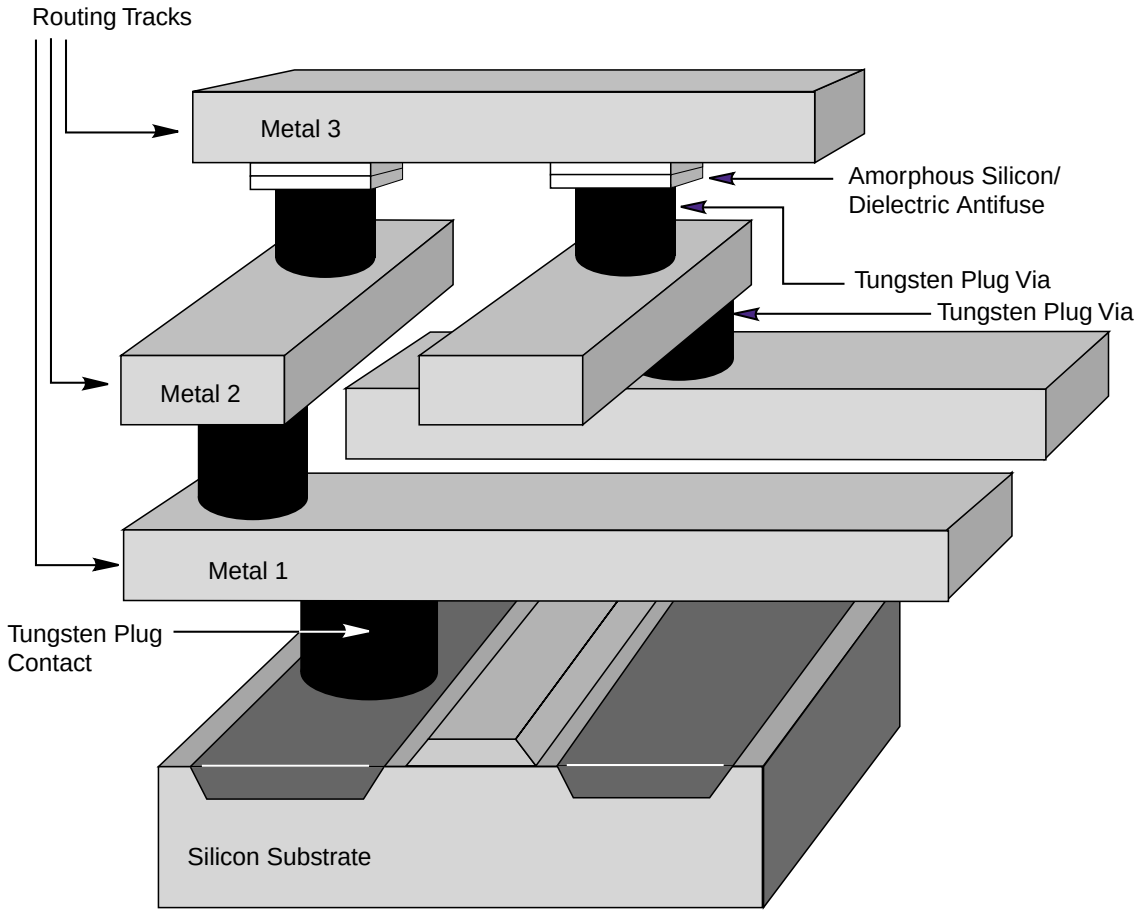
Programmable Interconnect Element

The RT54SX-S family incorporates up to four layers of metal interconnect, and provides much more efficient use of silicon by locating the routing interconnect resources between the Metal 2 (M2) and Metal 3 (M3) layers (see Figure 5). This completely eliminates the channels of routing and interconnect resources between logic modules (as implemented on SRAM FPGAs and previous generations of antifuse FPGAs), and enables the entire floor of the device to be spanned with an uninterrupted grid of logic modules.

Interconnection between these logic modules is achieved using Actel's patented metal-to-metal programmable antifuse interconnect elements, which are embedded between the top two metal layers. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection.

The extremely small size of these interconnect elements provides the RT54SX-S family abundant routing resources and additionally excellent protection against design theft. Reverse engineering is virtually impossible as a result of the extreme difficulty to distinguish between programmed and unprogrammed antifuses. Additionally, there is no configuration bitstream to intercept.

The RT54SX-S interconnect (i.e., the antifuses and metal tracks) also has lower capacitance and lower resistance than any other device of similar capacity, leading to the fastest signal propagation in the industry for the radiation tolerance offered.



Note: RT54SX32S has the antifuse between the top two layers of metal. The RT54SX72S has four layers of metal.

Figure 5 • *RT54SX-S Family Interconnect Elements*

Logic Module Desigsn

The RT54SX-S family architecture has been called a "sea-of-modules" architecture because the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Actel's RT54SX-S family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 2 on page 3). The R-cell registers feature programmable clock polarity, selectable on a register-by-register basis. This provides the designer with additional flexibility while allowing mapping of synthesized functions into the RT54SX-S FPGA. The clock source for the R-cell can be chosen from the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to 5-inputs (Figure 6). Inclusion of the DB input and its associated inverter function dramatically increases the number of combinatorial functions that can be implemented in a single module from 800 options in previous architectures to more than 4,000 in the SX-A architecture. An example of the improved flexibility enabled by the inversion capability is the ability to integrate a 3-input exclusive-OR function into a single C-cell. At the same time, the C-cell structure is extremely synthesis-friendly, simplifying the overall design and reducing synthesis time.

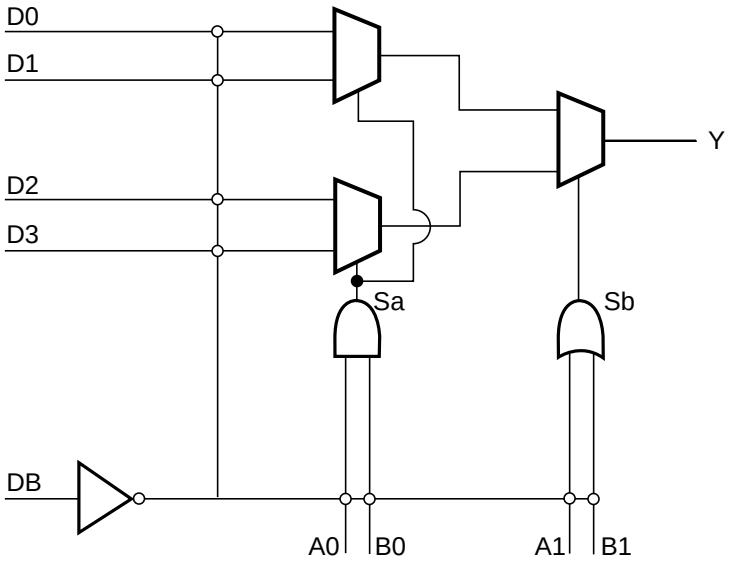


Figure 6 • *C-Cell*

Chip Architecture

The RT54SX-S family's chip architecture provides a unique approach to module organization and chip routing that delivers the best register/logic mix for a wide variety of new and emerging applications.

Module Organization

Actel has arranged all C-cell and R-cell logic modules into horizontal banks called *Clusters*. There are two types of Clusters: Type 1 contains two C-cells and one R-cell, while Type 2 contains one C-cell and two R-cells.

To increase design efficiency and device performance, Actel has further organized these modules into *SuperClusters* (see Figure 7 on page 7). SuperCluster 1 is a two-wide grouping of Type 1 clusters. SuperCluster 2 is a two-wide group containing one Type 1 cluster and one Type 2 cluster. RT54SX-S devices feature significantly more SuperCluster 1 modules than SuperCluster 2 modules because designers typically require significantly more combinatorial logic than flip-flops.

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative new local routing resources called *FastConnect* and *DirectConnect* which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (see Figure 8 on page 7 and Figure 9 on page 8). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of 0.1 ns.

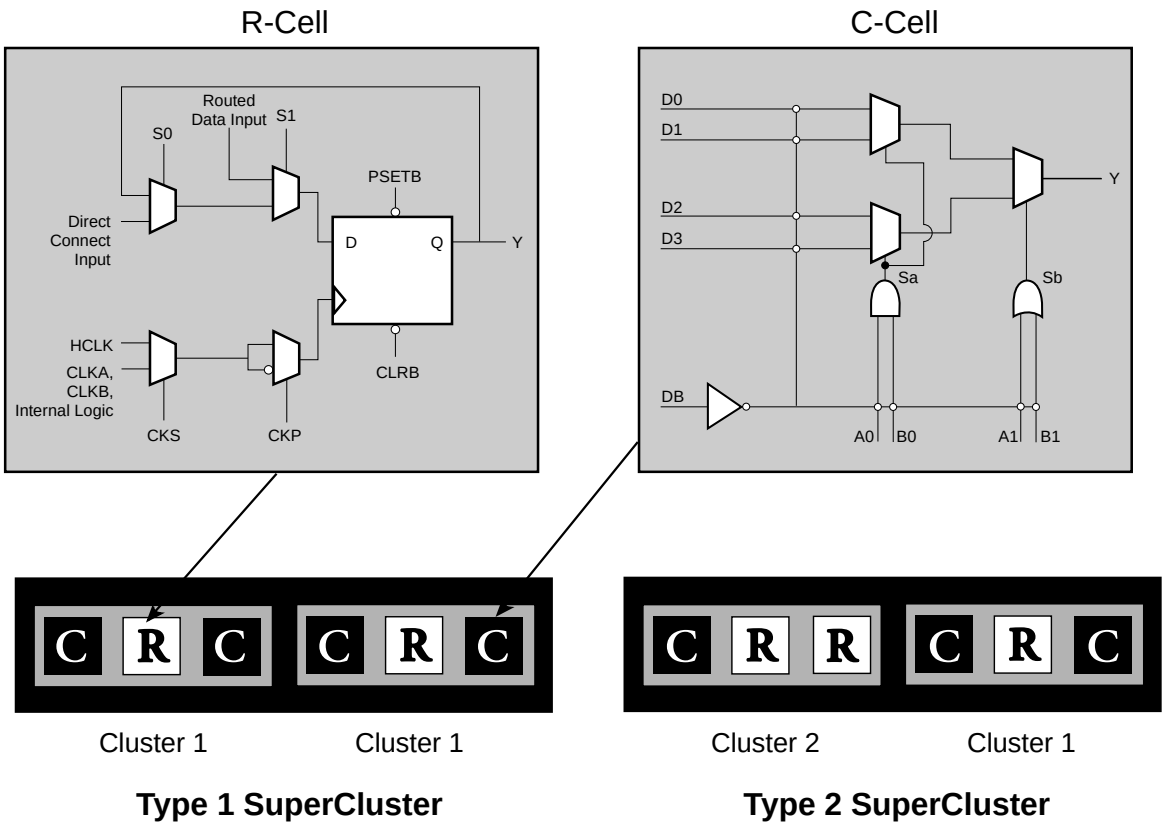


Figure 7 • *Cluster Organization*

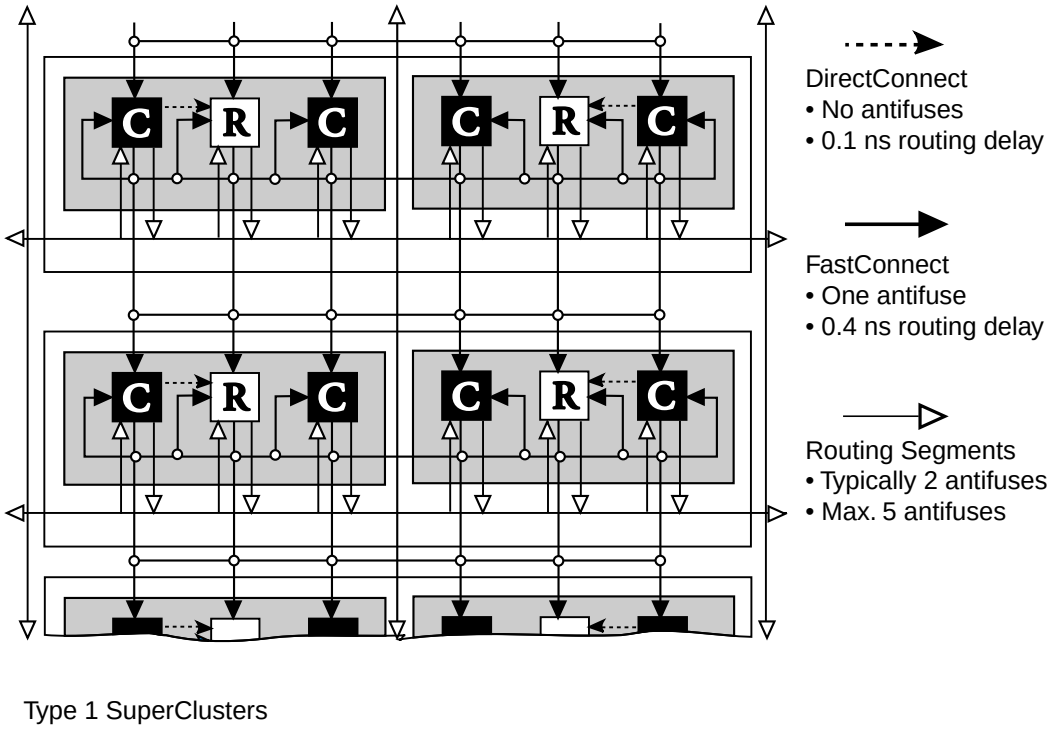


Figure 8 • *DirectConnect and FastConnect for Type 1 SuperClusters*

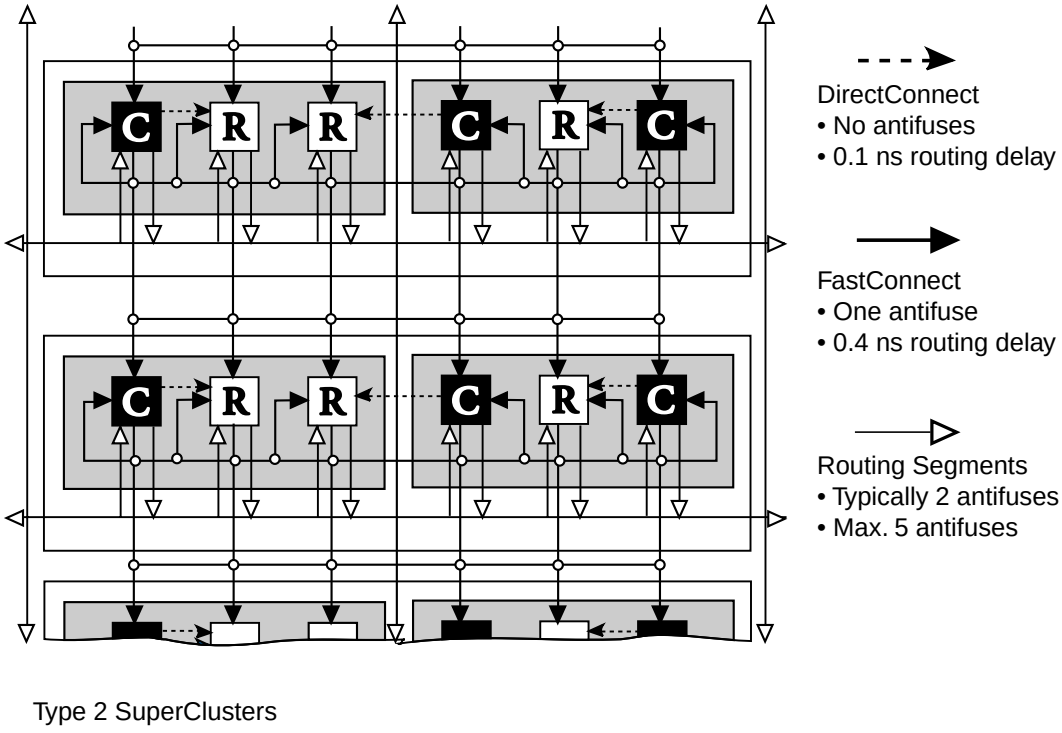


Figure 9 • *DirectConnect and FastConnect for Type 2 SuperClusters*

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster, and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.4 ns.

In addition to DirectConnect and FastConnect, the architecture makes use of two globally-oriented routing resources known as segmented routing and high-drive routing. Actel's segmented routing structure provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the 100% automatic place-and-route software to minimize signal propagation delays.

Clock Resources

Actel's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 8.9ns clock-to-out (pad-to-pad) performance of the Rt54SX-S devices. The hard-wired clock is tuned to provide clock skew is less than 0.5ns worst case.

The remaining two clocks (CLKA, CLKB) are global clocks that can be sourced from external pins or from internal logic signals within the RT54SX-S device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals then the external clock pin cannot be used for any other input and must be tied low or high. Figure 10 describes the clock circuit used for the constant load HCLK. Figure 11 describes the CLKA and CLKB circuit used in RT54SX-S devices with the exception of RT54SX72S. The CLKA, CLKB, and QCLK circuits for RT54SX72S are shown in Figure 12 on page 9.

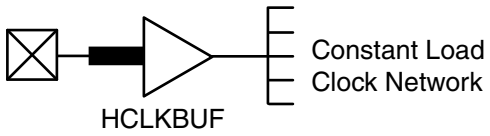
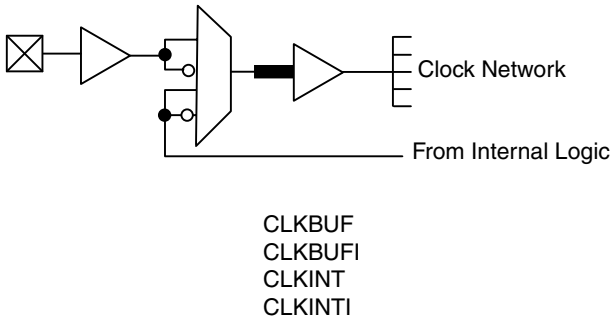


Figure 10 • *RT54SX-S Constant Load Clock Pad*



Note: *This does not include the clock pad for RT54SX72S.*

Figure 11 • *RT54SX-S Clock Pads*

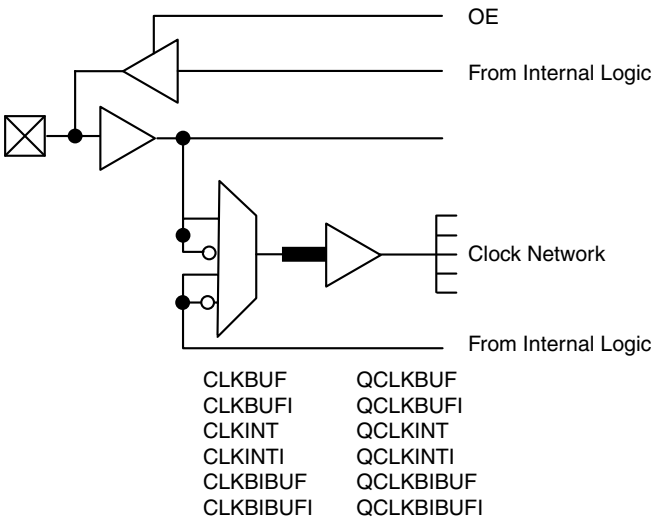


Figure 12 • RT54SX72S Clock/QClock Pads

Other Architecture Features

Technology

Actel's RT54SX-S family is implemented in high-voltage twin-well CMOS using 0.25µm design rules. The metal-to-metal antifuse is made up of a combination of amorphous silicon and dielectric material with barrier metals, and has a programmed ("on" state) resistance of 25 ¾ Ω with capacitance of 1.0 fF for low signal impedance.

Performance

The combination of architectural features described above enables RT54SX-S devices to operate with internal clock frequencies exceeding 250 MHz, enabling very fast execution of complex logic functions. Thus, the RT54SX-S family is an optimal platform upon which to integrate the functionality previously contained in multiple CPLDs. In addition, designs that previously would have required a gate array to meet performance goals can now be integrated into an RT54SX-S device with dramatic improvements in cost and time-to-market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance. With RT54SX-S devices, designers do not need to use complicated performance-enhancing design techniques such as redundant logic to reduce fanout on critical nets or the instantiation of macros in HDL code to achieve high performance.

I/O Modules

Each I/O on an RT54SX-S device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated registers, these I/Os, in combination with array registers, can achieve clock-to-out (PAD-to-PAD) timing as fast as 8.9 ns. I/O cells including embedded latches and flip-flops require instantiation in HDL code. This is a design complication not encountered in RT54SX-S FPGAs. Fast PAD-to-PAD timing ensures that the device will have little trouble interfacing with any other device in the system, which in turn enables parallel design of system components and reduces overall design time. Other I/O features are found in Table 1.

Table 1 • I/O Features

Function	Description
4 Level Selections	• LVTTL • 3.3V PCI • 5V CMOS • 5V PCI/TTL Selectable on an individual I/O basis
Input Buffer	5V tolerant
Output Buffer	"Hot-Swap" Capability • I/O on an unpowered device does not sink current • Can be used for "cold-sparing" Selectable on an individual I/O basis Individually selectable low-slew option
3.3V PCI	Individually selectable current clamp preventing reflection of a signal greater than 3.3V (V_{CCI})
Power Up	Individually selectable pull-ups and pull-downs during power up (default is to power up in tristate) Enables deterministic power up of device V_{CCA} and V_{CCI} can be powered in any order

Hot Swapping

RT54SX-S I/Os are specifically designed to be configurable as hot-swappable. During power up/down (or partial up/down), all I/Os are tristated. V_{CCA} and V_{CCI} do not have to be stable during power up/down and they are not required to power up or power down in any particular sequence in order to avoid damage to the RT54SX-S devices. After the RT54SX-S device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host-system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached.

Power Requirements

The RT54SX-S family supports 3.3 either or 5.0V I/O voltage operation and is designed to tolerate 5V inputs in each case (Table 2). Power consumption is extremely low due to the very short distances signals are required to travel to complete a circuit. Power requirements are further reduced due to the small number of antifuses in the path, and because of the low resistance properties of the antifuses. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power architecture on the market.

Table 2 • *Supply Voltages*

	V_{CCA}	V_{CCI}	Maximum Input Tolerance	Maximum Output Drive
RT54SX-S	2.5V	3.3V	5.0V	3.3V
	2.5V	5.0V	5.0V	5.0V

Boundary Scan Testing (BST)

All RT54SX-S devices are IEEE 1149.1 (JTAG) compliant. They offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins in conjunction with the program fuse. The functionality of each pin is described in Table 3.

Table 3 • *Boundary Scan Pin Functionality*

Program Fuse Blown (Dedicated Test Mode)	Program Fuse Not Blown (Flexible Mode)
TCK, TDI, TDO are dedicated test pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS	Use a pull-up resistor of 10k Ω on TMS

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the "Variation" dialog window. This dialog window is accessible through the Design Setup Wizard under the Tools menu in Actel's Designer software.

TRST pin

When the "Reserve JTAG Reset" box is checked (default setting in Designer software), the TRST pin will become a Boundary Scan Reset pin. In this mode, the TRST pin will function as an asynchronous, active-low input to initialize or reset the BST circuit. An internal pull-up resistor will be automatically enabled on the TRST pin.

The TRST pin will function as a user I/O when "Reserve JTAG Reset" box is not checked. The internal pull-up resistor will be disabled in this mode.

Dedicated Test Mode

When the "Reserve JTAG" box is checked in the Designer software, the RT54SX-S is placed in Dedicated Test mode, which configures the TDI, TCK, and TDO pins for BST or in-circuit verification with Silicon Explorer II. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins. In dedicated test mode, TCK, TDI, and TDO are dedicated test pins and become unavailable for pin assignment in the Pin Editor. The TMS pin will function as specified in the IEEE 1149.1 (JTAG) Specification.

Flexible Mode

When the "Reserve JTAG" box is not selected (default setting in Designer software), the RT54SX-S is placed in flexible mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or BST pins. In this mode the internal pull-up resistors on the TMS and TDI pins are disabled. An external 10k Ω pull-up resistor to VCCI is required on the TMS pin.

The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when a rising edge on TCK is detected while TMS is at logical low. Once the BST pins are in test mode they will remain in BST mode until the internal BST state machine reaches the "logic reset" state. At this point the BST pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set to logical HIGH.

The program fuse determines whether the device is in Dedicated Test or Flexible mode. The default (fuse not programmed) is Flexible mode.

Development Tool Support

The RT54SX-S RadTolerant devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP Series and Designer Series' tools. The Actel DeskTOP Series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place-and-route tools. Designer Series is Actel's suite of FPGA development point tools for PCs and Workstations that includes the ACTgen Macro Builder, Designer Series with DirectTime timing driven place-and-route and analysis tools, and device programming software.

RT54SX-S Probe Circuit Control Pins

The RT54SX-S RadTolerant devices contain internal probing circuitry that provides built-in access to every node in a design, enabling 100-percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy to use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer attaches to a PC's standard COM port, turning the PC into a fully functional 18 channel logic analyzer. Silicon Explorer allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TRST, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 13 illustrates the interconnection between Silicon Explorer II and the FPGA to perform in-circuit verification.

Design Considerations

For prototyping, the TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Because these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the security fuse should not be programmed during prototyping because doing so disables the probe circuitry.

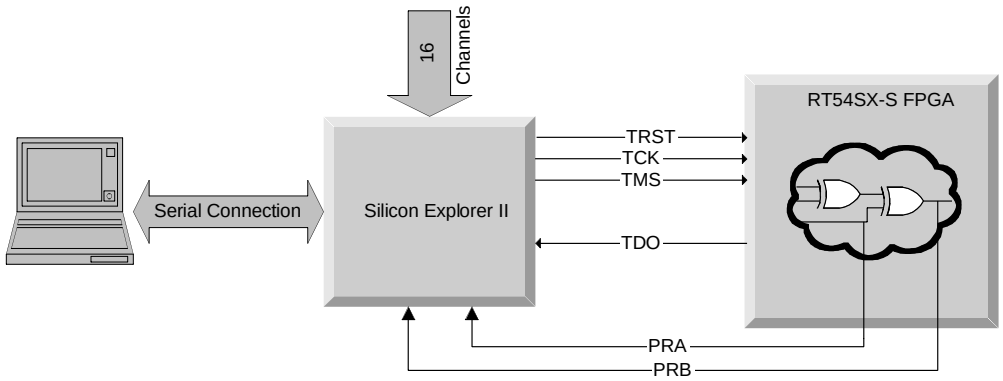


Figure 13 • *Probe Setup*

2.5V/3.3V/5.0V Operating Conditions

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits	Units
V_{CCI}	DC Supply Voltage	–0.3 to +6.0	V
V_{CCA}	DC Supply Voltage	–0.3 to +3.0	V
V_I	Input Voltage	–0.5 to +5.5	V
V_O	Output Voltage[2]	–0.5 to +V_{CCI} + 0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.*
2. *V_{CCI} is applied as 3.3V, and 5.0V respectively.*
3. *The I/O source sink numbers refer to tristated inputs and outputs.*

Recommended Operating Conditions

Parameter	Commercial	Military	Units
Temperature Range[1]	0 to +70	–55 to +125	°C
2.5V Power Supply Tolerance[2]	±8	±8	%V_{CC}
3.3V Power Supply Tolerance[2]	±9	±9	%V_{CC}
5V Power Supply Tolerance[2]	±5	±10	%V_{CC}

Notes:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*
2. *I/Os will be functional a maximum of 250µm after power supplies reach recommended operating range.*

Electrical Specifications

Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
V_{OH}	(I_{OH} = -20uA) (CMOS) (I_{OH} = -8mA) (TTL) (I_{OH} = -6mA) (TTL)	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	(V_{CCI} – 0.1) 2.4	V_{CCI} V_{CCI}	V
V_{OL}	(I_{OL}= 20uA) (CMOS) (I_{OL} = 12mA) (TTL) (I_{OL} = 8mA) (TTL)		0.10 0.50		 0.50	V
V_{IL}	Low Level Inputs		0.8		0.8	V
V_{IH}	High Level Inputs	2.0		2.0		V
I_{IL}/I_{IH}	Input Leakage Current, V_{IN} = V_{CCI} or GND	–20	20	–20	20	µA
I_{OZ}	3-State Output Leakage Current, V_{OUT} = V_{CCI} or GND	–20	20	–20	20	µA
t_R, t_F	Input Transition Time t_R, t_F		10		10	ns
C_{IO}	C_{IO} I/O Capacitance		10		10	pF
I_{CC}	Standby Current, I_{CC}		10		25	mA
$I_{CC\ (D)}$	Standby Current, $I_{CC\ (D)}$ $I_{DYNAMIC}$	See the Power Dissipation section page 15.				

Actel MIL-STD-883 Class B Product Flow

Step	Screen	883 Method	883—Class B Requirement
1.	Internal Visual	2010, Test Condition B	100%
2.	Temperature Cycling	1010, Test Condition C	100%
3.	Constant Acceleration	2001, Test Condition D or E, Y_1, Orientation Only	100%
4.	Seal a. Fine b. Gross	1014	 100% 100%
5.	Visual Inspection	2009	100%
6.	Pre-Burn-In Electrical Parameters	In accordance with applicable Actel device specification	100%
7.	Burn-in Test	1015, Condition D, 160 hours @ 125°C or 80 hours @ 150°C	100%
8.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
9.	Percent Defective Allowable	5%	All Lots
10.	Final Electrical Test	In accordance with applicable Actel device specification, which includes a, b, and c:	
	a. Static Tests (1) 25°C (Subgroup 1, Table I) (2) –55°C and +125°C (Subgroups 2, 3, Table I)	 5005 5005	100%
	b. Functional Tests (1) 25°C (Subgroup 7, Table I) (2) –55°C and +125°C (Subgroups 8A and 8B, Table I)	 5005 5005	100%
	c. Switching Tests at 25°C (Subgroup 9, Table I)	 5005	100%
11.	External Visual	2009	100%

Actel Extended Flow[1]

Step	Screen	Method	Requirement
1.	Wafer Lot Acceptance	5007	All Lots
2.	Destructive In-Line Bond Pull[3]	2011, Condition D	Sample
3.	Internal Visual	2010, Condition A	100%
4.	Serialization		100%
5.	Temperature Cycling	1010, Condition C	100%
6.	Constant Acceleration	2001, Condition D or E, Y_1 Orientation Only	100%
7.	Particle Impact Noise Detection	2020, Condition A	100%
8.	Radiographic	2012 (one view only)	100%
9.	Pre-Burn-In Test	In accordance with applicable Actel device specification	100%
10.	Burn-in Test	1015, Condition D, 240 hours @ 125°C minimum	100%
11.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
12.	Reverse Bias Burn-In	1015, Condition C, 72 hours @ 150°C minimum	100%
13.	Interim (Post-Burn-In) Electrical Parameters	In accordance with applicable Actel device specification	100%
14.	Percent Defective Allowable (PDA) Calculation	5%, 3% Functional Parameters @ 25°C	All Lots
15.	Final Electrical Test	In accordance with Actel applicable device specification which includes a, b, and c:	100%
	a. Static Tests		100%
	(1) 25°C (Subgroup 1, Table1)	5005	
	(2) –55°C and +125°C (Subgroups 2, 3, Table 1)	5005	
	b. Functional Tests		100%
	(1) 25°C (Subgroup 7, Table 15)	5005	
	(2) –55°C and +125°C (Subgroups 8A and B, Table 1)	5005	
	c. Switching Tests at 25°C (Subgroup 9, Table 1)	5005	100%
16.	Seal	1014	100%
	a. Fine		
	b. Gross		
17.	External Visual	2009	100%

Notes:

1. *Actel offers Extended Flow for users requiring additional screening beyond MIL-STD-833, Class B requirement. Actel is offering this Extended Flow incorporating the majority of the screening procedures as outlined in Method 5004 of MIL-STD-883, Class S. The exceptions to Method 5004 are shown in notes 2 and 3 below.*
2. *MIL-STD-883, Method 5004 requires a 100 percent Radiation latch-up testing to Method 1020. Actel will not be performing any radiation testing, and this requirement must be waived in its entirety.*
3. *Method 5004 requires 100 percent nondestructive bond part to Method 2003. Actel substitutes a destructive bond path to Method 2011 Condition D on a sample basis only.*

Power Dissipation

$$P = [I_{CC}\text{standby} + I_{CC}\text{active}] * V_{CCA} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CCA} - V_{OH}) * M$$

where:

I_{CC} standby is the current flowing when no inputs or outputs are changing.

I_{CC} active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

Accurate values for N and M are difficult to determine because they depend on the design and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

The power due to standby current is typically a small component of the overall power. Standby power is shown below for military, worst case conditions (125°C).

I_{CC}	V_{CCA}	Power
25 mA	2.7V	68 mW

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs.

An additional component of the active power dissipation is the totempole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

The power dissipated by a CMOS circuit can be expressed by Equation 1:

$$\text{Power } (\mu W) = C_{EQ} * V_{CCA}^2 * F \quad (1)$$

where:

C_{EQ} = Equivalent capacitance in pF

V_{CCA} = Power supply in volts (V)

F = Switching frequency in MHz

Equivalent Capacitance

Equivalent capacitance is calculated by measuring I_{CC}active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CCA}. Equivalent capacitance is frequency-independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values (pF)

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$P_{AC} = V_{CCA}^2 * [(m * C_{EQM} * f_m)_{\text{Module}} + (n * C_{EQI} * f_n)_{\text{Input Buffer}} + (0.5 * (q_1 * C_{EQCR} * f_{q1}) + (r_1 * f_{q1}))_{RCLKA} + (0.5 * (q_2 * C_{EQCR} * f_{q2}) + (r_2 * f_{q2}))_{RCLKB} + (0.5 * (s_1 * C_{EQHV} * f_{s1}) + (C_{EQHF} * f_{s1})_{HCLK}] + V_{CCI}^2 * [(p * (C_{EQO} + C_L) * f_p)_{\text{Output Buffer}}] \quad (2)$$

		RT54SX32S	RT54SX72S
Equivalent Capacitance (pF)			
Modules	C_{EQM}	2.0	2.0
Input Buffers	C_{EQI}	1.4	1.4
Output Buffers	C_{EQO}	7.4	7.4
Routed Array Clock Buffer Loads	C_{EQCR}	1.9	1.9
Variable Capacitance of Dedicated Array Clock	C_{EQHV}	1.2	1.2
Fixed Capacitance of Dedicated Array Clock	C_{EQHF}	195.0	449.0
Fixed Capacitance (pF)			
routed_Clk1	r_1	194.0	475.0
routed_Clk2	r_2	194.0	475.0
Fixed Clock Loads			
Maximum Clock Loads on Dedicated Array Clock	s_1	1080	2012

where:

m = Number of logic modules switching at f_m

n = Number of input buffers switching at f_n

p = Number of output buffers switching at f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = Fixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

s_1 = Fixed number of clock loads on the dedicated array clock = (1080 for RT54SX32S)

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output lead capacitance in pF

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Determining Average Switching Frequency

To determine the switching frequency for a design, the user must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to estimate the upper limits of power dissipation:

Logic Modules (m)	=	80% of modules
Inputs Switching (n)	=	# inputs/4
Outputs Switching (p)	=	# output/4
First Routed Array Clock Loads (q_1)	=	40% of sequential modules
Second Routed Array Clock Loads (q_2)	=	40% of sequential modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F/2
Average Second Routed Array Clock Rate (f_{q2})	=	F/2
Average Dedicated Array Clock Rate (f_{s1})	=	F

PCI Compliance for the RT54SX-S Family

The RT54SX-S family supports 3.3V and 5V PCI and is compliant with the PCI Local Bus Specification Rev. 2.1.

DC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		4.5	5.5	V
V_{IH}	Input High Voltage[1]		2.0	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage[1]		–0.5	0.8	V
I_{IH}	Input High Leakage Current	V_{IN} = 2.7		70	µA
I_{IL}	Input Low Leakage Current	V_{IN} = 0.5		–70	µA
V_{OH}	Output High Voltage	I_{OUT} = –2 mA	2.4		V
V_{OL}	Output Low Voltage[2]	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
2. *Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, and, when used AD[63::32], C/BE[7::4]#, PAR64, REQ64#, and ACK64#.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean, in general, that components for expansion boards would need to use alternatives to ceramic PGA packaging (i.e., PQFP, SGA, etc.).*

AC Specifications (5.0V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 1.4$ [1]	–44		mA
		$1.4 \le V_{OUT} < 2.4$ [1, 2]	$(–44 + (V_{OUT} – 1.4)/0.024)$		mA
		$3.1 < V_{OUT} < V_{CCI}$ [1, 3]		Equation A on page 19	
	(Test Point)	$V_{OUT} = 3.1$ [3]		–142	mA
$I_{OL(AC)}$	Switching Current Low	$V_{OUT} \ge 2.2$ [1]	95		mA
		$2.2 > V_{OUT} > 0.55$ [1]	$(V_{OUT}/0.023)$		mA
		$0.71 > V_{OUT} > 0$ [1, 3]		Equation B on page 19	
	(Test Point)	$V_{OUT} = 0.71$		206	mA
I_{CL}	Low Clamp Current	$–5 < V_{IN} \le –1$	$–25 + (V_{IN} + 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	0.4V to 2.4V load[4]	1	5	V/ns
$slew_F$	Output Fall Slew Rate	2.4V to 0.4V load[4]	1	5	V/ns

Notes:

1. *Refer to the V/I curves in Figure 14 on page 19. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Note that this segment of the minimum current curve is drawn from the AC drive point directly to the DC drive point rather than toward the voltage rail (as is done in the pull-down curve). This difference is intended to allow for an optional N-channel pull-up.*
3. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 14 on page 19. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
4. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per revision 2.0 of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is now required (the maximum is no longer simply a guideline). Since adherence to the maximum slew rate was not required prior to revision 2.1 of the specification, there may be components in the market for some time that have faster edge rates; therefore, motherboard designers must bear in mind that rise and fall times faster than this specification could occur, and should ensure that signal integrity modeling accounts for this. Rise slew rate does not apply to open drain outputs.*

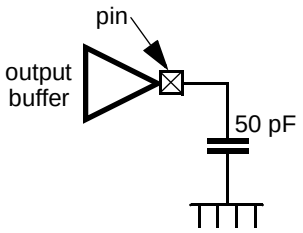


Figure 14 shows the 5.0V PCI V/I curve and the minimum and maximum PCI drive characteristics of the RT54SX-S family.

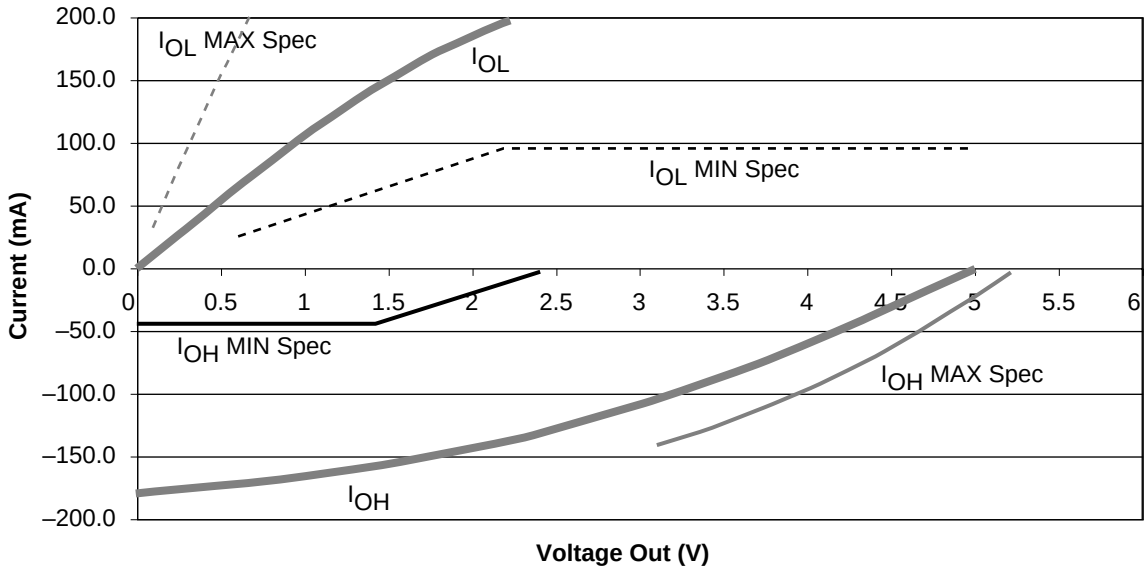


Figure 14 • 5.0V PCI Curve for RT54SX-S Family

Equation A

$$I_{OH} = 11.9 * (V_{OUT} - 5.25) * (V_{OUT} + 2.45)$$
$$\text{for } V_{CCI} > V_{OUT} > 3.1V$$

Equation B

$$I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.71V$$

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{CCA}	Supply Voltage for Array		2.3	2.7	V
V_{CCI}	Supply Voltage for I/Os		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{CCI}$	V_{CCI} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{CCI}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{CCI}$		V
I_{IL}/I_{IH}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$		±10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{CCI}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{CCI}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

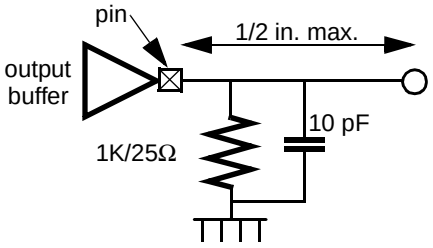
1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input V_{IN}.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10pF (except for CLK) with an exception granted to motherboard-only devices, which could be up to 16 pF, in order to accommodate PGA packaging. This would mean in general that components for expansion boards would need to use alternatives to ceramic PGA packaging.*

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{CCI} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation C on page 22	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{CCI}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation D on page 22	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{CCI} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load[3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load[3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 15 on page 22. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST# which are system outputs. "Switching Current High" specification are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD# which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (C and D) are provided with the respective diagrams in Figure 15 on page 22. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*



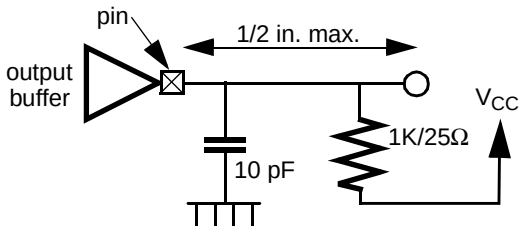


Figure 15 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the RT54SX-S family.

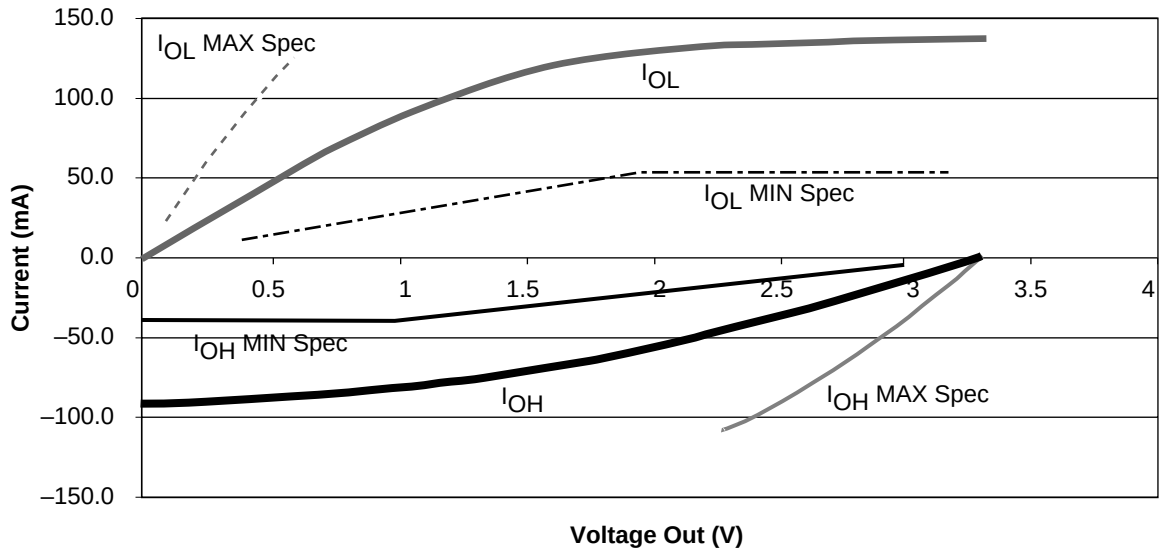


Figure 15 • *3.3V PCI Curve for RT54SX-S Family*

Equation C

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } V_{CCI} > V_{OUT} > 0.7\ V_{CCI}$$

Equation D

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

Junction Temperature (T_J)

The temperature that is selected in Designer Series software is the junction temperature, not ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. Equation 3, shown below, can be used to calculate junction temperature.

$$\text{Junction Temperature} = \Delta T + T_a \quad (3)$$

Where:

T_a = Ambient Temperature

ΔT = Gradient between junction (silicon) and ambient

$\Delta T = \theta_{ja} * P$

P = Estimating Power Consumption better calculation

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the Package Thermal Characteristics section below.

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. θ_{ja} thermal characteristics are shown with two different air flow rates.

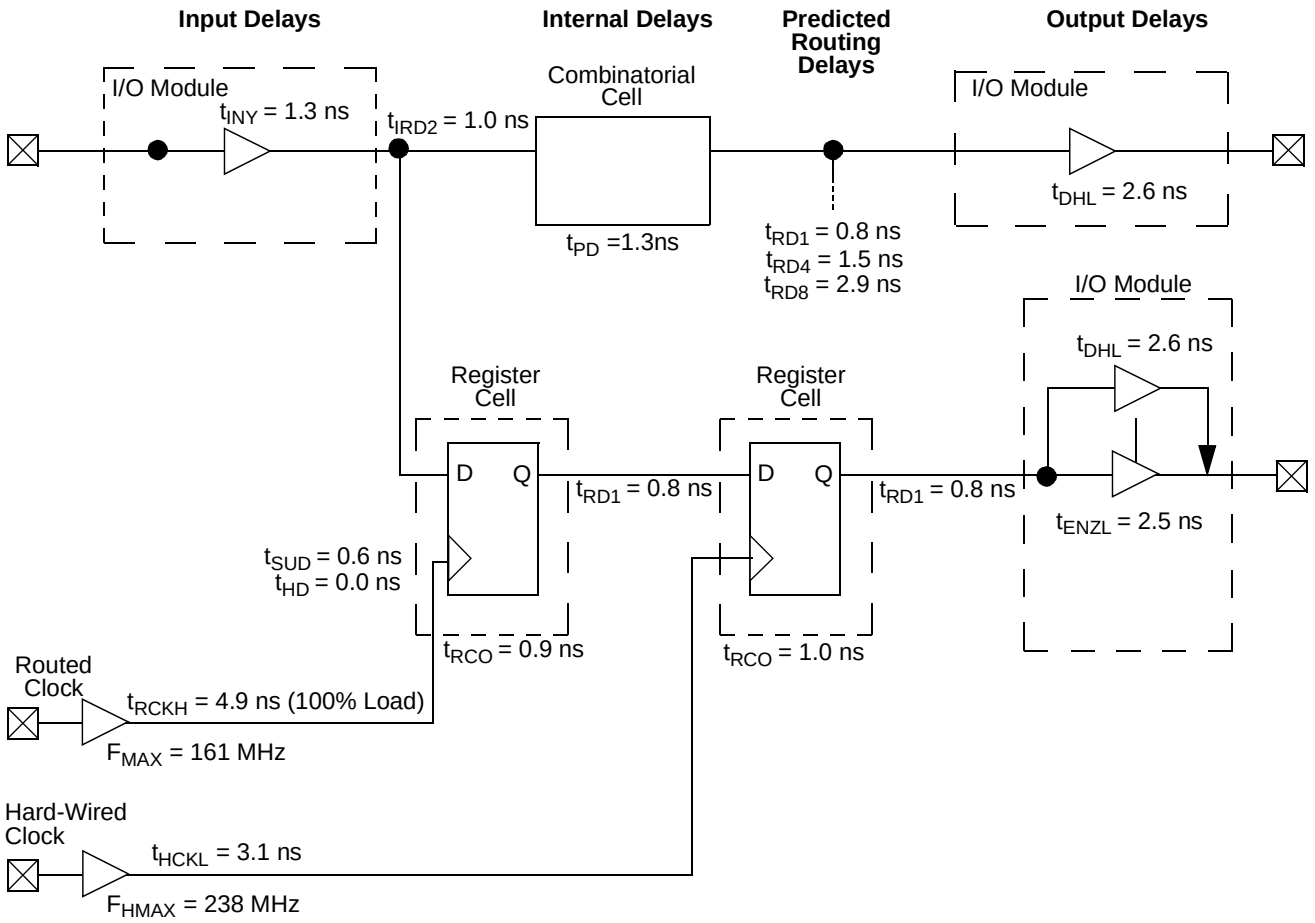
The maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a CQFP 208-pin package at military temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{150\text{°C} - 125\text{°C}}{22\text{°C/W}} = 1.14\text{W}$$

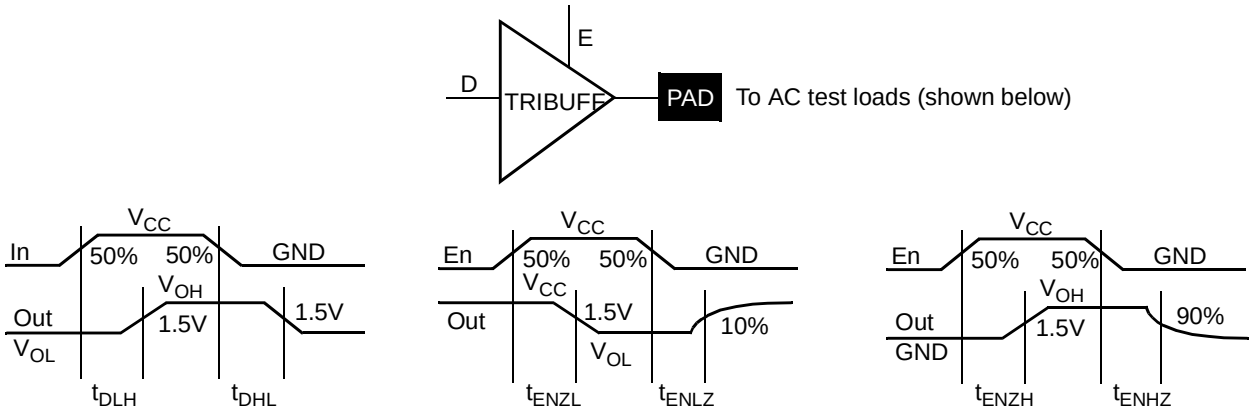
Package Type	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 300 ft/min	Units
RT54SX32S					
Ceramic Quad Flat Pack (CQFP)	208	6.3	22	14	°C/W
Ceramic Quad Flat Pack (CQFP)	256	6.2	20	10	°C/W
RT54SX72S					
Ceramic Quad Flat Pack (CQFP)	208	6.3	22	13	°C/W
Ceramic Quad Flat Pack (CQFP) with Heat Sink	256	6.2	19	9	°C/W

RT54SX-S Timing Model*

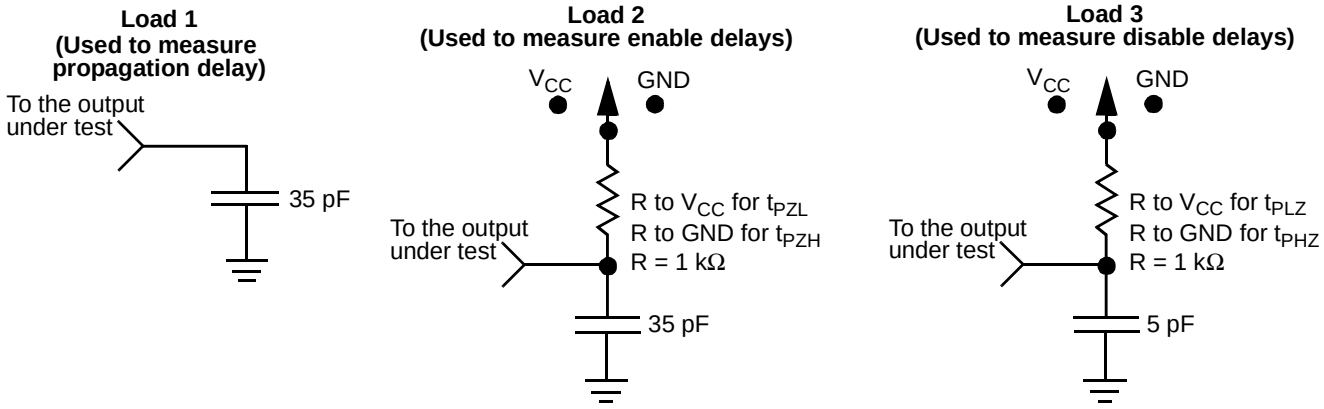


**Values shown for RTSX32S-1, 5V TTL worst-case military conditions.*

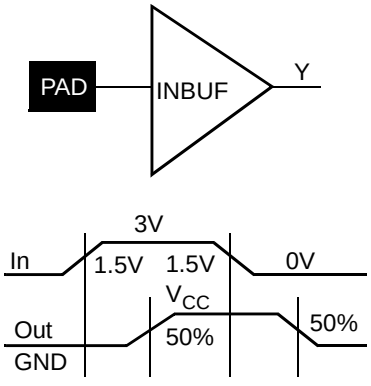
Output Buffer Delays



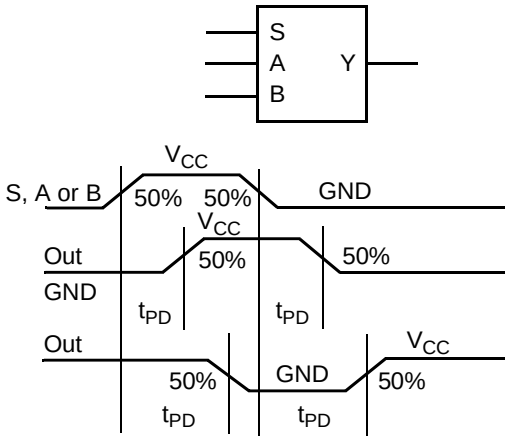
AC Test Loads



Input Buffer Delays

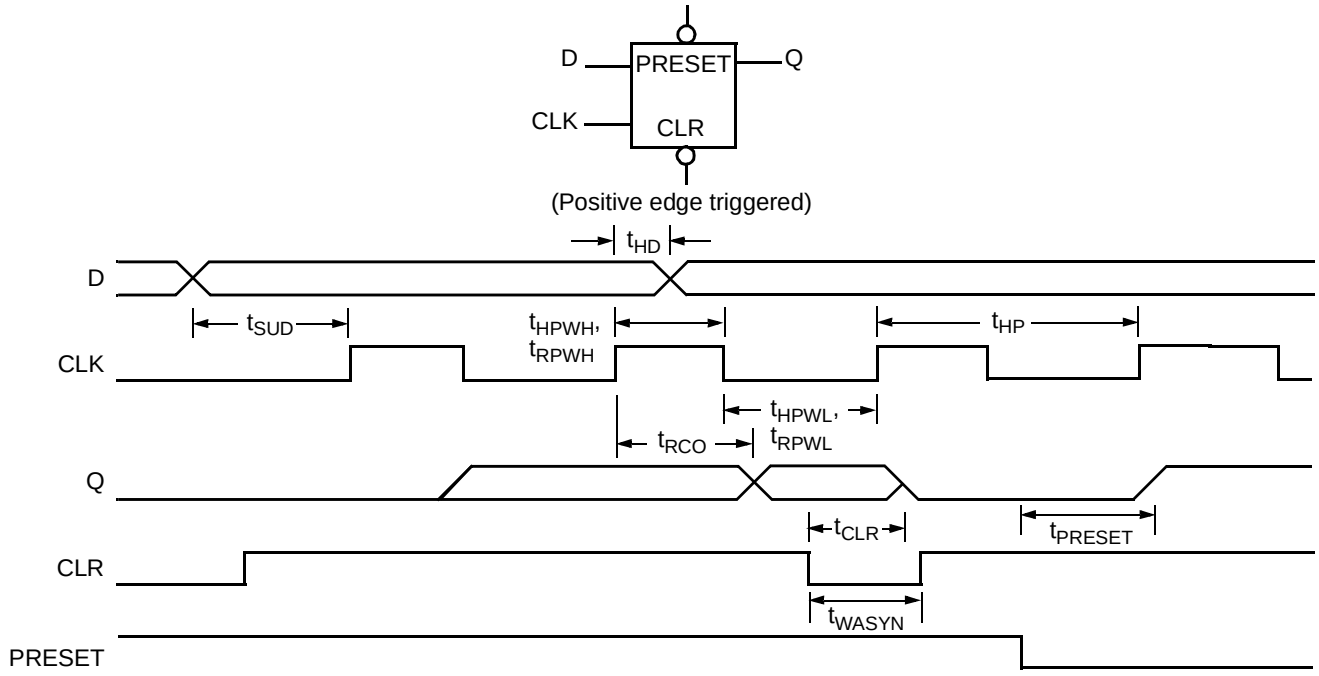


C-Cell Delays



Cell Timing Characteristics

Flip-Flops



Timing Characteristics

RT54SX-S device timing characteristics are in three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all RT54SX-S devices. Internal routing delays are device dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most time-critical paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6% of the nets in a design may be designated as critical, while 90% of the nets in a design are typical.

Long Tracks

Some nets in the design use long tracks. Long tracks are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes five antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 4 ns to 8.4 ns delay. This additional delay is represented statistically in higher fanout routing delays in the data sheet specifications section.

Timing Derating

RT54SX-S devices are manufactured in a CMOS process. Therefore, device performance varies according to temperature, voltage, and process variations. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and best-case processing. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case processing.

Temperature and Voltage Derating Factors

(Normalized to Worst-Case Military, T_J = 125°C, V_{CCA} = 2.3V)

	Junction Temperature (T_J)						
V_{CCA}	–55	–40	0	25	70	85	125
2.3	0.68	0.69	0.75	0.77	0.86	0.90	1.00
2.5	0.64	0.65	0.70	0.72	0.81	0.84	0.93
2.7	0.60	0.61	0.66	0.68	0.76	0.79	0.88

RT54SX32S Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.6	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.4		0.4	ns
t_{RD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{RD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{RD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{RD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{RD12}	FO=12 Routing Delay		4.0		4.7	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.1	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.6		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		2.2		ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V PCI		1.4		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V PCI		1.5		1.8	ns
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V LVTTL		1.4		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V LVTTL		1.5		1.8	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V PCI		1.3		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V PCI		1.7		2.0	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V TTL		1.3		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V TTL		1.7		2.0	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V CMOS		1.7		2.0	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V CMOS		1.6		1.9	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{IRD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{IRD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{IRD12}	FO=12 Routing Delay		4.0		4.7	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.4		4.0	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.4		4.0	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.5		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		5.0		ns
f_{HMAX}	Maximum Frequency		238		200	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.2		3.7	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.2		3.7	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		4.0		4.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.8		4.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.9		5.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.8		4.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.0	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.0	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.0	ns

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		3.1		3.6	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		3.1		3.6	ns
t_{HPWH}	Minimum Pulse Width HIGH	2.1		2.5		ns
t_{HPWL}	Minimum Pulse Width LOW	2.1		2.5		ns
t_{HCKSW}	Maximum Skew		0.5		0.6	ns
t_{HP}	Minimum Period	4.2		5.0		ns
f_{HMAX}	Maximum Frequency		238		200	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		3.1		3.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		3.7		4.6	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		3.8		4.4	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		4.9		5.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		3.8		4.5	ns
t_{RPWH}	Min. Pulse Width HIGH	3.1		3.7		ns
t_{RPWL}	Min. Pulse Width LOW	3.1		3.7		ns
t_{RCKSW}	Maximum Skew (Light Load)		1.9		2.3	ns
t_{RCKSW}	Maximum Skew (50% Load)		1.9		2.3	ns
t_{RCKSW}	Maximum Skew (100% Load)		1.9		2.3	ns

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.9		3.4	ns
t_{DHLS}	Data-to-Pad High to LOW – low slew		15.0		17.7	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.5	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.3		10.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		3.0	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.065		0.075	ns/pF
3.3V LVTTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		12.7		14.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.9		3.4	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		12.7		14.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.7		4.4	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.7		4.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0	ns
d_{TLH}	Delta LOW to HIGH		0.033		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.067		0.073	ns/pF

Notes:

1. *Delays based on 10pF loading and 25 Ω resistance.*
2. *Delays based on 35pF loading.*

RT54SX32S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.`**	**Units**
5.0V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.9		3.4	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		9.7		11.4	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.8		3.3	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		10.1		11.9	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.2		3.8	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.9		5.8	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.1		4.9	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.022	ns/pF
d_{THL}	Delta HIGH to LOW		0.032		0.04	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.06		0.07	ns/pF
5.0V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.6		3.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		4.1	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		8.9		10.4	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.5		3.0	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.0		10.6	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.4	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.4		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.6		4.4	ns
d_{TLH}	Delta LOW to HIGH		0.017		0.023	ns/pF
d_{THL}	Delta HIGH to LOW		0.031		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.06		0.07	ns/pF
5.0V CMOS Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.1		3.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.2		3.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		8.5		10.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.71	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		8.8		10.4	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.5		4.7	ns

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

RT54SX72S Timing Characteristics

(Worst-Case Military Conditions, V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
C-Cell Propagation Delays[1]						
t_{PD}	Internal Array Module		1.3		1.6	ns
Predicted Routing Delays[2]						
t_{DC}	FO=1 Routing Delay, Direct Connect		0.1		0.1	ns
t_{FC}	FO=1 Routing Delay, Fast Connect		0.4		0.4	ns
t_{RD1}	FO=1 Routing Delay		0.9		1.0	ns
t_{RD2}	FO=2 Routing Delay		1.2		1.4	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.0	ns
t_{RD4}	FO=4 Routing Delay		1.9		2.3	ns
t_{RD8}	FO=8 Routing Delay		3.7		4.3	ns
t_{RD12}	FO=12 Routing Delay		5.1		6.0	ns
R-Cell Timing						
t_{RCO}	Sequential Clock-to-Q		1.0		1.2	ns
t_{CLR}	Asynchronous Clear-to-Q		0.9		1.1	ns
t_{PRESET}	Asynchronous Preset-to-Q		1.0		1.2	ns
t_{SUD}	Flip-Flop Data Input Set-Up	0.6		0.8		ns
t_{HD}	Flip-Flop Data Input Hold	0.0		0.0		ns
t_{WASYN}	Asynchronous Pulse Width	1.8		2.2		ns
Input Module Propagation Delays						
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V PCI		1.4		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V PCI		1.5		1.8	ns
t_{INYH}	Input Data Pad-to-Y HIGH 3.3V LVTTL		1.4		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 3.3V LVTTL		1.5		1.8	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V PCI		1.3		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V PCI		1.7		2.0	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V LVTTL		1.3		1.6	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V LVTTL		1.7		2.0	ns
t_{INYH}	Input Data Pad-to-Y HIGH 5.0V CMOS		1.7		2.0	ns
t_{INYL}	Input Data Pad-to-Y LOW 5.0V CMOS		1.6		1.9	ns
Input Module Predicted Routing Delays[2]						
t_{IRD1}	FO=1 Routing Delay		0.8		0.9	ns
t_{IRD2}	FO=2 Routing Delay		1.0		1.2	ns
t_{IRD3}	FO=3 Routing Delay		1.4		1.6	ns
t_{IRD4}	FO=4 Routing Delay		1.5		1.8	ns
t_{IRD8}	FO=8 Routing Delay		2.9		3.4	ns
t_{IRD12}	FO=12 Routing Delay		4.0		4.7	ns

Notes:

1. *For dual-module macros, use $t_{PD} + t_{RD1} + t_{PDn}$, $t_{RCO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance.*

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		5.8		1.8	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		5.8		6.8	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.6		4.3		ns
t_{HPWL}	Minimum Pulse Width LOW	3.6		4.3		ns
t_{HCKSW}	Maximum Skew		1.4		1.6	ns
t_{HP}	Minimum Period	7.2		8.6		ns
f_{HMAX}	Maximum Frequency		139		116	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		5.9		6.8	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		5.9		6.8	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		7.4		8.7	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		9.1		10.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.7		6.8		ns
t_{RPWL}	Min. Pulse Width LOW	5.7		6.8		ns
t_{RCKSW}	Maximum Skew (Light Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		3.5		3.7	ns

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Dedicated (Hard-Wired) Array Clock Network						
t_{HCKH}	Input LOW to HIGH (Pad to R-Cell Input)		5.3		6.1	ns
t_{HCKL}	Input HIGH to LOW (Pad to R-Cell Input)		5.3		6.1	ns
t_{HPWH}	Minimum Pulse Width HIGH	3.6		4.3		ns
t_{HPWL}	Minimum Pulse Width LOW	3.6		4.3		ns
t_{HCKSW}	Maximum Skew		1.4		1.6	ns
t_{HP}	Minimum Period	7.2		8.6		ns
f_{HMAX}	Maximum Frequency		139		116	MHz
Routed Array Clock Networks						
t_{RCKH}	Input LOW to HIGH (Light Load) (Pad to R-Cell Input)		5.7		6.6	ns
t_{RCKL}	Input HIGH to LOW (Light Load) (Pad to R-Cell Input)		5.7		6.6	ns
t_{RCKH}	Input LOW to HIGH (50% Load) (Pad to R-Cell Input)		6.8		8.4	ns
t_{RCKL}	Input HIGH to LOW (50% Load) (Pad to R-Cell Input)		7.0		8.2	ns
t_{RCKH}	Input LOW to HIGH (100% Load) (Pad to R-Cell Input)		9.1		10.8	ns
t_{RCKL}	Input HIGH to LOW (100% Load) (Pad to R-Cell Input)		7.0		8.3	ns
t_{RPWH}	Min. Pulse Width HIGH	5.7		6.8		ns
t_{RPWL}	Min. Pulse Width LOW	5.7		6.8		ns
t_{RCKSW}	Maximum Skew (Light Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (50% Load)		3.5		3.7	ns
t_{RCKSW}	Maximum Skew (100% Load)		3.5		3.7	ns

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 3.0V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
3.3V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.7		3.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		2.9		3.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		15.0		17.7	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.1		2.5	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.3		10.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		2.7		3.9	ns
t_{ENLZ}	Enable-to-Pad, L to Z		2.7		3.9	ns
t_{ENHZ}	Enable-to-Pad, H to Z		2.5		3.0	ns
d_{TLH}	Delta LOW to HIGH		0.03		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.015		0.015	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.065		0.075	ns/pF
3.3V LVTTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.7		4.3	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.6		4.2	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		12.7		14.9	ns
t_{ENZL}	Enable-to-Pad, Z to L		2.9		3.4	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		12.7		14.9	ns
t_{ENZH}	Enable-to-Pad, Z to H		3.7		4.4	ns
t_{ENLZ}	Enable-to-Pad, L to Z		3.7		4.4	ns
t_{ENHZ}	Enable-to-Pad, H to Z		3.4		4.0	ns
d_{TLH}	Delta LOW to HIGH		0.033		0.04	ns/pF
d_{THL}	Delta HIGH to LOW		0.02		0.02	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.067		0.073	ns/pF

Notes:

1. *Delays based on 10pF loading and 25 Ω resistance.*
2. *Delays based on 35pF loading.*

RT54SX72S Timing Characteristics (continued)

(Worst-Case Military Conditions V_{CCA} = 2.3V, V_{CCI} = 4.5V, T_J = 125°C)

		'–1' Speed		'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.`**	**Units**
5.0V PCI Output Module Timing[1]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.9		3.4	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.8		4.4	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		9.7		11.4	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.8		3.3	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		10.1		11.9	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.2		3.8	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.9		5.8	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		4.1		4.9	ns
d_{TLH}	Delta LOW to HIGH		0.02		0.022	ns/pF
d_{THL}	Delta HIGH to LOW		0.032		0.04	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.06		0.07	ns/pF
5.0V TTL Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		2.6		3.1	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.5		4.1	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		8.9		10.4	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.5		3.0	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		9.0		10.6	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		2.8		3.4	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.4		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.6		4.4	ns
d_{TLH}	Delta LOW to HIGH		0.017		0.023	ns/pF
d_{THL}	Delta HIGH to LOW		0.031		0.037	ns/pF
d_{THLS}	Delta HIGH to LOW – low slew		0.06		0.07	ns/pF
5.0V CMOS Output Module Timing[2]						
t_{DLH}	Data-to-Pad LOW to HIGH		3.1		3.6	ns
t_{DHL}	Data-to-Pad HIGH to LOW		3.2		3.8	ns
t_{DHLS}	Data-to-Pad HIGH to LOW – low slew		8.5		10.0	ns
t_{ENZL}	Enable-to-Pad, Z to LOW		2.3		2.71	ns
t_{DENZLS}	Enable-to-Pad, Z to LOW – low slew		8.8		10.4	ns
t_{ENZH}	Enable-to-Pad, Z to HIGH		3.0		3.6	ns
t_{ENLZ}	Enable-to-Pad, LOW to Z		4.5		5.3	ns
t_{ENHZ}	Enable-to-Pad, HIGH to Z		3.5		4.7	ns

Notes:

1. *Delays based on 50pF loading.*
2. *Delays based on 35pF loading.*

Pin Description

CLKA/B Clock A and B

These pins are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. The clock input is buffered prior to clocking the R-cells. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating. (For RT54SX72S, these clocks can be configured as user I/O.)

QCLKA/B/C/D, I/O Quadrant Clock A, B, C, and D

These four pins are the quadrant clock inputs and are only for RT54SX72S. They are clock inputs for clock distribution networks. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. Each of these clock inputs can drive up to a quarter of the chip, or they can be grouped together to drive multiple quadrants. The clock input is buffered prior to clocking the R-cells. If not used as a clock it will behave as a regular I/O.

GND Ground

LOW supply voltage.

HCLK Dedicated (Hard-wired) Array Clock

This pin is the clock input for sequential modules. Input levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. This input is directly wired to each R-cell and offers clock speeds independent of the number of R-cells being driven. If not used, this pin must be set LOW or HIGH on the board. It must not be left floating.

I/O Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Based on certain configurations, input and output levels are compatible with standard TTL, LVTTL, 3.3V PCI or 5.0V PCI specifications. Unused I/O pins are automatically tristated by the Designer Series software.

NC No Connection

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O, PRB, I/O Probe A/B

The Probe pin is used to output data from any user-defined design node within the device. This independent diagnostic pin can be used in conjunction with the other probe pin to allow real-time diagnostic output of any signal path within the device. The Probe pin can be used as a user-defined I/O when verification has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality.

TDI, I/O Test Data Input

Serial input for boundary scan testing and diagnostic probe. In flexible mode, TDI is active when the TMS pin is set LOW (refer to Table 3 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TDO, I/O Test Data Output

Serial output for boundary scan testing. In flexible mode, TDO is active when the TMS pin is set LOW (refer to Table 3 on page 10). This pin functions as an I/O when the boundary scan state machine reaches the "logic reset" state.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1149.1 Boundary Scan pins (TCK, TDI, TDO, TRST). In flexible mode when the TMS pin is set LOW, the TCK, TDI, and TDO pins are boundary scan pins (refer to Table 3 on page 10). Once the boundary scan pins are in test mode, they will remain in that mode until the internal boundary scan state machine reaches the "logic reset" state. At this point, the boundary scan pins will be released and will function as regular I/O pins. The "logic reset" state is reached 5 TCK cycles after the TMS pin is set HIGH. In dedicated test mode, TMS functions as specified in the IEEE 1149.1 specifications.

TRST, I/O Boundary Scan Reset Pin

Once it is configured as the JTAG Reset pin, the TRST pin functions as an active-low input to asynchronously initialize or reset the boundary scan circuit. The TRST pin is equipped with an internal pull-up resistor. This pin functions as an I/O when the "Reserve JTAG Reset Pin" is not selected in Designer.

V_{CCI} Supply Voltage

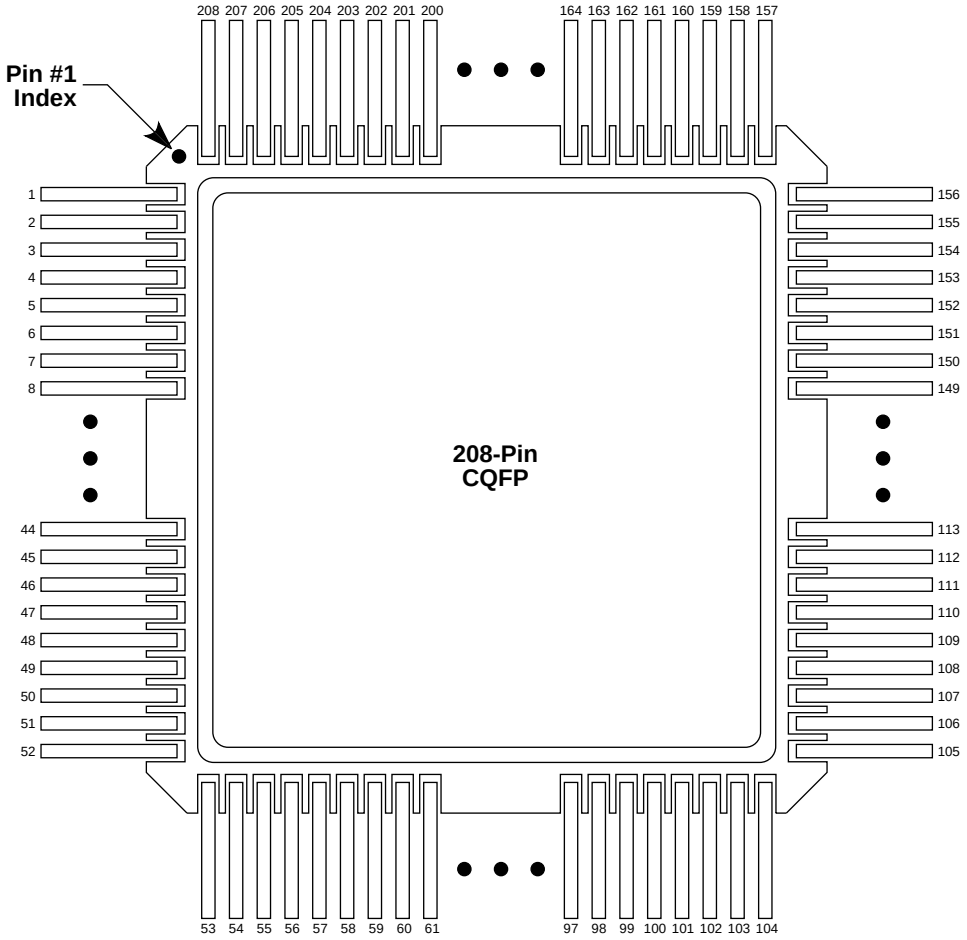
Supply voltage for I/Os. See Table 2 on page 10.

V_{CCA} Supply Voltage

Supply voltage for Array. See Table 2 on page 10.

Package Pin Assignments

208-Pin CQFP (Top View)



208-Pin CQFP

Pin Number	RT54SX32S Function	RT54SX72S Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	V_{CCI}	V_{CCI}
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	I/O
18	I/O	GND
19	I/O	V_{CCA}
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	NC	I/O
26	GND	GND
27	V_{CCA}	V_{CCA}
28	GND	GND
29	I/O	I/O
30	TRST	TRST
31	I/O	I/O
32	I/O	I/O
33	I/O	I/O
34	I/O	I/O
35	I/O	I/O
36	I/O	I/O
37	I/O	I/O
38	I/O	I/O
39	I/O	I/O
40	V_{CCI}	V_{CCI}
41	V_{CCA}	V_{CCA}
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	I/O	I/O
47	I/O	I/O
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	GND	GND
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	I/O
57	I/O	I/O
58	I/O	I/O
59	I/O	I/O
60	V_{CCI}	V_{CCI}
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	NC	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	I/O
74	I/O	QCLKA
75	I/O	I/O
76	PRB, I/O	PRB, I/O
77	GND	GND
78	V_{CCA}	V_{CCA}
79	GND	GND
80	NC	NC
81	I/O	I/O
82	HCLK	HCLK
83	I/O	V_{CCI}
84	I/O	QCLKB
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	I/O
90	I/O	I/O
91	I/O	I/O
92	I/O	I/O
93	I/O	I/O
94	I/O	I/O
95	I/O	I/O
96	I/O	I/O
97	I/O	I/O
98	V_{CCI}	V_{CCI}
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	TDO, I/O	TDO, I/O
104	I/O	I/O

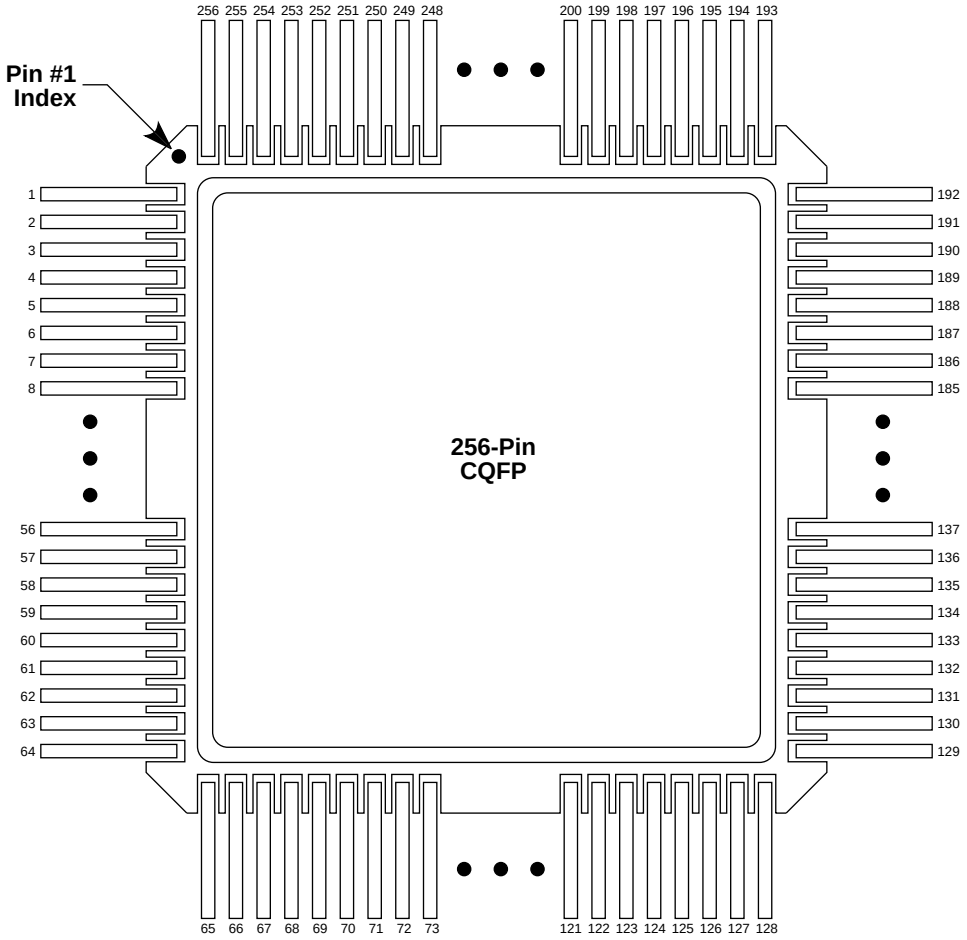
Note: *Pin 65 is a No Connect (NC) on Commercial A54SX32S-PQ208.*

208-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
105	GND	GND
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	I/O	I/O
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	V_{CCA}	V_{CCA}
115	V_{CCI}	V_{CCI}
116	I/O	GND
117	I/O	V_{CCA}
118	I/O	I/O
119	I/O	I/O
120	I/O	I/O
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	I/O	I/O
127	I/O	I/O
128	I/O	I/O
129	GND	GND
130	V_{CCA}	V_{CCA}
131	GND	GND
132	NC	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	I/O	I/O
142	I/O	I/O
143	I/O	I/O
144	I/O	I/O
145	V_{CCA}	V_{CCA}
146	GND	GND
147	I/O	I/O
148	V_{CCI}	V_{CCI}
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O
157	GND	GND
158	I/O	I/O
159	I/O	I/O
160	I/O	I/O
161	I/O	I/O
162	I/O	I/O
163	I/O	I/O
164	V_{CCI}	V_{CCI}
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	I/O	I/O
175	I/O	I/O
176	I/O	I/O
177	I/O	I/O
178	I/O	QCLKD
179	I/O	I/O
180	CLKA	CLKA
181	CLKB	CLKB
182	NC	NC
183	GND	GND
184	V_{CCA}	V_{CCA}
185	GND	GND
186	PRA, I/O	PRA, I/O
187	I/O	V_{CCI}
188	I/O	I/O
189	I/O	I/O
190	I/O	QCLKC
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	V_{CCI}	V_{CCI}
202	I/O	I/O
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	TCK, I/O	TCK, I/O

Package Pin Assignments (continued)

256-Pin CQFP (Top View)



256-Pin CQFP

Pin Number	RT54SX32S Function	RT54SX72S Function
1	GND	GND
2	TDI, I/O	TDI, I/O
3	I/O	I/O
4	I/O	I/O
5	I/O	I/O
6	I/O	I/O
7	I/O	I/O
8	I/O	I/O
9	I/O	I/O
10	I/O	I/O
11	TMS	TMS
12	I/O	I/O
13	I/O	I/O
14	I/O	I/O
15	I/O	I/O
16	I/O	I/O
17	I/O	V_{CCI}
18	I/O	I/O
19	I/O	I/O
20	I/O	I/O
21	I/O	I/O
22	I/O	I/O
23	I/O	I/O
24	I/O	I/O
25	I/O	I/O
26	I/O	I/O
27	I/O	I/O
28	V_{CCI}	V_{CCI}
29	GND	GND
30	V_{CCA}	V_{CCA}
31	GND	GND
32	I/O	I/O
33	I/O	I/O
34	TRST	TRST
35	I/O	I/O
36	I/O	V_{CCA}
37	I/O	GND
38	I/O	I/O
39	I/O	I/O
40	I/O	I/O
41	I/O	I/O
42	I/O	I/O
43	I/O	I/O
44	I/O	I/O
45	I/O	I/O
46	V_{CCA}	V_{CCA}
47	I/O	V_{CCI}
48	I/O	I/O
49	I/O	I/O
50	I/O	I/O
51	I/O	I/O
52	I/O	I/O
53	I/O	I/O
54	I/O	I/O
55	I/O	I/O
56	I/O	GND
57	I/O	I/O
58	I/O	I/O
59	GND	GND
60	I/O	I/O
61	I/O	I/O
62	I/O	I/O
63	I/O	I/O
64	I/O	I/O
65	I/O	I/O
66	I/O	I/O
67	I/O	I/O
68	I/O	I/O
69	I/O	I/O
70	I/O	I/O
71	I/O	I/O
72	I/O	I/O
73	I/O	V_{CCI}
74	I/O	I/O
75	I/O	I/O
76	I/O	I/O
77	I/O	I/O
78	I/O	I/O
79	I/O	I/O
80	I/O	I/O
81	I/O	I/O
82	I/O	I/O
83	I/O	I/O
84	I/O	I/O
85	I/O	I/O
86	I/O	I/O
87	I/O	I/O
88	I/O	I/O
89	I/O	QCLKA
90	PRB, I/O	PRB, I/O
91	GND	GND
92	V_{CCI}	V_{CCI}
93	GND	GND
94	V_{CCA}	V_{CCA}
95	I/O	I/O
96	HCLK	HCLK
97	I/O	I/O
98	I/O	QCLKB
99	I/O	I/O
100	I/O	I/O
101	I/O	I/O
102	I/O	I/O
103	I/O	I/O
104	I/O	I/O

256-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
105	I/O	I/O
106	I/O	I/O
107	I/O	I/O
108	I/O	I/O
109	I/O	I/O
110	GND	GND
111	I/O	I/O
112	I/O	I/O
113	I/O	I/O
114	I/O	I/O
115	I/O	I/O
116	I/O	I/O
117	I/O	I/O
118	I/O	I/O
119	I/O	I/O
120	I/O	V_{CCI}
121	I/O	I/O
122	I/O	I/O
123	I/O	I/O
124	I/O	I/O
125	I/O	I/O
126	TDO, I/O	TDO, I/O
127	I/O	I/O
128	GND	GND
129	I/O	I/O
130	I/O	I/O
131	I/O	I/O
132	I/O	I/O
133	I/O	I/O
134	I/O	I/O
135	I/O	I/O
136	I/O	I/O
137	I/O	I/O
138	I/O	I/O
139	I/O	I/O
140	I/O	I/O
141	V_{CCA}	V_{CCA}
142	I/O	V_{CCI}
143	I/O	GND
144	I/O	V_{CCA}
145	I/O	I/O
146	I/O	I/O
147	I/O	I/O
148	I/O	I/O
149	I/O	I/O
150	I/O	I/O
151	I/O	I/O
152	I/O	I/O
153	I/O	I/O
154	I/O	I/O
155	I/O	I/O
156	I/O	I/O

Pin Number	RT54SX32S Function	RT54SX72S Function
157	I/O	I/O
158	GND	GND
159	NC	NC
160	GND	GND
161	V_{CCI}	V_{CCI}
162	I/O	V_{CCA}
163	I/O	I/O
164	I/O	I/O
165	I/O	I/O
166	I/O	I/O
167	I/O	I/O
168	I/O	I/O
169	I/O	I/O
170	I/O	I/O
171	I/O	I/O
172	I/O	I/O
173	I/O	I/O
174	V_{CCA}	V_{CCA}
175	GND	GND
176	GND	GND
177	I/O	I/O
178	I/O	I/O
179	I/O	I/O
180	I/O	I/O
181	I/O	I/O
182	I/O	I/O
183	I/O	V_{CCI}
184	I/O	I/O
185	I/O	I/O
186	I/O	I/O
187	I/O	I/O
188	I/O	I/O
189	GND	GND
190	I/O	I/O
191	I/O	I/O
192	I/O	I/O
193	I/O	I/O
194	I/O	I/O
195	I/O	I/O
196	I/O	I/O
197	I/O	I/O
198	I/O	I/O
199	I/O	I/O
200	I/O	I/O
201	I/O	I/O
202	I/O	V_{CCI}
203	I/O	I/O
204	I/O	I/O
205	I/O	I/O
206	I/O	I/O
207	I/O	I/O
208	I/O	I/O

256-Pin CQFP (continued)

Pin Number	RT54SX32S Function	RT54SX72S Function
209	I/O	I/O
210	I/O	I/O
211	I/O	I/O
212	I/O	I/O
213	I/O	I/O
214	I/O	I/O
215	I/O	I/O
216	I/O	I/O
217	I/O	I/O
218	I/O	QCLKD
219	CLKA	CLKA
220	CLKB	CLKB
221	V_{CCI}	V_{CCI}
222	GND	GND
223	NC	NC
224	GND	GND
225	PRA, I/O	PRA, I/O
226	I/O	I/O
227	I/O	I/O
228	I/O	V_{CCA}
229	I/O	I/O
230	I/O	I/O
231	I/O	QCLKC
232	I/O	I/O

Pin Number	RT54SX32S Function	RT54SX72S Function
233	I/O	I/O
234	I/O	I/O
235	I/O	I/O
236	I/O	I/O
237	I/O	I/O
238	I/O	I/O
239	I/O	I/O
240	GND	GND
241	I/O	I/O
242	I/O	I/O
243	I/O	I/O
244	I/O	I/O
245	I/O	I/O
246	I/O	I/O
247	I/O	I/O
248	I/O	I/O
249	I/O	V_{CCI}
250	I/O	I/O
251	I/O	I/O
252	I/O	I/O
253	I/O	I/O
254	I/O	I/O
255	I/O	I/O
256	TCK, I/O	TCK, I/O

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v6.0)	Page
Advanced v0.1.1	The TRSTB pin was incorrectly named and changed to TRST.	All
	In the "RT54SX-S Product Profile" section on page 1, the User I/Os have changed.	1
	In the "Ceramic Device Resources" section on page 2, the User I/Os have changed.	2
	The Clock Networks section has changed to "Clock Resources" section on page 8.	8
	The "TRST pin" section on page 10 has changed.	10
	The"Design Considerations" section on page 11 Design Considerations section has changed.	11
	In the "2.5V/3.3V/5.0V Operating Conditions" section on page 12 section, the "Absolute Maximum Ratings[1]" section on page 12 changed. The I_{IO} row containing the I/O Source Sink Current was deleted.	12
	Equation 2 in the "Power Dissipation" section on page 15 was corrected.	15
	Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as "Advanced" or Preliminary" data sheets. The definition of these categories are as follows:

Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

The data sheet contains information that is considered to be final.

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