RM3182A

ARINC 429 Differential Line Driver

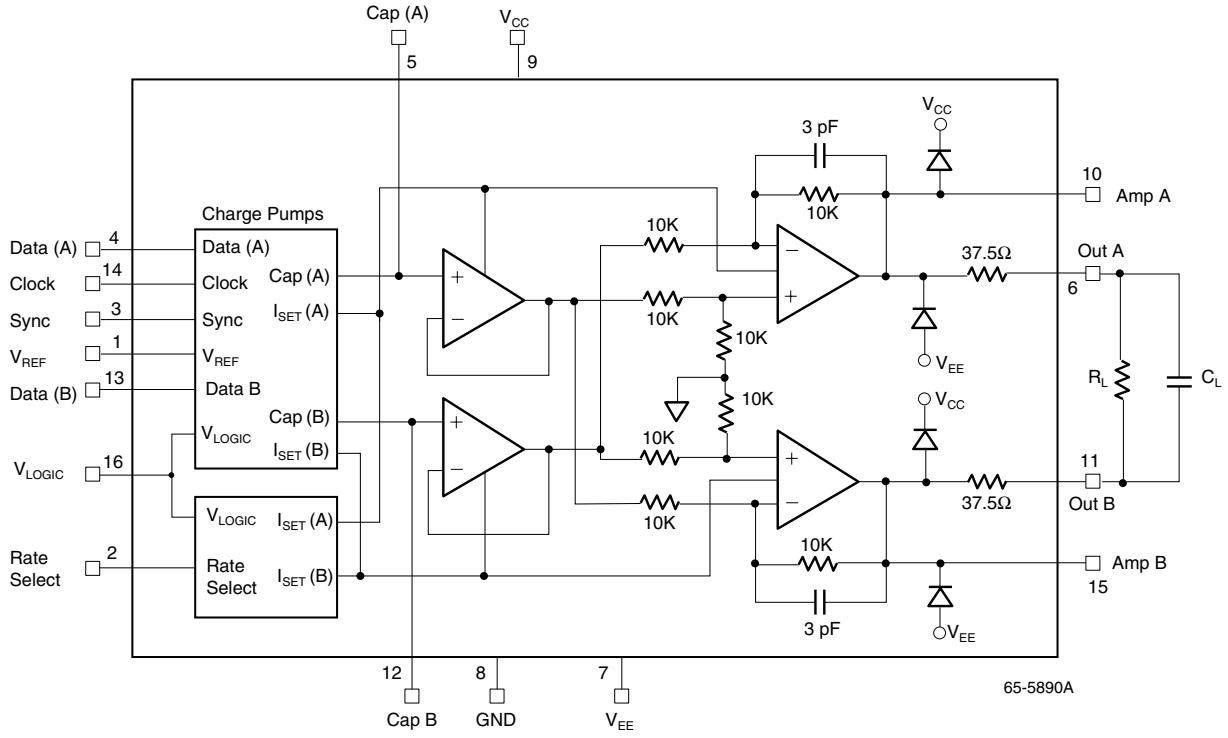
Features

- Adjustable rise and fall times
- Low supply current
- Capable of driving 30 nF ‖ 400Ω
- Digitally selectable 12.5 or 100 kbit/sec data rate
- Adjustable output voltages swing
- Output overvoltage protected
- Short circuit protected
- TTL and CMOS compatible inputs
- Available in 16-lead ceramic sidebrazed DIP

Description

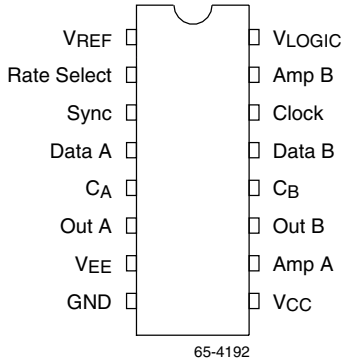
The RM3182A is a complete differential line driver IC. When Data A = Data B or Sync or Clock Signal is low, the driver forces the output to a Voltage Null level (0V ± 250 mV). Designed to address the ARINC 429 standard, the RM3182A has output rise and fall times that can be adjusted by the selection of an external capacitor (C_A or C_B) and an output voltage range adjustable through an externally applied V_{REF} signal. All logic inputs and sync control inputs are TTL/CMOS compatible. The device is constructed on a monolithic IC using a junction-isolated bipolar process. Sputtered SiCr resistors in the internal bias circuitry provide for stable bias currents and a tighter tolerance of output impedance. The RM3182A is available in 16-lead ceramic sidebrazed DIP.

Block Diagram



Note: Pin numbers are for the DIP package.

Pin Assignments



Functional Description

The device contains three main functional blocks. The first block is a digital section used to decode the ARINC Clock, Synchronization, and Data inputs as shown in Block Diagram. This block takes these inputs and channels the data to the charge pump circuits. The logical relationship for these pins is presented in Table 1.

Table 1. I/O Truth Table

Sync	Clock	Data A	Data B	Out A	Out B	Comments
X	L	X	X	0V	0V	Null
L	X	X	X	0V	0V	Null
H	H	L	L	0V	0V	Null
H	H	L	H	-VREF	+VREF	Low
H	H	H	L	+VREF	-VREF	High
H	H	H	H	0V	0V	Null

The second functional block is a charge pump circuit that is used to control the output waveform and its timing characteristics. This is achieved through charging and discharging a capacitor with a known current. The capacitor is user selectable, and is connected between C_A or C_B pins and ground. A rate select pin (digital input) enables to set the rise and fall time. If this pin is tied to ground, the device functions in the high rate. This mode is recommended if the user does not have an application requiring data rate switching. In the table below, recommended capacitor values are given for each possible data combination.

Table 2. Rate Select Pin Truth Table

Rate Select	C_A C_B (pF)	10% to 90% RIse/Fall time (µS)	Data Rate (Kbits/sec)	Comments
Logic 0	56	1.5	100	High Rate
Logic 1	56	10	12-14.5	Low Rate
Logic 0	390	10	12-14.5	Low Rate
Logic 1	390	N/A	N/A	Not Used

The last functional block of the device consists of a voltage follower and a high power output differential amplifier. The voltage follower buffers the signals presented at the charge caps and presents the mirrored signal to the difference amplifier to drive the ARINC line. Two different outputs are available from the differential amplifiers: Amp A, Amp B, and Out A, Out B. The outputs Amp A and Amp B are the direct outputs of the power amplifier. The outputs Out A and Out B include 37.5Ω series resistors added to minimize bus reflections by matching the power amplifier's output impedance to the cable's impedance of 75Ω. Amp A and Amp B may be used to customize the output impedance of the device. These outputs can also be used to enhance the device's drive capability. For example, driving the standard 30 nF ‖ 400Ω load defined in the ARINC specifications (see output drive capability and capacitive loads for more details). All outputs are protected from voltage spikes with diodes connected between the output pins and the supply lines.

Output Drive Capability and Capacitive Loads

The Traditional Approach

The RM3182A is capable of driving a high capacitive/resistive load. If complete ARINC compliance is required then Out A and Out B pins are recommended to maintain the output impedance. In this configuration, driving the full ARINC load of 30nF ‖ 400Ω the output characteristic takes on the transfer function of a low pass filter due to the internal 37.5Ω resistor, the line resistance and the capacitance associated with the cable. This will result in a lower rise/fall time of the device. Equation 1.1 relates the output voltage at Out A and Out B to the voltage at the power amplifier's output. Output A is taken for this example:

$$1.1 \qquad \text{Out A} = \frac{\text{AmpA}\, Z_L/2}{(Z_L/2) + R_{OUT}}$$

Where: $R_{OUT} = 37.5\Omega$ and $Z_L = R_L \parallel C_L$

The output as a function of frequency is given by equation 1.2.

$$1.2 \quad A_{OUT}(j\omega) = \text{Amp A}(j\omega)\left[\frac{R_L}{R_L + 2R_{OUT}(1 + j\omega C_L R_L)}\right]$$

Using equation 1.2, a time constant can be determined for the given application which is shown in equation 1.3.

$$1.3 \qquad \tau = (R_{OUT} \parallel R_L)C_L$$

So, for the maximum loading condition of 30nF ‖ 400Ω the resulting time constant is 1.9 μs. This shows that with a maximum load, the output waveform is greatly affected by the low pass filter combinabon of the $R_{OUT} \parallel R_L$ resistor and the load capacitance.

A New Option: Amp A/Amp B

The RM3182A also provides the user the option of connecting the data line directly to the power output amplifiers thus bypassing the internal 37.5Ω resistance of the device and matching the line more precisely. For example, using a 1% 37.5Ω resistor allows better control of the output impedance. By applying the load directly to the power amplifiers output pins, the resulting waveform is virtually unchanged when driving other loads. There may be applications where these pins present a more desirable result. For instance, if the line that the chip is driving is short, then the parasitic components of the line can be neglected, and power amplifier can be tied directly to the lines. This option can be utilized to achieve a greater noise immunity through bypassing the internal resistors.

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
Supply Voltage (V_{CC} to V_{EE})		+36	V
V_{LOGIC} Theshold Voltage		+7	V
V_{REF} Voltage		$+V_{CC}$	V
Logic Input Voltage	-0.3	V_{LOGIC} + 0.3	V
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	°C
Junction Temperature	-55	+175	°C
Lead Soldering Temperature (60 sec.)		+300	°C

Thermal Characteristics

(Still air, soldered into PC board)

Parameter	16-Lead Sidebrazed DIP
Maximum Junction Temperature	+175°C
Thermal Resistance, θ_{JC}	70°C/W
Thermal Resistance, θ_{JA}	28°C/W(1)
For T_A > 50°C Derate at	14.3 mW/°C

Electrical Characteristics

(V_{CC} = +15V, V_{EE} = -15V, V_{REF} = +5V, V_{LOGIC} = +5V, Rate Select = 0V, R_L = Open Circuit, C_L = 0 pF, and -55°C < T_A < +125°C)

Symbol	Parameters	Test Conditlons	Min.	Typ.	Max.	Units
I_{CC}	Positive Supply Current	Data Rate = 0 to 100 Kbits/sec	4.0	5.7	6.9	mA
I_{EE}	Negative Supply Current	Data Rate = 0 to 100 Kbits/sec	4.0	4.9	6.9	mA
I_{LOGIC}	V_{LOGIC} Supply Current	Data Rate = 0 to 100 Kbits/sec	150	214	300	µA
I_{REF}	V_{REF} Supply Current	Data Rate = 0 to 100 Kbits/sec	-500	-294	-100	µA
V_{IH}	Input Logic Level High	Dependent on V_{LOGIC}	2.0		Vlogic	V
V_{IL}	Input Logic Level Low				0.5	V
V_{OH}	Output Voltage High	With Respect to Ground	4.75	5.0	5.25	V
V_{OL}	Output Voltage Low	With Respect to Ground	-5.25	-5.0	-4.75	V
V_{NULL}	Output Voltage Null	Both Data Inputs = Logic 0	-250	0	+250	mV
I_{IH}	Input Current High	V_{IN} = 2.0V			1	µA
I_{IL}	Input Current Low	V_{IN} = 0.5V	-645	-161	-50	nA
C_I[1]	Input Capacitance				15	pF
I_{SC}	Output Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line to line or to GND	100	133	156	mA
I_{SCVCC}	V_{CC} Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line to line or to GND		140	165	mA
I_{SCVEE}	V_{EE} Short Circuit Current	A_{OUT} and/or B_{OUT} shorted line to line or to GND		140	165	mA

Note:

1. Guaranteed by design.

Typical Power Dissipation Characteristics

(V_{CC} = +15V, V_{EE} = -15V, V_{REF} = +5V, T_A = + 25°C, C_A = C_B = 56pF)

Data Rate (Kbits/sec)	Load	Rate Select	Positive Supply Current	Negative Supply Current	Pin V_{LOGIC} Supply Current	Total Power Dissipatlon
0 - 100	Open Circuit	Logic 1,0	5.7 mA	4.9 mA	214 µA	160 mW
12.5 - 14	Full Load[1]	Logic 1	19.6 mA	22.7 mA	200 µA	655 mW
100	Full Load[1]	Logic 0	39.1 mA	38.4 mA	200 µA	1165 mW

Note:

1. R_L = 400Ω, C_L = 0.03 µF (see Block Diagram).

Typical Performance Characteristics

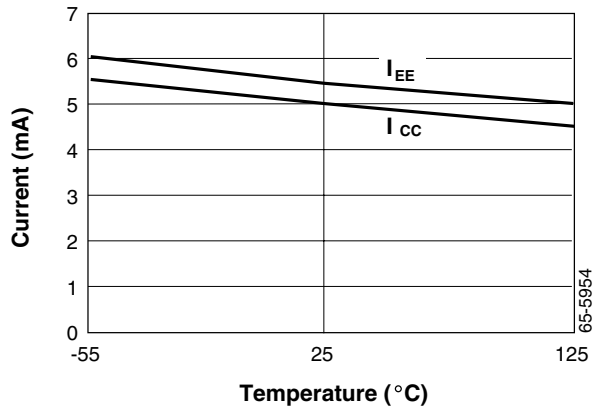


Figure 1. Supply Current vs. Temperature (C_L = 0 pF, R_L = Open Circuit)

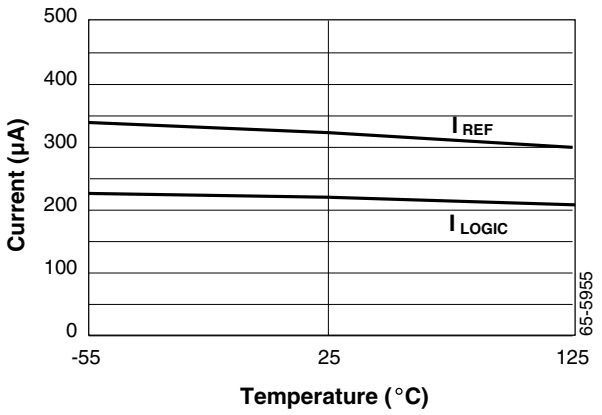


Figure 2. I_{REF}, I_{LOGIC} vs. Temperature

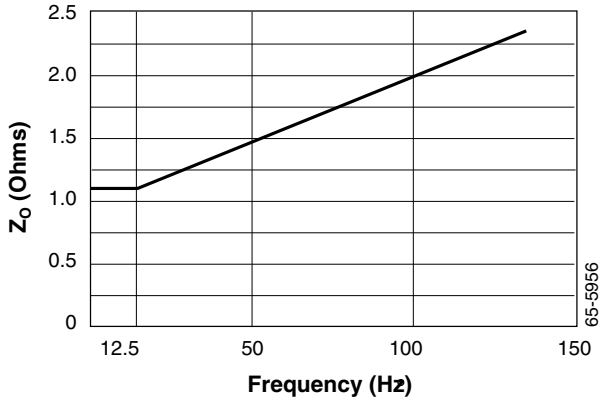


Figure 3. AmpA, AmpB Output Impedance Typical

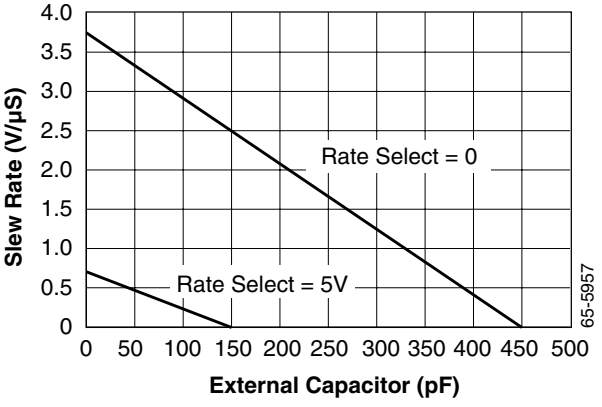


Figure 4. Slew Rate vs. C_A, C_B

Applications

Heat Sinking /Air Flow and Short Circuit Protection

The user application will determine if and how much heat sinking/air flow will be required for the RM3182A. Consideration must be given to ambient temperature, load conditions and output voltage swing. In addition, power consumption increases with increased operating frequency. Use the numbers given in the Thermal Characteristics Table to determine that the maximum allowable junction temperature of 175°C is not exceeded.

Outputs Out A and Out B are short circuit protected by the internal 37.5Ω back termination resistors. During a short circuit of the output to either power supply or ground, the device must be able to dissipate the generated heat. For example, if the output is shorted to ground and V_{CC} = +15V, the device must dissipate 15V x 0.165A = 2.5W. An appropriate heat sink is required in this situation.

Note that the Amp A and Amp B outputs are not short circuit protected. Shorting these pins to either power supply or ground will cause failure of the device. An added external resistor will protect the circuit by limiting the current.

Power Supply Considerations

Three power supplies are required to operate the RM3182A in a typical ARINC 429 bus application: +15V for V_{CC}, -15V for V_{EE}, and +5V for both V_{REF} and V_{LOGIC}. The differential output swing of the RM3182A is equal to 2 x V_{REF}. Using +5V gives a differential output swing of 10V. If a different output voltage swing is required, an additional power supply is needed to set V_{LOGIC}.

Each power supply pin should be decoupled to ground using a high quality 10 μF tantalum capacitor. This is especially true when driving a large capacitive or resistive loads. The decoupling capacitors should be located as close to the device pins as possible to eliminate the wiring inductance.

Typical ARINC 429 Application

Figure 5 shows typical switching waveform for the RM3182A in any configuration.

Figure 6 depicts connections for a ARINC 429 high speed bus driver application. This circuit shows the complete configuration for a 100 Kbits/sec, 10V differential output swing using the terminated output pins.

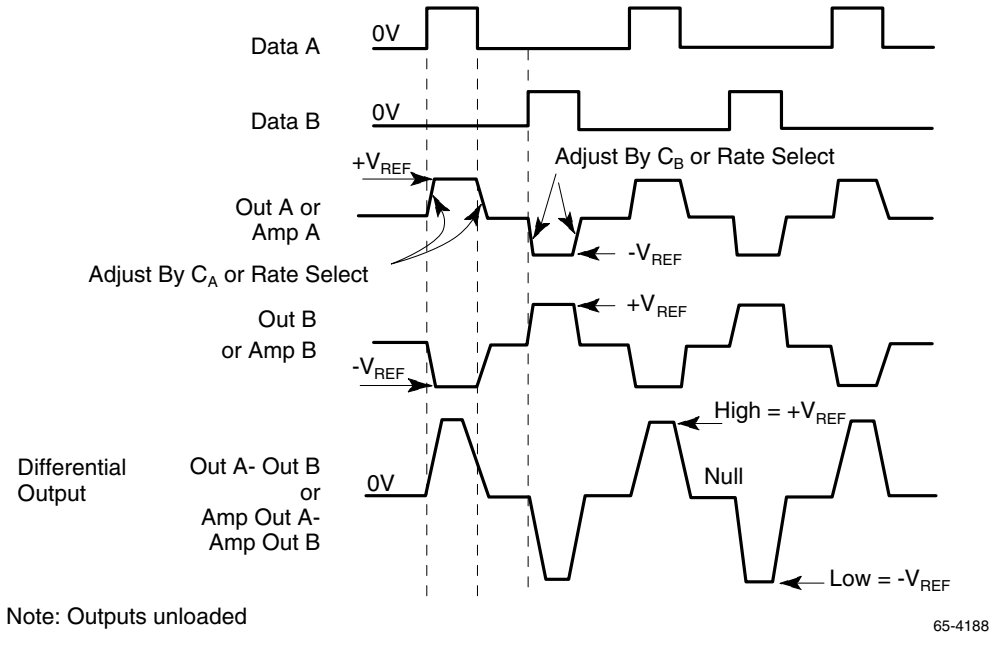


Figure 5. Switching Waveforms

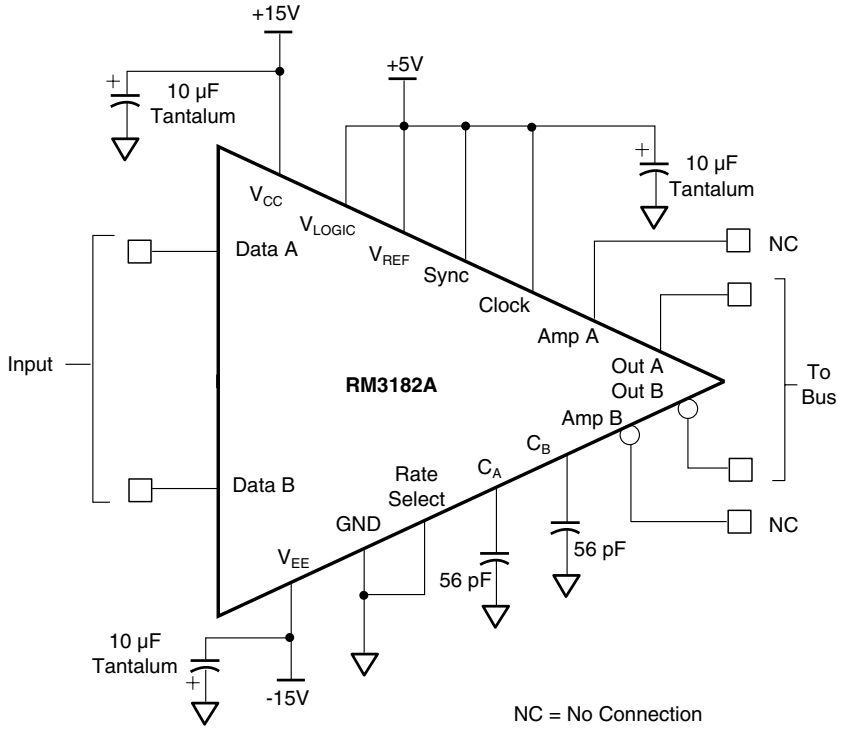


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Figure 6. ARINC 429 Bus Driver Applications (100 kb/s Mode)

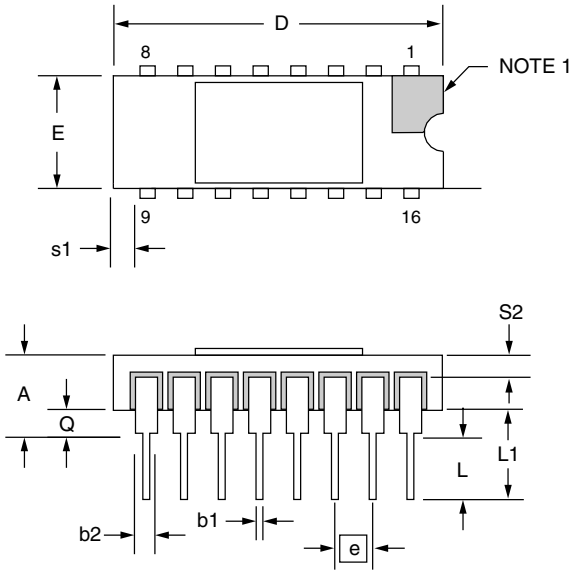
Mechanical Dimensions

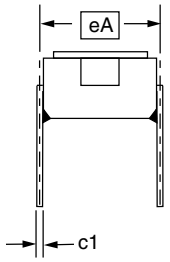
16-Lead SideBraze Ceramic DIP

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.200	—	5.08	
b1	.014	.023	.36	.58	7
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	7
D	—	.860	—	21.84	
E	.280	.310	7.11	7.87	
e	.100 BSC		2.54 BSC		4, 8
eA	.300 BSC		7.62 BSC		6
L	.125	.200	3.18	5.08	
L1	.140	—	3.56	—	
Q	.015	.070	.38	1.78	3
s1	.005	—	.13	—	5
s2	.005	—	.13	—	

Notes:

1. Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
3. Dimension "Q" shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
5. Applies to all four corners (leads number 1, 8, 9, and 16).
6. "eA" shall be measured at the centerline of the leads.
7. All leads – Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
8. Fourteen spaces.





Ordering Information

Part Number	Package	Operating Temperature Range
RM3182AS	16-Lead Sidebraze Ceramic DIP	-55°C to +125°C