

LSI Computer Systems, Inc. 1235 Walt Whitman Road, Melville, NY 11747 (516) 271-0400 FAX (516) 271-0405

COMPLEMENTARY MOS (CMOS) DIVIDER

RED SERIES

RED 5/6
RED 50/60
RED 100/120
RED 300/360
RED 500/600
RED 3000/3600
Divide by 50 or 60
Divide by 100 or 120
Divide by 300 or 360
Divide by 500 or 600
Divide by 3000 or 3600
Divide by 3000 or 3600

FEATURES:

- Clock input pulse shaper accepts 50 Hz/60 Hz sine wave directly
- Fully static counter operation
- +4.5V to +15 V operation (VDD-VSS)
- · Low power dissipation
- High noise immunity
- Reset
- Input Enable
- 50/Hz/60 Hz division select input
- Output low power TTL compatible at +4.5V operation
- Square Wave Output (except for ÷ 5)
- 8 Pin DIP (See Figure 1)

APPLICATION:

Time base generator from either 50 Hz or 60 Hz line frequency to produce:

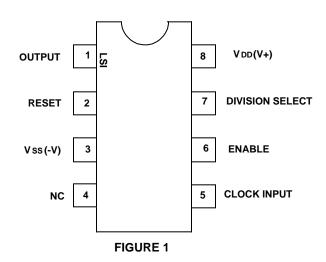
10 pulses per second	(RED 5/6)
1 pulse per second	(RED 50/60)
1 pulse per 2 seconds	(RED 100/120)
1 pulse per .1 minute	(RED 300/360)
1 pulse per 10 seconds	(RED 500/600)
1 pulse per minute	(RED 3000/3600)

DESCRIPTION OF OPERATION:

The counter advances by one on each negative transition of the input clock pulse as long as the Enable signal is "High" and the Reset signal is "Low". When the Enable signal is "Low" the input clock pulses will be inhibited and the counter will be held at the state it was in prior to bringing the Enable "Low". A "High" Reset signal clears the counter to zero count.

Depending on the device used, a "Low" on the Division Select input will cause a Divide by 6, 60, 120, 360, 600 or 3600. A "High" on the Division Select will cause a Divide by 5, 50, 100, 300, 500 or 3000.

PIN ASSIGNMENT - TOP VIEW STANDARD 8 PIN PLASTIC DIP



MARKING AS FOLLOWS: PART MARKING

RED 5/6	RED 6
RED 50/60	RED 60
RED 100/120	RED 120
RED 300/360	RED 360
RED 500/600	RED 600
RED 3000/3600	RED 3600

MAXIMUM RATINGS:

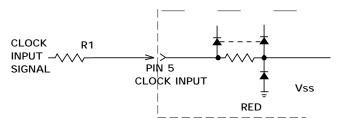
PARAMETER	SYMBOL	VALUE	UNIT
Storage Temperature	Tstg	-65 to +150	°C
Operating Temperature	TA	-40 to +85	°C
DC Supply Voltage	(VDD-VSS)	+18	Volts
Voltage at any input	VIN	Vss5 to VDD +.5	Volts
- ' '			

The information included herein is believed to be accurate and reliable. However, LSI Computer Systems, Inc. assumes no responsibilities for inaccuracies, nor for any infringements of patent rights of others which may result from its use.

TEST CONDITIONS: Vss = OV						VDD	MIN	MAX	UNITS
Output Capacitance Load = 15 pF		Input Capacitance:	(Any lı	nput)	5	pF			
Input Rise and	Fall ti	mes = 2	20 ns,		Clock Rise and Fall Time:	5V	No Ma	aximum L	_imit
except clock Rise and Fall times			10V	No Maximum Limit					
•					Clock Frequency:	5V	DC	600	KHz
	VDD	Min	Max	Units		10V	DC	1200	KHz
Quiescent Device Current	5V		10	uA	Input Clock Pulse Width:	5V		800	ns
	10V		20	uA		10V		400	ns
Output Voltage, Low Level:	5V		0.0	Volts	Output Rise and Fall Time:	5V		225	ns
	10V		0.0	Volts		10V		150	ns
High Level:	5V	4.99		Volts	Propagation Delay to Output:	5V		1500	ns
	10V	9.99		Volts		10V		750	ns
Clock Input Voltage, Low Level:	5V		1	Volts	Enable Set-up Time:	5V		300	ns
	10V		2	Volts		10V		150	ns
High Level:	5V	4		Volts	Reset Pulse Width:	5V		800	ns
	10V	8		Volts		10V		400	ns
Input Noise Immunity(except clock):	5V	1.5		Volts	Reset Removal Time:	5V		1200	ns
(Low and High)	10V	3.0		Volts		10V		600	ns
Output Drive Current:					Reset Propagation Delay				
FullN Channel Sink Current:	4.5V	0.18		mA	to Output:	5V		1400	ns
Temp. (Vout - Vss +.4V)	10V	0.45		mA		10V		700	ns
Range									
P Channel Source Current	: 4.5V	0.3		mA					
(Vout = VDD - 1V)	10V	0.75		mA					

ENABLE SIGNAL TIMING CONSIDERATION

If the Enable signal switches Low during a positive clock phase and then switches High during a negative clock phase, a false count will be registered. To prevent this from happening, the Enable signal should not switch Low during a positive clock phase unless the switch to High also occurs during a positive clock phase. The Enable signal should normally be switched during a netative clock phase.



TYPICAL CLOCK INPUT

If input signals are less than the Vss or greater than VDD, series input resistor, R1, should be used to limit the maximum input current to 2 milliamperes.

