

# Switching (250V, 8A)

## RDN080N25

### ●Features

- 1) Low on-resistance.
- 2) Low input capacitance.
- 3) Excellent resistance to damage from static electricity.

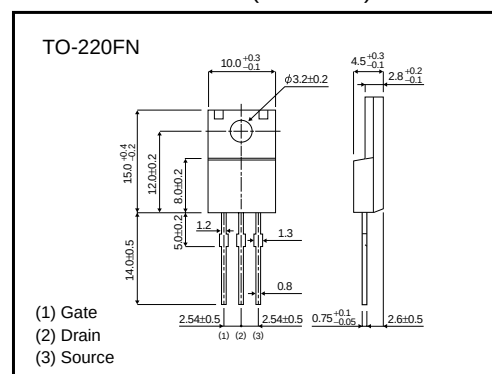
### ●Application

Switching

### ●Structure

Silicon N-channel  
MOS FET

### ●External dimensions (Units : mm)



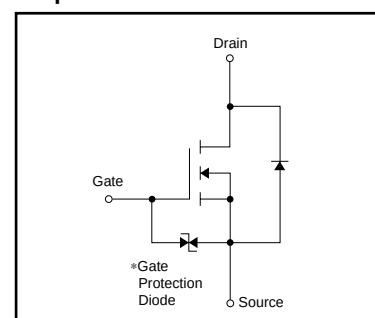
### ●Absolute maximum ratings (Ta=25°C)

| Parameter                         | Symbol      | Limits       | Unit |
|-----------------------------------|-------------|--------------|------|
| Drain-Source Voltage              | $V_{DS}$    | 250          | V    |
| Gate-Source Voltage               | $V_{GS}$    | $\pm 30$     | V    |
| Drain Current                     | Continuous  | $I_D$        | 8    |
|                                   | Pulsed      | $I_{DP}$ *1  | 32   |
| Reverse Drain Current             | Continuous  | $I_{DR}$     | 8    |
|                                   | Pulsed      | $I_{DRP}$ *1 | 32   |
| Avalanche Current                 | $I_{AS}$ *2 | 8            | A    |
| Avalanche Energy                  | $E_{AS}$ *2 | 136          | mJ   |
| Total Power Dissipation (Tc=25°C) | $P_D$       | 35           | W    |
| Channel Temperature               | $T_{ch}$    | 150          | °C   |
| Storage Temperature               | $T_{stg}$   | -55 to +150  | °C   |

\*1  $P_w \leq 10\mu s$ , Duty cycle  $\leq 1\%$

\*2  $L = 4.5mH$ ,  $V_{DS}=50V$ ,  $R_G=25\Omega$ , 1Pulse,  $T_{ch}=25^\circ C$

### ●Equivalent Circuit



\*A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use. Use the protection circuit when the fixed voltages are exceeded.

| Parameter                               | Symbol                | Min. | Typ. | Max. | Unit | Conditions                                                      |
|-----------------------------------------|-----------------------|------|------|------|------|-----------------------------------------------------------------|
| Gate-Source Leakage                     | I <sub>GSS</sub>      | —    | —    | ±10  | μA   | V <sub>GS</sub> =±30V, V <sub>DS</sub> =0V                      |
| Drain-Source Breakdown Voltage          | V <sub>(BR)</sub> DSS | 250  | —    | —    | V    | I <sub>D</sub> =250μA, V <sub>GS</sub> =0V                      |
| Zero Gate Voltage Drain Current         | I <sub>DSS</sub>      | —    | —    | 25   | μA   | V <sub>DS</sub> =250V, V <sub>GS</sub> =0V                      |
| Gate Threshold Voltage                  | V <sub>GS</sub> (th)  | 2.0  | —    | 4.0  | V    | V <sub>DS</sub> =10V, I <sub>D</sub> =1mA                       |
| Static Drain-Source On-State Resistance | R <sub>DS</sub> (on)  | —    | 0.38 | 0.5  | Ω    | I <sub>D</sub> =4A, V <sub>GS</sub> =10V                        |
| Forward Transfer Admittance             | Y <sub>fs</sub>       | 1.9  | 3.1  | —    | S    | V <sub>DS</sub> =10V, I <sub>D</sub> =4.0A                      |
| Input Capacitance                       | C <sub>iss</sub>      | —    | 543  | —    | pF   | V <sub>DS</sub> =10V                                            |
| Output Capacitance                      | C <sub>oss</sub>      | —    | 193  | —    | pF   | V <sub>GS</sub> =0V                                             |
| Reverse Transfer Capacitance            | C <sub>rss</sub>      | —    | 64   | —    | pF   | f=1MHz                                                          |
| Turn-On Delay Time                      | t <sub>d</sub> (on)   | —    | 13   | —    | ns   | I <sub>D</sub> =4.0A, V <sub>DD</sub> ≐ 100V                    |
| Rise Time                               | t <sub>r</sub>        | —    | 25   | —    | ns   | V <sub>GS</sub> =10V                                            |
| Turn-Off Delay Time                     | t <sub>d</sub> (off)  | —    | 38   | —    | ns   | R <sub>L</sub> =25Ω                                             |
| Fall Time                               | t <sub>f</sub>        | —    | 26   | —    | ns   | R <sub>GS</sub> =10Ω                                            |
| Reverse Recovery Time                   | t <sub>rr</sub>       | —    | 151  | —    | ns   | I <sub>DR</sub> =8A, V <sub>GS</sub> =0V                        |
| Reverse Recovery Charge                 | Q <sub>rr</sub>       | —    | 0.63 | —    | μC   | di / dt=100A / μs                                               |
| Total Gate Charge                       | Q <sub>g</sub>        | —    | 15   | —    | nC   | V <sub>DD</sub> =125V, V <sub>GS</sub> =10V, I <sub>D</sub> =8A |

Graph showing Gate Threshold Voltage ( $V_{th}$ ) versus Channel Temperature ( $T_{ch}$ ) for the 74VHC00. The conditions are  $V_{DD}=10V$  and  $I_{DD}=1mA$ .

| Channel Temperature ( $T_{ch}$ ) (°C) | Gate Threshold Voltage ( $V_{th}$ ) (mV) |
|---------------------------------------|------------------------------------------|
| -25                                   | 3.2                                      |
| 125                                   | 2.4                                      |

Figure 10 is a log-log plot showing the Static Drain-Source On-State Resistance ( $R_{DS(on)}$ ) in Ohms ( $\Omega$ ) versus Drain Current ( $I_D$ ) in Amperes (A) for the 2N7000 MOSFET. The y-axis ranges from 0.1 to 10  $\Omega$ , and the x-axis ranges from 0.01 to 100 A. The graph includes four curves for different temperatures:  $T_a = -25^\circ\text{C}$ ,  $T_a = 25^\circ\text{C}$ ,  $T_a = 75^\circ\text{C}$ , and  $T_a = 125^\circ\text{C}$ . The curves show that  $R_{DS(on)}$  decreases as  $I_D$  increases and as temperature decreases. A note specifies  $V_{GS} = 10\text{V}$  Pulsed.

Figure 10 is a graph showing the Static Drain-Source On-State Resistance ( $R_{DS(on)}$ ) in  $\Omega$  versus the Gate-Source Voltage ( $V_{GS}$ ) in V for the 2N7000 MOSFET. The graph is for pulsed operation at  $T_a = 25^\circ\text{C}$ . Two curves are shown for different drain currents:  $I_D = 8\text{A}$  and  $I_D = 4\text{A}$ . The resistance decreases sharply as  $V_{GS}$  increases from approximately 5.5V to 10V and then levels off. The resistance is higher for  $I_D = 8\text{A}$  than for  $I_D = 4\text{A}$ .

| $V_{GS}$ (V) | $R_{DS(on)}$ ( $\Omega$ ) at $I_D = 8\text{A}$ | $R_{DS(on)}$ ( $\Omega$ ) at $I_D = 4\text{A}$ |
|--------------|------------------------------------------------|------------------------------------------------|
| 5.5          | > 2.0                                          | > 2.0                                          |
| 6.0          | ~0.5                                           | ~0.4                                           |
| 10.0         | ~0.45                                          | ~0.35                                          |
| 15.0         | ~0.45                                          | ~0.35                                          |
| 20.0         | ~0.45                                          | ~0.35                                          |
| 25.0         | ~0.45                                          | ~0.35                                          |
| 30.0         | ~0.45                                          | ~0.35                                          |

**ROHM**

## Transistors

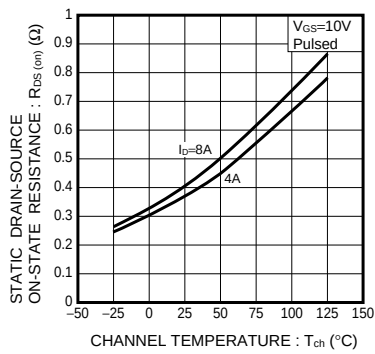


Fig.7 Static Drain-Source On-State Resistance vs. Channel Temperature

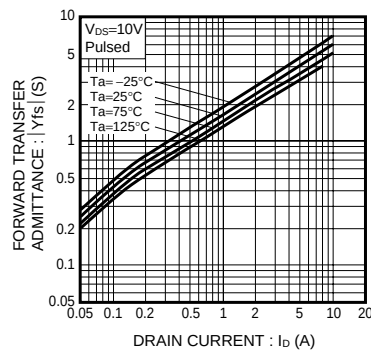


Fig.8 Forward Transfer Admittance vs. Drain Current

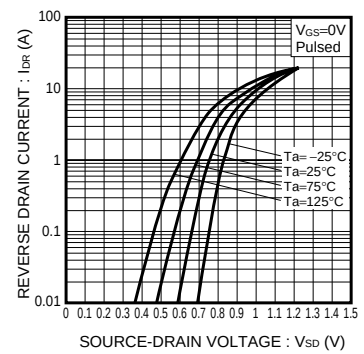


Fig.9 Reverse Drain Current vs. Source-Drain Voltage

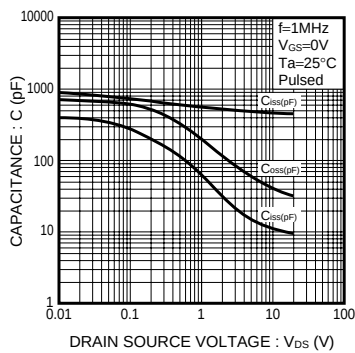


Fig.10 Typical Capacitance vs. Drain-Source Voltage

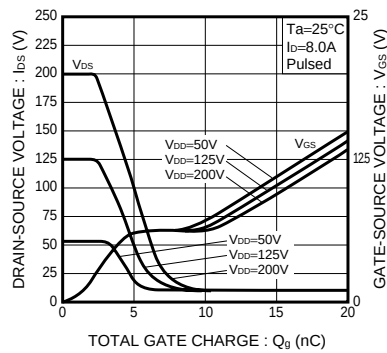


Fig.11 Dynamic Input Characteristics

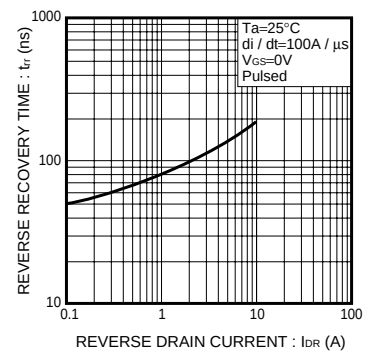


Fig.12 Reverse Recovery Time vs. Reverse Drain Current

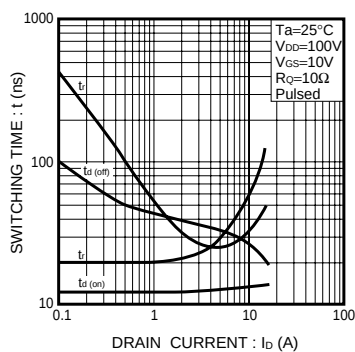


Fig.13 Switching Characteristics

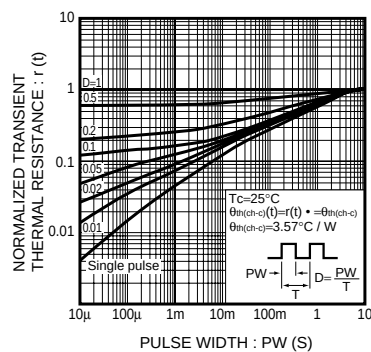


Fig.14 Normalized Transient Thermal Resistance vs. Pulse Width