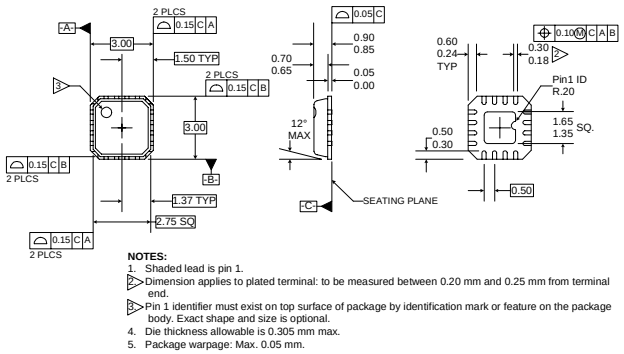
Typical Applications

- 3V 1850-1910MHz CDMA PCS Handsets
- Commercial and Consumer Systems
- Spread-Spectrum Systems

Product Description

The RF5154 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 3V CDMA hand-held digital equipment, spread-spectrum systems, and other applications in the 1850MHz to 1910MHz band. The device is packaged in a compact 3mmx3mm package. The device's frequency response can be optimized for linear performance in the 1850MHz to 1910MHz band. The RF5154 has a low power mode to extend battery life under low output power conditions.



NOTES:
1. Shaded lead is pin 1.
2. Dimension applies to plated terminal: to be measured between 0.20 mm and 0.25 mm from terminal end.
3. Pin 1 identifier must exist on top surface of package by identification mark or feature on the package body. Exact shape and size is optional.
4. Die thickness allowable is 0.305 mm max.
5. Package warpage: Max. 0.05 mm.

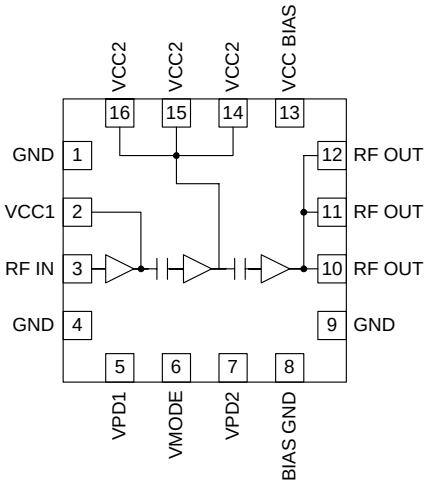
Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☐ GaInP/HBT
- ☐ GaN HEMT
- ☐ SiGe Bi-CMOS

Package Style: LCC, 16-Pin, 3x3

Features

- Single 3V Supply
- 29dBm Linear Output Power
- 30dB Linear Gain
- 35% Linear Efficiency CDMA
- On-Board Power Down Mode
- Low Power Mode



Functional Block Diagram

Ordering Information

RF5154	CDMA 1900MHz 3V Power Amplifier
RF5154 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7628 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

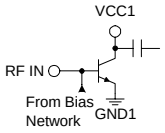
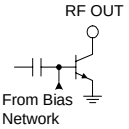
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤31dBm)	+4.5	V_{DC}
Mode Voltage (V_{MODE})	+3.5	V_{DC}
Control Voltage (V_{PD})	+3.5	V_{DC}
Input RF Power	+10	dBm
Operating Case Temperature	-30 to +110	℃
Storage Temperature	-30 to +150	℃

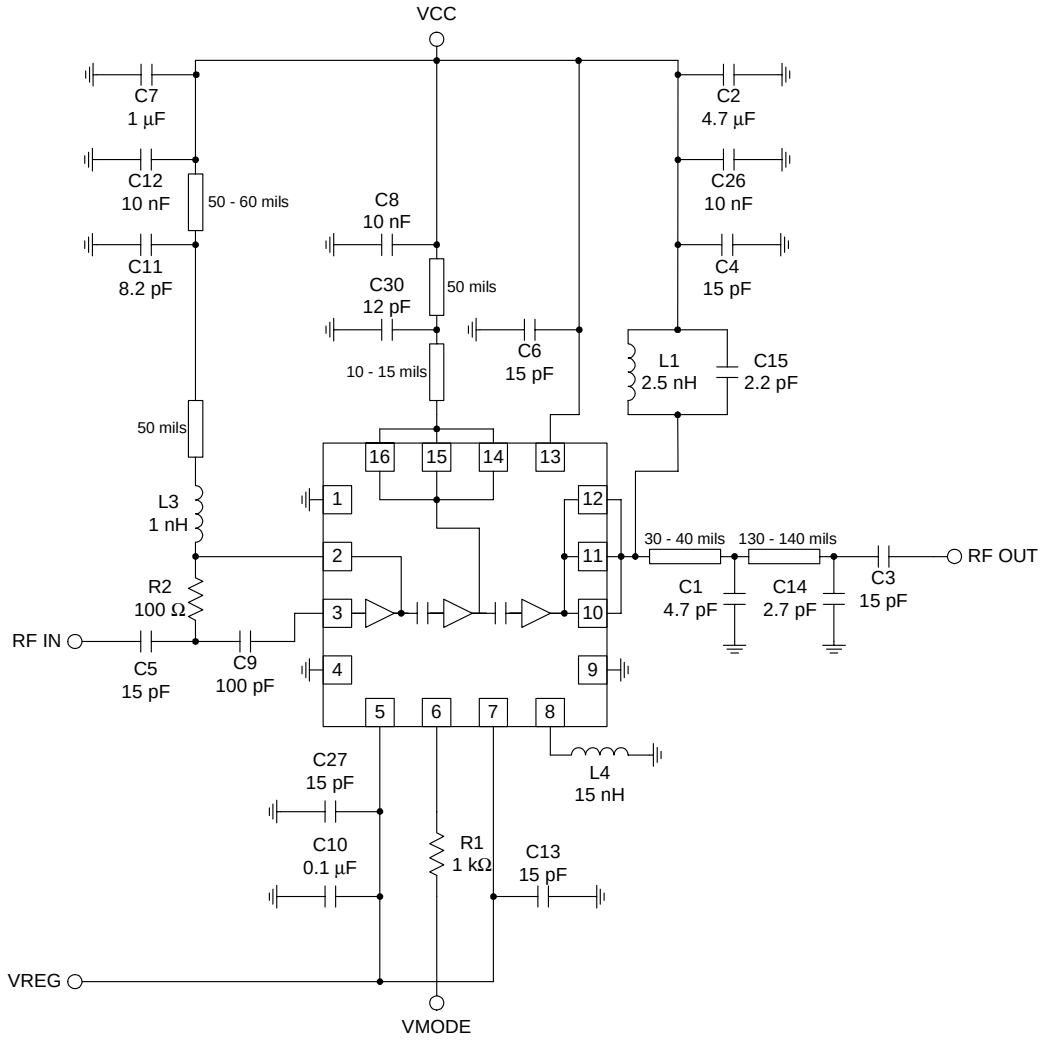
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
High Power State (V_{MODE} Low)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=0V to 0.5V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	27	30		dB	
Second Harmonic			-35	dBc	
Third Harmonic			-40	dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency		35		%	P_{OUT}=29dBm
Adjacent Channel Power Rejection		-46	-44	dBc	ACPR @ 1.25MHz
		-58	-56	dBc	ACPR @ 2.25MHz
Input VSWR		<2:1			
Output Load VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc
Noise Power		-135		dBm/Hz	At 80MHz offset.
Low Power State (V_{MODE} High)					Case T=25°C, V_{CC}=3.4V, V_{REG}=2.85V, V_{MODE}=1.8V to 3V, Freq=1850MHz to 1910MHz (unless otherwise specified)
Frequency Range	1850		1910	MHz	
Linear Gain	22	25	28	dB	For one device the low power state linear gain will always be lower than the high power state linear gain.
Second Harmonic			-35	dBc	
Third Harmonic			-40	dBc	
Maximum Linear Output Power (CDMA Modulation)	21			dBm	
Max I_{CC}		170	200	mA	P_{OUT}=+16dBm (all currents included)
Adjacent Channel Power Rejection		<-46	-44	dBc	ACPR @ 1.25MHz
		<-60	-56	dBc	ACPR @ 2.25MHz
Input VSWR		2:1			
Output Load VSWR			10:1		No damage.
			6:1		No oscillations. >-70dBc

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DC Supply					
Supply Voltage	3.0	3.4	4.2	V	
Quiescent Current	130	170	200	mA	V_{MODE}=Low
		60	80	mA	V_{MODE}=High
V_{REG} Current			10	mA	
V_{MODE} Current			1	mA	
Turn On/Off time			<40	µs	Time between V_{PD} turned on and part reaching full power.
Total Current (Power Down)			10	µA	V_{REG}=Low
V_{REG} "Low" Voltage	0		0.5	V	
V_{REG} "High" Voltage	2.75	2.85	2.95	V	
V_{MODE} "Low" Voltage	0		0.5	V	
V_{MODE} "High" Voltage	1.8		3.0	V	

Pin	Function	Description	Interface Schematic
1	GND		
2	VCC1	Power supply for first stage and interstage match. V_{CC} should be fed through a 1nH inductor terminated with a 8.2pF capacitor on the supply side.	
3	RF IN	RF input. An external 15pF series capacitor is required as a DC block and also provides for an input VSWR of <2:1 typical.	
4	GND1		
5	VPD1	Power Down control for first and second stages. When this pin is “low”, all first and second stage circuits are shut off. When this pin is 2.85V, all first stage circuits are operating normally. V_{PD1} requires a regulated 2.85V for the amplifier to operate properly over all specified temperature and voltage ranges. A 15pF high frequency bypass capacitor is recommended.	
6	VMODE	V_{MODE}=High is the Low Power mode V_{MODE}=Low is the High Power mode	
7	VPD2	Power Down control for the third stage. When this pin is “low”, the third stage circuit is shut off. When this pin is 2.85V, the third stage circuit is operating normally. V_{PD} requires a regulated 2.85V for the amplifier to operate properly over all specified temperature and voltage ranges. A 15pF high frequency bypass capacitor is recommended.	
8	BIAS GND	Requires a 15nH inductor.	
9	GND		
10	RF OUT	RF output and power supply for final stage. This is the unmatched collector output of the third stage. A DC block is required following the matching components. The biasing may be provided via a parallel L-C set for resonance at the operating frequency of 1850MHz to 1910MHz. It is important to select an inductor with very low DC resistance with a 1A current rating. Alternatively, shunt microstrip techniques are also applicable and provide very low DC resistance. Low frequency bypassing is required for stability.	
11	RF OUT	Same as pin 10.	
12	RF OUT	Same as pin 10.	
13	VCC BIAS	Supply for bias reference and control circuits. High frequency bypassing may be necessary.	
14	VCC2	Power supply for second stage and interstage match. Pins 14, 15 and 16 should be connected by a common trace where the pins contact the printed circuit board.	
15	VCC2	Same as pin 14.	
16	VCC2	Same as pin 14.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Evaluation Board Schematic
US - CDMA



Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.031”, Board Material FR-4, Multi-Layer, Ground Plane at 0.015”