RX3408 Low Power IF Receiver and PLL Frequency Synthesizer IC

Advance Information

Description

The RX3408 is a low power IF receiver suitable for use as the second IF downconverter in double conversion receiver systems and a serial data input, phase-locked loop IC with programmable input and reference frequency dividers. The RX3408 is well-suited for wireless FM applications and incorporates a quadrature FM demodulator, on-chip audio filter, and a squelch/mute circuit. When combined with a VCO, this IC becomes the core of a very low power frequency synthesizer well-suited for mobile communication applications, e.x. paging systems and family radio service (FRS). There are some features implemented in this IC, including an 18-bit programmable input frequency divider, a terminal for reference oscillator buffer output, as well as stand-by control through programming, and etc. Details are listed in the following.

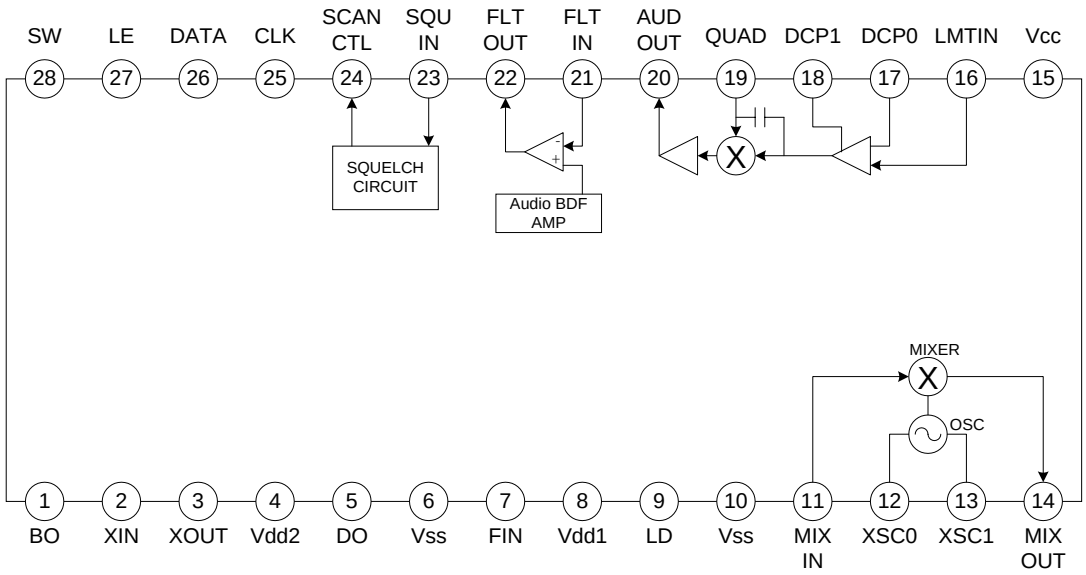
Features

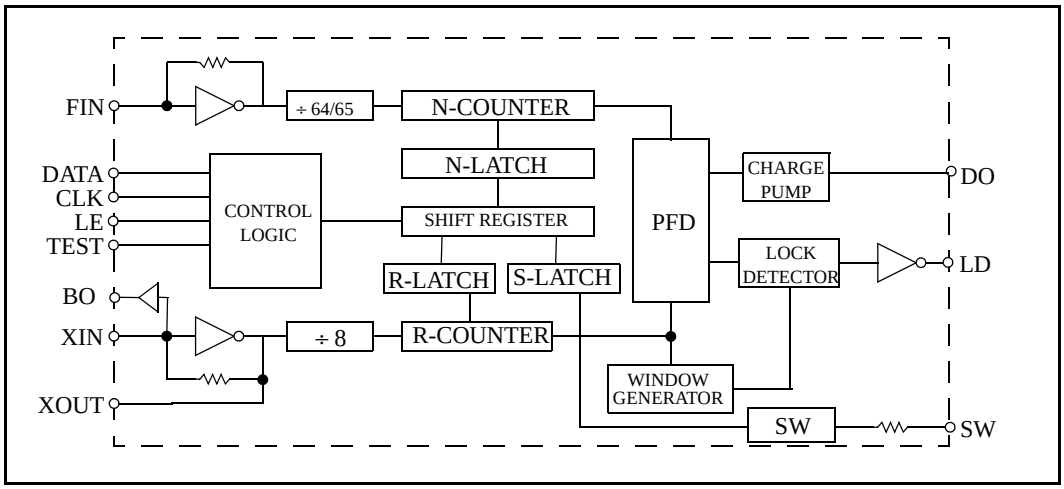
- Supply voltage range: 2.7 to 3.3 V
- Built-in crystal oscillator for mixer local oscillator
- Mixer input frequency: 10 — 50 MHz
- Quadrature detector
- On-chip audio filter
- Audio output
- Up to 40 MHz external crystal oscillator reference frequency under normal condition
- With Schmitt trigger added for noise-immune programming input
- 18-bit programmable input frequency divider (including a ÷ 64/65 prescaler) with divide ratio range from 4032 to 262143
- 13-bit programmable reference frequency divider (including a ÷ 8 prescaler) with divide ratio range from 40 to 65528
- Optional lock detector output (*LD*, $f_R/2$, $f_V/2$)
- Charge pump output for passive low-pass filter
- Wide tuning range of charge pump output for external VCO (V_{SS}*+0.5 to* V_{DD2}*-0.5*)
- Switchover terminal for constant of loop filter or general open drain output
- Reference oscillator buffer output
- SSOP 28L package (0.64mm pitch)

Applications

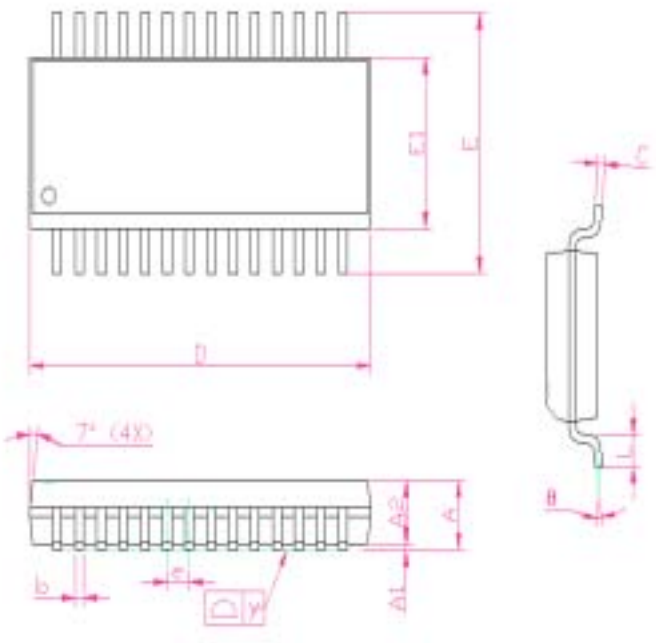
- Pager
- Family radio service (FRS)
- Wireless communication system

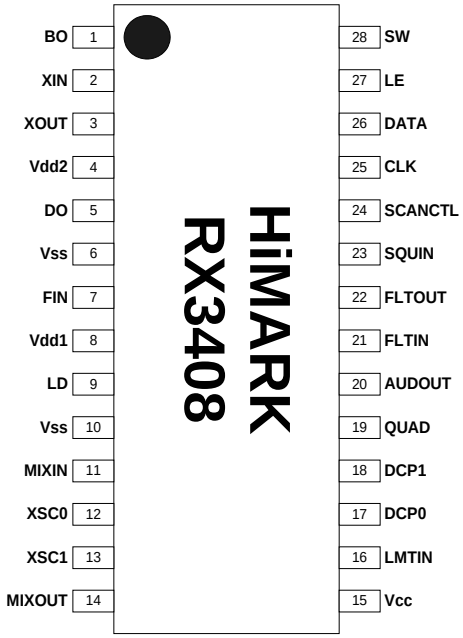
Block Diagram





Package and Pin Assignment: 28L, SSOP





Symbols	Dimensions in mm			Dimensions in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.60	0.75	0.053	0.064	0.069
A1	1.10	---	0.25	0.004	---	0.010
A2	---	1.45	---	---	0.057	---
b	0.20	0.25	0.30	0.008	0.010	0.012
C	0.19	---	0.25	0.007	---	0.010
D	9.80	---	10.00	0.386	---	0.394
E	5.80	---	6.20	0.228	---	0.244
E1	3.80	---	4.00	0.150	---	0.157
e	---	0.64	---	---	0.025	---
L	0.40	---	1.27	0.015	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°

Note: Tolerance ± 0.1mm unless otherwise specified

Pin Descriptions

Number	Name	I/O	Description
1	BO	O	Terminal of reference crystal oscillator buffer output
2	XIN	I	Reference crystal oscillator or external clock input with internally biased amplifier (any external input to XIN must be ac-coupled)
3	XOUT	O	Reference crystal oscillator or external clock output
4	VDD2	POWER	Nominal 3.0 V supply voltage
5	DO	O	Single-ended charge pump output for passive low-pass filter
6	VSS	GND	PLL Ground
7	FIN	I	VCO frequency input with internally biased input amplifier (any external input to FIN must be ac-coupled)
8	VDD1	POWER	Nominal 1.0 V supply voltage
9	LD	O	Lock detector output (high when PLL is locked)
10	GND	GND	Ground
11	MIXIN	I	Mixer input (3.3 KΩ input impedance)
12	XSC0	I	Oscillator input (base)
13	XSC1	O	Oscillator output (emitter)
14	MIXOUT	O	Mixer output (1.8 KΩ output impedance)
15	VCC	POWER	Nominal 3.0 V supply
16	LMTIN	I	IF amplifier input (1.8 KΩ input impedance)
17	DCP0		IF amplifier de-coupling capacitor connection
18	DCP1		IF amplifier de-coupling capacitor connection
19	QUAD	I	Quadrature FM demodulator input
20	AUDOUT	O	Quadrature FM demodulator output
21	FLTIN	I	Audio bandpass filter input
22	FLTOUT	O	Audio bandpass filter output
23	SQUIN	I	Squelch circuit input
24	MUTE	O	Mute Outpou. Impedance to ground is low when squelch circut input level is low.
25	CLK	I	Shift register clock input
26	DATA	I	Serial data input
27	LE	I	Latch enable input
28	SW	O	Switchover terminal for constant of loop filter or a general open drain output

Absolute Maximum Ratings

V_{SS} = 0 V

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD1}	V_{SS} – 0.3 to V_{SS} + 2.0	V
	V_{DD2}	V_{SS} – 0.3 to V_{SS} + 6.0	V
	VCC	V_{SS} – 0.3 to V_{SS} + 6.0	V
Input voltage range	V_{FIN}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	–30 to 70	°C
Storage temperature range	T_{STG}	–65 to 150	°C
Soldering temperature range	T_{SLD}	255	°C
Soldering time range	t_{SLD}	10	s

Recommended Operating Conditions

V_{SS} = 0 V

Parameter	Symbol	Value			Unit
		min.	typ.	max.	
Supply voltage range	VCC	2	3	6	V
	V_{DD1}	0.95	1.0	2.0	V
	V_{DD2}	2.4	3.0	3.6	V
MIXIN input frequency	f_{MIXIN}		10.7		MHz
Operating temperature	T_A	–30	25	70	°C

Electrical Characteristics

(V_{CC} = 3.0 V, V_{DD1}= 3.0 V, V_{DD2}= 1.0 V, V_{SS} = 0 V, T_A = 25 °C, f_o=10.7 MHz, unless otherwise noted)

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
Quiescent current consumption Unmuted Muted	 $I_{cc,unm}$ $I_{cc,mut}$	FIN(pin7) = 500MHz V(pin23) = 1 V V(pin23) = 0 V		 4.0 5.4		mA
Audio output voltage	V_{aud}	On pin 20 with 10 mV rms in.	130	170	210	mV_{rms}
Input Limiting Voltage	V_{lim3dB}	On pin 11		2.6	6	µV
Total Harmonic Distortion	THD	On pin 20		0.86		%
Recovered Output Voltage	V_{rec}	On pin 20	60	190	350	mV_{rms}
Audio output impedance	$Z_{det,out}$	On pin 20		450		Ω
Filter Amplifier Gain	G_{filt}	On pin 22, with 10 KHz 0.3 mV rms signal input to pin 21	40	50		dB
Filter Amplifier dc Output voltage	V_{filt}	On Pin 22, measured with no audio input.	0.5	0.7	0.9	V
Scan control output level Unmuted Muted	 $V_{SC,unm}$ $V_{SC,mut}$	Measured on pin 24 V(pin23) = 1 V V(pin23) = 0 V	 3.0	 0 3.9	 0.4	V
Squelch Circuit Hysteresis	V_{hys}	Referred to pin 23		45	100	mV
Mixer Conversion Gain	G_{mix}	From pin 11 to pin 14		28		dB
Mixer Input Resistance	$R_{mix,in}$	On pin 11		3.3		KΩ
Mixer Input Capacitance	$C_{mix,in}$	On pin 11		9.0		pF
PLL part						
FIN operating frequency range	f_{FIN}	P_{FIN} = -15dBm V_{DD1} = 1.0 V, PS="L"	20		500	MHz
XIN operating frequency range	f_{XIN}	V_{DD1} = 1.0 V	7		40	MHz
FIN input voltage swing	P_{FIN}		-15			dBm
XIN input voltage swing	V_{XIN}		0.3			V_{pk-pk}
CLK, DATA, LE logic LOW input voltage	V_{IL}				0.3	V
CLK, DATA, LE logic HIGH input voltage	V_{IH}		V_{DD}-0.3			V

Parameter	Symbol	Condition	Value			Unit
			min.	typ.	max.	
XIN logic LOW input current	$I_{IL,XIN}$	V_{IL} = 0 V			10	µA
XIN logic HIGH input current	$I_{IH,XIN}$	$V_{IH} = V_{DD1}$			10	µA
FIN logic LOW input current	$I_{IL,FIN}$	V_{IL} = 0 V			60	µA
FIN logic HIGH input current	$I_{IH,FIN}$	$V_{IH} = V_{DD1}$			60	µA
Charge Pump Drive Current	I_{DO}	V_{DD2} = 3.0V, V_{DO} = 1.5V		1.0		mA
Charge Pump Sink Current	I_{DO}	V_{DD2} = 3.0V, V_{DO} = 1.5V		1.0		mA
LD, FV, FR logic LOW output current	I_{OL}	V_{OL} = 0.4 V	0.1			mA
LD, FV, FR logic HIGH output current	I_{OH}	$V_{OH} = V_{DD2}$ – 0.4 V	0.1			mA
SW logic LOW output current	$I_{SW,OFF}$	SW = 'L' $V_{SW} = V_{DD2}$ = 3.0V			10	µA
SW logic HIGH output current	$I_{SW,ON}$	SW = 'H' $V_{SW} = V_{DD2}$ = 3.0V		2.8		mA
DATA to CLK setup time	t_{SU1}		2			µs
CLK to LE setup time	t_{SU2}		2			µs
Hold time	t_{HOLD}		2			µs

Functional Description

The IF receiver part incorporates a mixer, crystal-based local oscillator, IF amplifier, quadrature FM demodulator, audio filter, and a squelch circuit and is capable of demodulating FM input signals.

Mixer

The mixer provides frequency downconversion from the 1st IF input on pin 16 down to the 455 KHz 2nd IF output on pin 3. The external 2nd IF filter should be chosen so that the specified output impedance on the mixer output port is an acceptable termination for the filter.

Crystal Oscillator

A single dcdc coupled transistor is available as a two port gain element (pins 1 & 2) to implement a crystal oscillator. The device is biased on-chip to a constant dc current.

IF Amplifier

The IF Limiter amplifies and limits the pin 5 input from the external 2nd IF filter. The output is a square wave that drives the following demodulator stage. Two off-chip decoupling capacitors to Vcc are required on pins 6 & 7 to remove dc content from the limiter input.

FM Demodulator

The demodulator provides an audio output generated by multiplying the input IF from the limiter with a quadrature version of the input. The quadrature version is generated by the combination of an on-chip 10pF series capacitor with an off-chip shunt LCR resonator connected between pin 8 and Vcc. Biasing for the input transistor on pin 8 comes from the off-chip resonator. The shape of the demodulator S-curve is determined by the shunt resistance on this LCR resonator. An off-chip RC low pass filter should be used on pin 9 for removal of the 2nd IF components.

Filter Amplifier

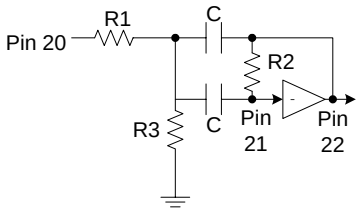
The filter amplifier provides an inverting gain element between pins 10 & 11 for the implementation of an audio filter. Typically, a bandpass Delyiannis-Friend active filter is built by adding externally at least two resistors and two capacitors to this amplifier. An external dc path must be provided through the feedback network across these pins to set the dc operating point. The design equations are as follows:

$$R_1 = \frac{R_2}{2A_o} \qquad R_2 = \frac{1}{(2Q)^2} \cdot \left(\frac{R_1 \cdot R_2}{R_1 - R_2}\right) \qquad R_3 = \frac{Q}{\pi(f_o \cdot C)}$$

where:

f_o is the desired center frequency, Q is the quality factor, A_o is the voltage gain at band cen-

ter, R_2 is the feedback resistance, C is the value for both capacitors, R_1 the series input resistance and R_2 the shunt resistance.



PLL Programmable Input Frequency Divider

The VCO input to the FIN pin is divided by the programmable divider and then internally output to the phase/frequency detector (PFD) as f_V. The programmable input frequency divider consists of a ÷ 64/65 (P/P+1) dual-modulus prescaler in prior to a 18-bit (N) counter, which is further comprised of a 6-bit swallow (A) counter, and a 12-bit main (B) counter. The total divide ratio, N, is related to values for P, A, and B through the relation

$$N = (P+1) \times A + P \times (B - A) = P \times B + A,$$

with $B \geq A$. The minimum available programmable divisor for continuous counting is given by $P \times (P-1) = 64 \times 63 = 4032$, and the valid total divide ratio range for the input divider is $M = 4032 \text{ to } 262143$.

Take N=10000 for example, since P=64 and hence that B=156 and A=16. Therefore, the binary codes of B and A should be 0000 1001 1100 and 010000, respectively. An alternative approach is to translate the decimal N into binary code directly. And then just take the last 6-bit as A and the remaining 12-bit as B. By far the binary code of N=10000 is 00 0010 0111 0001 0000. One can get the same result as the former method.

Programmable Reference Frequency Divider

The crystal oscillator output is divided by the programmable divider and then internally output to the PFD as f_R. The programmable reference frequency divider consists of a fixed ÷ 8 (S) prescaler and a 13-bit reference (R) counter. The total divide ratio, T, is related to values for S and R through the relation

$$T = S \times R = 8 \times R.$$

The usable divisior range of the reference counter is $R = 5 \text{ to } 8191$ and therefore, the valid total divide ratio range for the reference divider is $T = 40 \text{ to } 65528$ (in steps of 8.)

Serial Input Data Format

The divsors of the input and reference dividers are input using a 20-bit serial interface consisting of separate clock (CLK), data (DATA), and latch enable (LE) lines. The format

of the serial data is shown in Fig. 1. The data on the DATA line is written to the shift register on the rising edge of the CLK signal and is input with MSB first. The last two bits are recognized as the latch select control bits. Data on the DATA line should be changed on the falling edge of CLK, and LE should be held low while data is being written to the shift register. Data is transferred from the shift register to either one of the frequency divider latches or the optional control latch when LE is set high. When the latch select control bits are set high-low or low-low, data is loaded to the 18-bit *N*-counter latch, and when the latch select control bits are set high-high, the 2 MSBs are ignored, the next 13 data bits are loaded to the 13-bit *R*-counter latch and the remaining 3 LSBs are used to control testing modes and should be set as follows for normal operation: R14 = high, R15 = low, R16 = low. To disable LD output (*i.e.* set LD low), R14 should be set low. When the latch select control bits are set low-high, the 2 MSBs are recognized as PS and SW, which are used as stand-by control and open drain output control, respectively. The detail of two control bits setting is summarized in Table 1. In normal work condition, PS is set to low. When PS is programmed to high, it will enter stand-by mode.

Serial input data timing waveforms are shown in Fig. 2.

Fig. 1 – Serial input data format

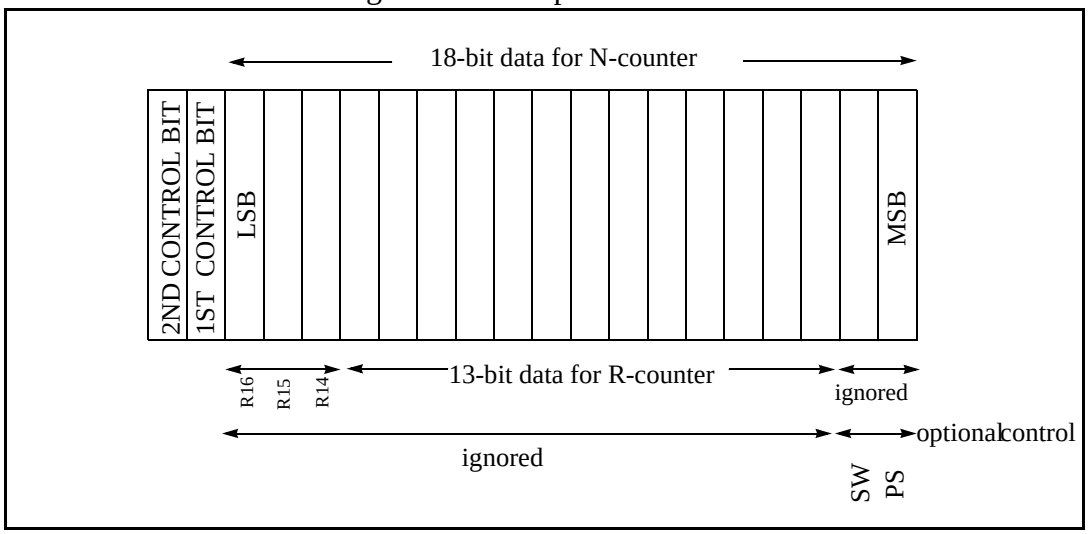
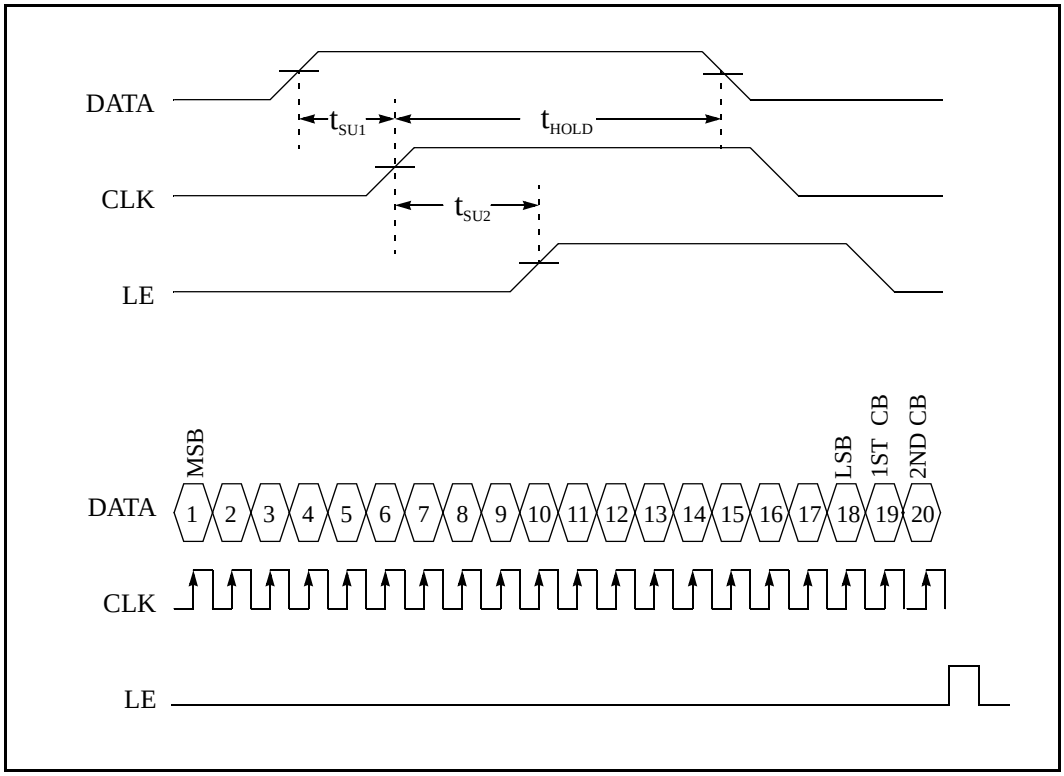


Table 1: Control Bit Setting

1st CB	2nd CB	Fetching Target of Serial Data Input
X	0	N-counter
0	1	PS and SW
1	1	R-counter

Fig. 2 – Serial input data timing waveforms



Phase/Frequency Detector (PFD)

The PFD compares an internal input frequency divider output signal, f_V, with an internal reference frequency divider output signal, f_R, and generates an error signal, DO, which is proportional to the phase error between f_V and f_R. The DO output is intended for use with a passive filter as shown in Fig. 2.

Lock Detector (LD)

When phase comparator detects phase difference, LD terminal outputs “L”. When phase comparator locks, LD terminal outputs “H”. On standby, outputs “H”. The criteria for lock condition is that the phase difference between f_V and f_R is less than *2/xin* and continues for more than three consecutive times.

The input/output waveforms for the PFD and LD are shown in Fig. 3.

Fig. 2 – Passive low-pass filter circuit

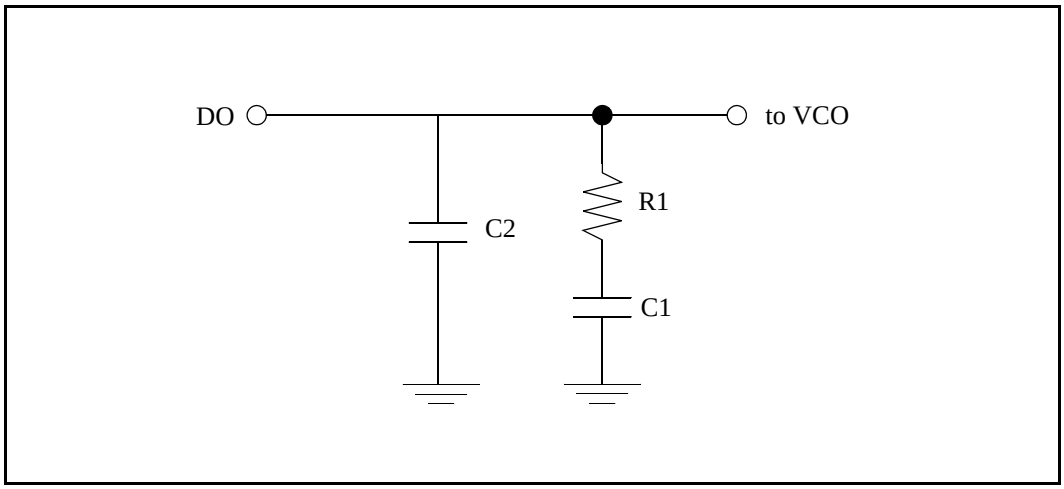
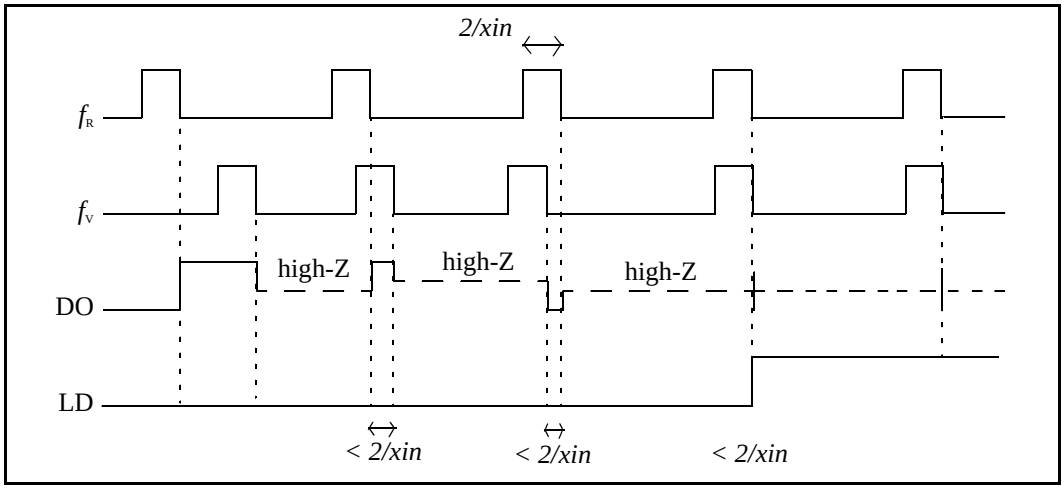


Fig. 3 – PFD input/output waveforms



Reference Crystal Oscillator Buffer Output (BO)

This IC provides a reference crystal oscillator buffer output intended to be used as a crystal local oscillator to a 2nd mixer. The terminal is represented as BO. For cases to enhance the buffer output swing, increasing V_{DD1} will be an efficient way.

Filter Switch Control (SW)

Control of SW terminal by "SW" bit. This terminal is for switching time-constant of loop filter. Output type of this terminal is open drain output. When constant of loop filter doesn't change by this switch, general open drain output is available. Note that there is an internal 200Ω resistor connected between and drain terminal and output pin.

Application Circuit