2.1A, 30V, 0.150 Ohm, P-Channel Logic Level, Power MOSFET

This product is a P-Channel power MOSFET manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. This transistor can be operated directly from integrated circuits.

Formerly developmental type TA49222.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFT2P03L	SOT-223	2P03L

NOTE: RFT2P03L is available only in tape and reel. Use the entire part number and add the suffix T.
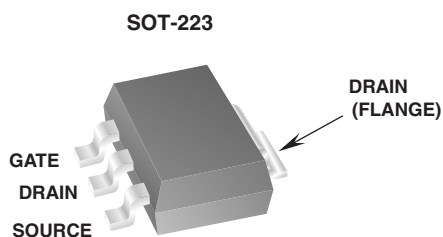
Features

- 2.1A, 30V
- $r_{DS(ON)} = 0.150\Omega$
- Temperature Compensating PSPICE® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

Packaging

SOT-223
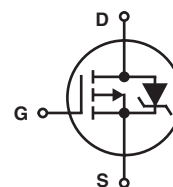
GATE
DRAIN
SOURCE

DRAIN
(FLANGE)

Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1) . . . . V_{DSS}	-30		V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) . . . . V_{DGR}	-30		V
Gate to Source Voltage . . . . V_{GS}	±20V		V
Drain Current			
Continuous (Note 2) (Figure 2). . . . . I_D	2.1		A
Pulsed Drain Current . . . . I_{DM}	Figure 5		
Pulsed Avalanche Rating. . . . . E_{AS}	Figures 6, 14, 15		
Power Dissipation (Note 2) . . . . P_D	1.1		W
Derate Above 25°C	0.009		W/^{o}C
Operating and Storage Temperature . . . . T_J, T_{STG}	-55 to 150		^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s. . . . . T_L	300		^{o}C
Package Body for 10s, See Techbrief 334 . . . . T_{pkg}	260		^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 11)		-30	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 10)		-1	-	-3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V$, $V_{GS} = 0V$		-	-	-1	µA
		$V_{DS} = -30V$, $V_{GS} = 0V$, $T_A = 150^oC$		-	-	-50	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = ±20V$		-	-	±100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 2.1A$, $V_{GS} = -10V$ (Figure 9)		-	0.120	0.150	Ω
		$I_D = 2.1A$, $V_{GS} = -4.5V$ (Figure 9)		-	0.300	0.360	Ω
Turn-On Time	t_{ON}	$V_{DD} = -15V$, $I_D \cong 2.1A$, $R_L = 7.1\Omega$, $V_{GS} = -10V$, $R_{GS} = 21\Omega$		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	13	-	ns
Rise Time	t_r			-	18	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	43	-	ns
Fall Time	t_f			-	24	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to -20V	$V_{DD} = -15V$, $I_D \cong 2.1A$, $R_L = 7.1\Omega$ $I_{g(REF)} = -1.0mA$ (Figure 13)	-	27	33	nC
Gate Charge at -10V	$Q_{g(-10)}$	$V_{GS} = 0V$ to -10V		-	14	17	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to -2V		-	1.3	1.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$, f = 1MHz (Figure 12)		-	620	-	pF
Output Capacitance	C_{OSS}			-	240	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	30	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.171 in^2 (See note 2)		-	-	110	^{o}C/W
		Pad Area = 0.068 in^2 (See Tech Brief 377)		-	-	128	^{o}C/W
		Pad Area = 0.026 in^2 (See Tech Brief 377)		-	-	147	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = -2.1A$	-	-	-1.25	V
Reverse Recovery Time	t_{rr}	$I_{SD} = -2.1A$, $dI_{SD}/dt = 100A/\mu s$	-	-	49	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = -2.1A$, $dI_{SD}/dt = 100A/\mu s$	-	-	45	nC

NOTE:

2. 110°C/W measured using FR-4 board with 0.171 in^2 footprint for 1000 seconds.
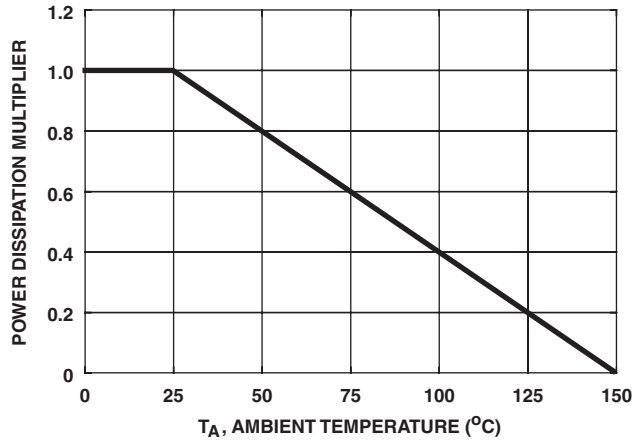
Typical Performance Curves Unless Otherwise Specified

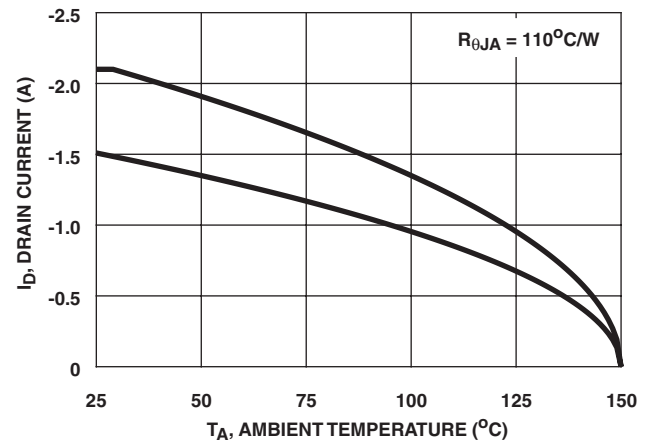FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

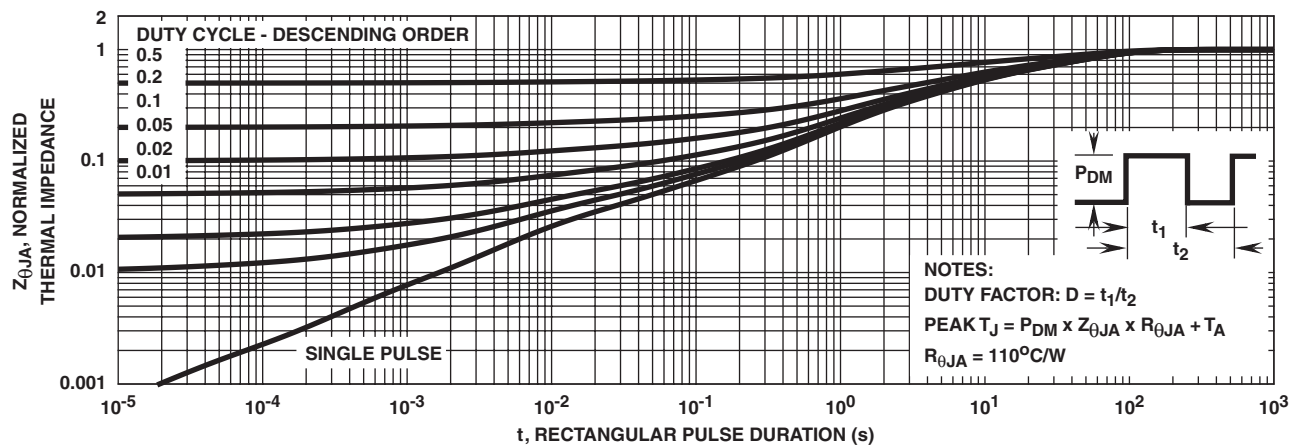FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

NOTES:

DUTY FACTOR: $D = t_1/t_2$

PEAK $T_J = P_{DM} \times Z_{\theta JA} \times R_{\theta JA} + T_A$

$R_{\theta JA} = 110^o C/W$

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

T_J = MAX RATED
$T_A = 25^o C$
$R_{\theta JA} = 110^o C/W$

OPERATION IN THIS AREA MAY BE LIMITED BY $r_{DS(ON)}$
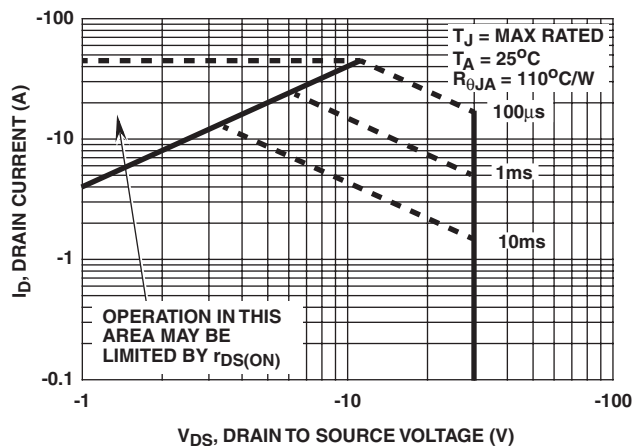
FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

$R_{\theta JA} = 110^o C/W$
$T_A = 25^o C$

FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$I = I_{25} \left[\sqrt{\dfrac{150 - T_A}{125}} \right]$
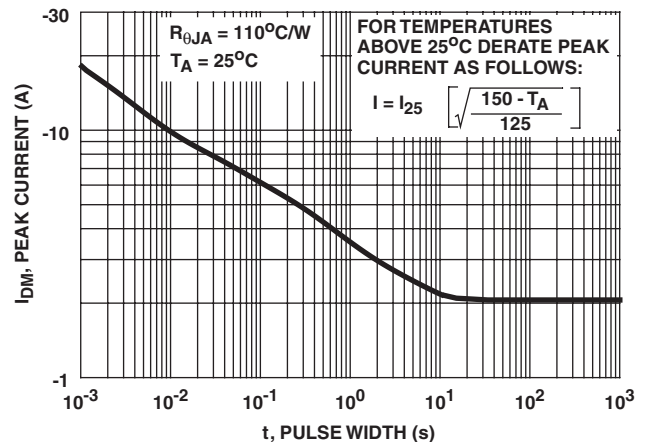
FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)

If R = 0
$t_{AV} = (L)(I_{AS})/(1.3*RATED BV_{DSS} - V_{DD})$
If R ≠ 0
$t_{AV} = (L/R)ln[(I_{AS}*R)/(1.3*RATED BV_{DSS} - V_{DD}) +1]$
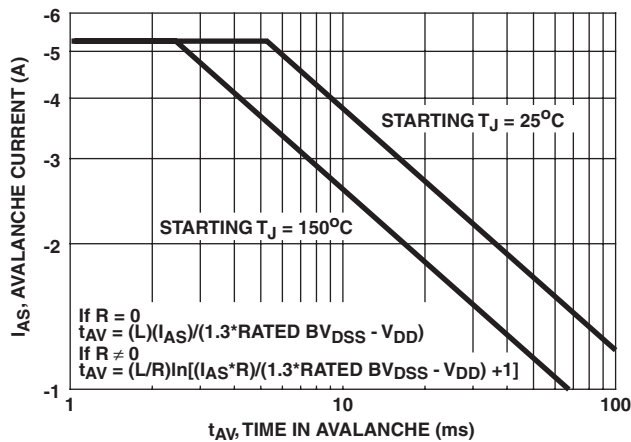
NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

PULSE DURATION = 250μs
DUTY CYCLE = 0.5% MAX
$T_A = 25^oC$
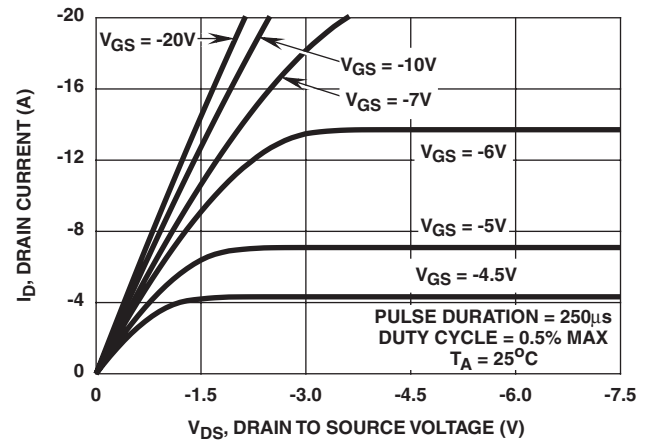
FIGURE 7. SATURATION CHARACTERISTICS

PULSE DURATION = 250μs
DUTY CYCLE = 0.5% MAX
V_{DD} = 15V
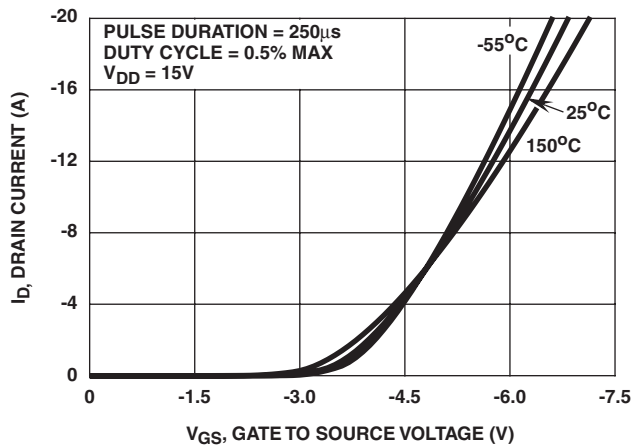
FIGURE 8. TRANSFER CHARACTERISTICS

PULSE DURATION = 80μs
DUTY CYCLE = 0.5% MAX
V_{GS} = -10V, I_D = 2.1A
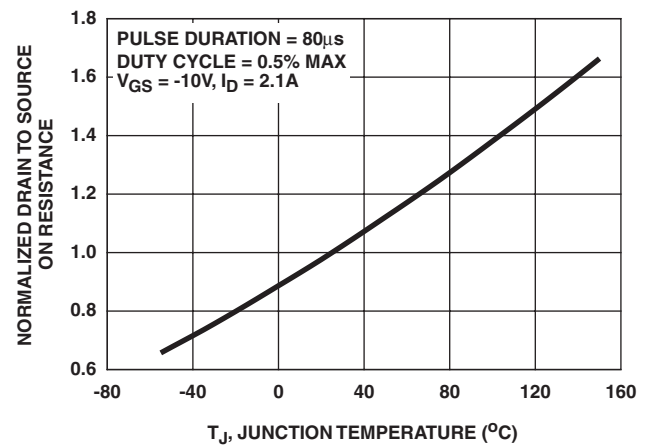
FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

$V_{GS} = V_{DS}$, I_D = 250μA
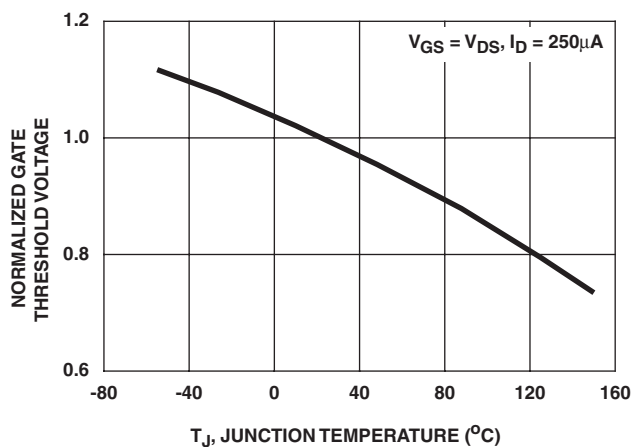
FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

I_D = 250μA
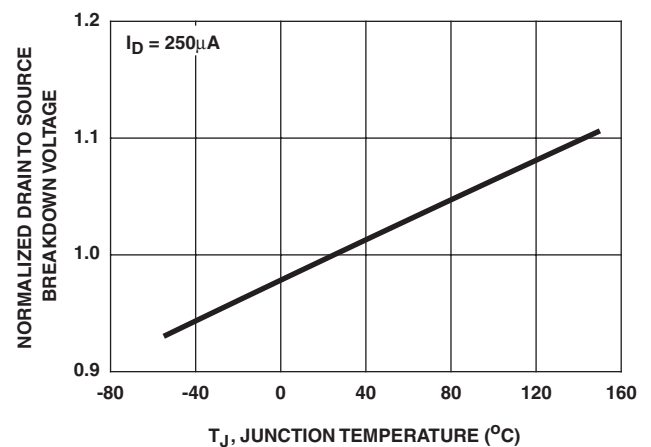
FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**
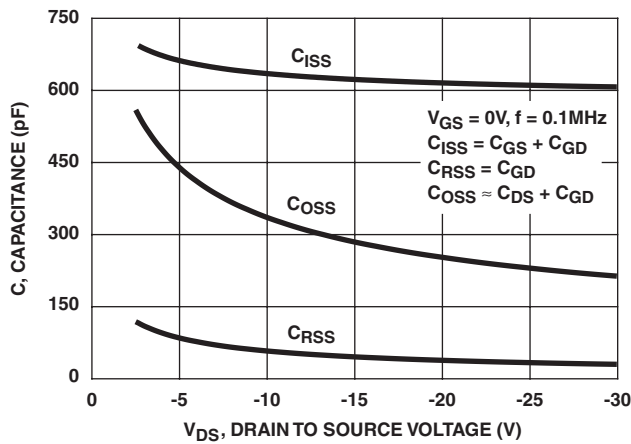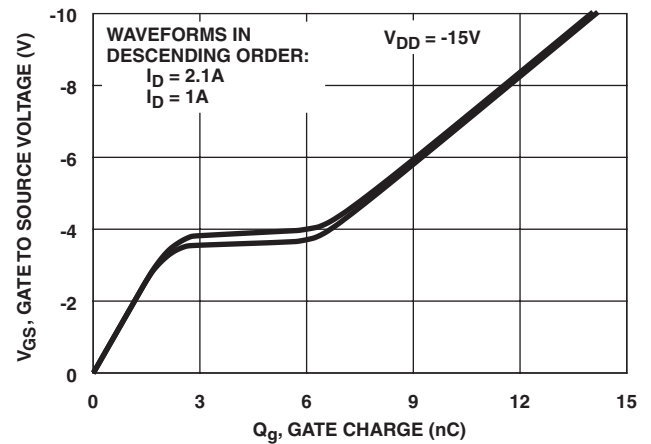

FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT
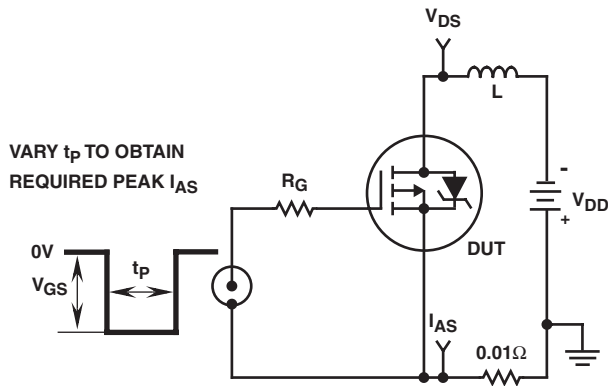
Test Circuits and Waveforms
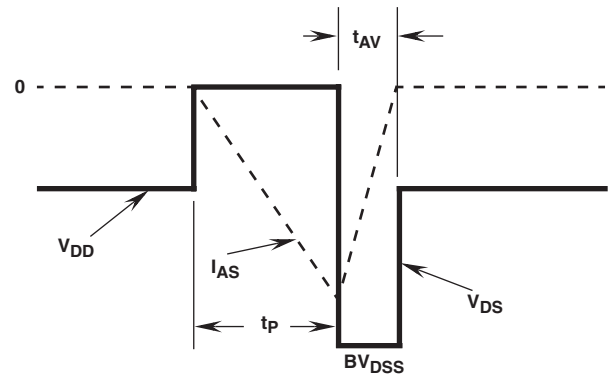

FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

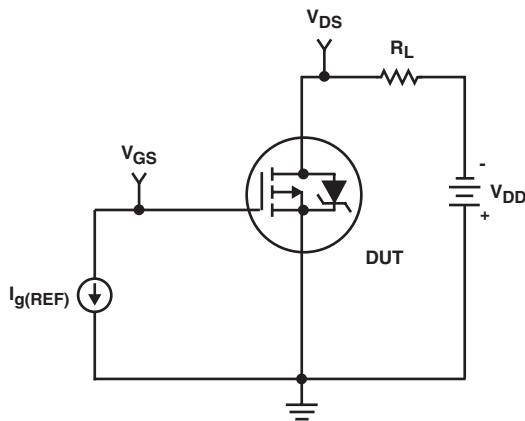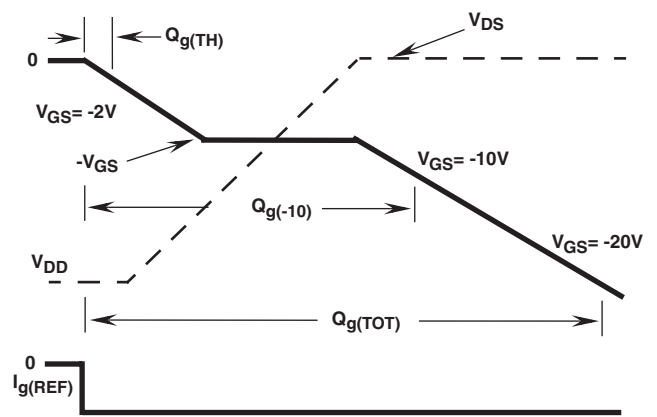FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

FIGURE 16. GATE CHARGE TEST CIRCUIT

FIGURE 17. GATE CHARGE WAVEFORM
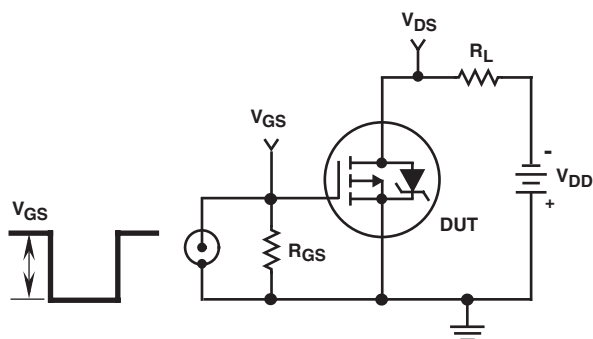
Test Circuits and Waveforms (Continued)

FIGURE 18. SWITCHING TIME TEST CIRCUIT

FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^{O}C), and thermal impedance $R_{\theta JA}$ (^{O}C/W) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SOT-223 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of the P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board

2. The number of copper layers and the thickness of the board

3. The use of external heat sinks

4. The use of thermal vias

5. Air flow and board orientation

6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides
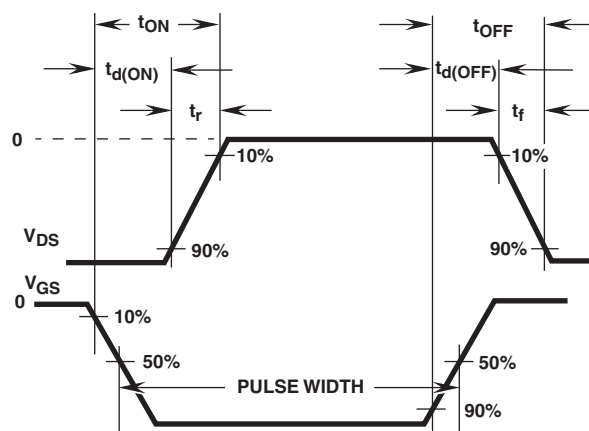
the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.
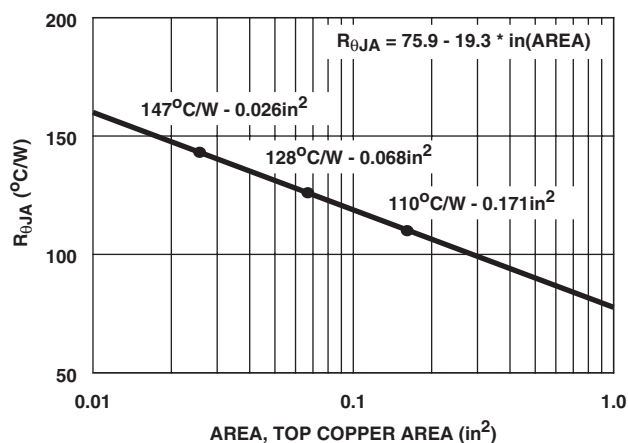

FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD AREA

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}. Thermal resistances corresponding to other component side copper areas can be obtained from Figure 20 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 75.9 - 19.3 \times \text{in(Area)} \qquad \text{(EQ. 2)}$$

PSPICE Electrical Model

.SUBCKT RFT2P03L 2 1 3 ;   REV July 1998

CA 12 8 6.5e-10
CB 15 14 6.4e-10
CIN 6 8 5.77e-10

DBODY 5 7 DBODYMOD
DBREAK 7 11 DBREAKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -41.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTHRES 6 21 19 8 1
EVTEMP 6 20 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.27e-9
LSOURCE 3 7 4.2e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 24e-3
RGATE 9 20 5.2
RLDRAIN 2 5 10
RLGATE 1 9 12.7
RLSOURCE 3 7 4.2
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 68e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*45),2.5))}

.MODEL DBODYMOD D (IS = 2e-13 RS = 3.5e-2 IKF = 0.7 XTI = 8.2 TRS1 = 6e-4 TRS2 = 5e-7 CJO = 7.3e-10 TT = 3.51e-8 M = 0.4
.MODEL DBREAKMOD D (RS = 2e-1   TRS1 = 1e-4 TRS2 = 1e-5)
.MODEL DPLCAPMOD D (CJO = 2.65e-10 IS = 1e-30 N = 10 M = 0.63)
.MODEL MMEDMOD PMOS (VTO = -2.6 KP = 1.2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 5.2)
.MODEL MSTROMOD PMOS (VTO = -3.27 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD PMOS (VTO = -2.11 KP = 0.07 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 52 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.2e-4 TC2 = -1e-7)
.MODEL RDRAINMOD RES (TC1 = 1.8e-2 TC2 = 2.1e-5)
.MODEL RSLCMOD RES (TC1 = 3.5e-3 TC2 = 1.3e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = 8.8e-4 TC2 = 6.1e-6)
.MODEL RVTEMPMOD RES (TC1 = -2e-3 TC2 = 1e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.7 VOFF= 2.7)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.7 VOFF= 5.7)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.1 VOFF= -2.4)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF= -0.1)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.
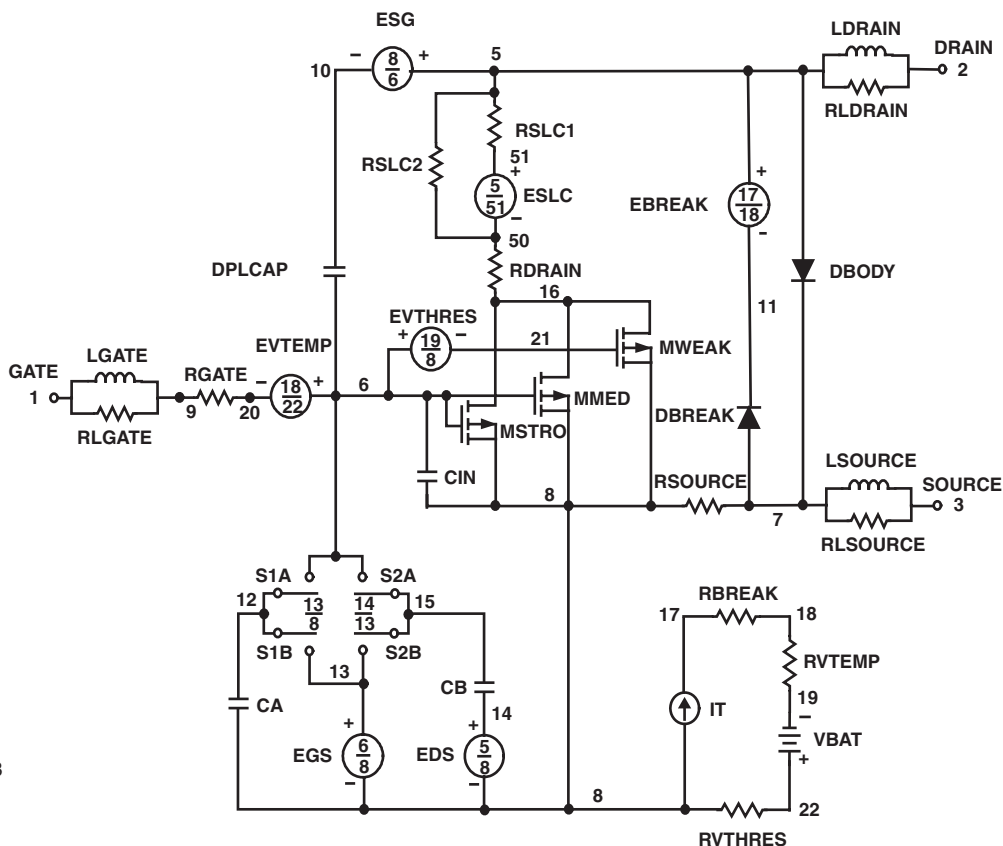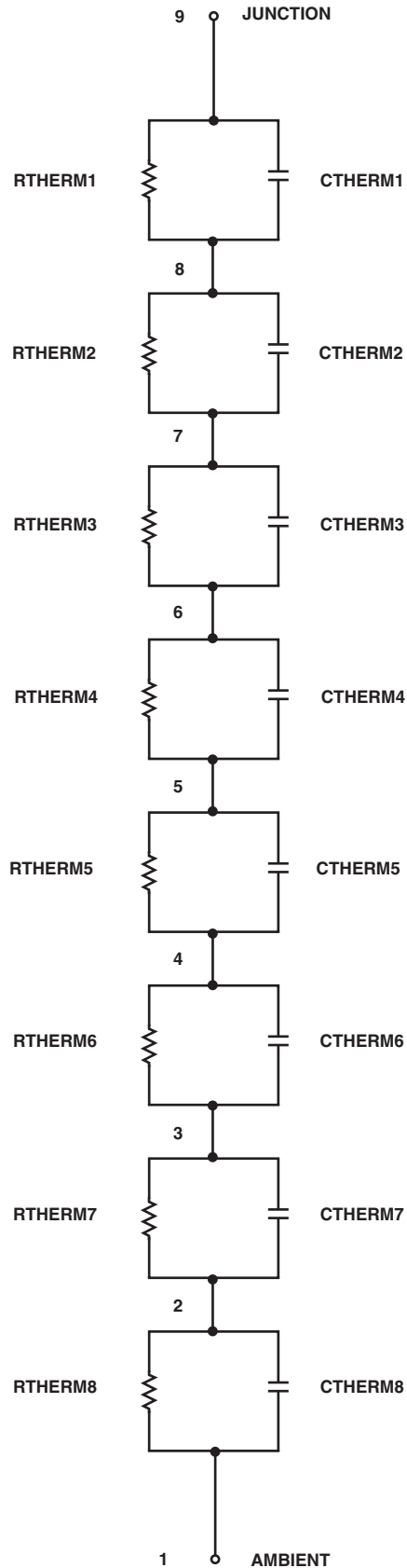
SPICE Thermal Model

REV July 98

RFT2P03L

CTHERM1 9 8 1.9e-5
CTHERM2 8 7 3.0e-4
CTHERM3 7 6 1.2e-3
CTHERM4 6 5 3.5e-3
CTHERM5 5 4 2.0e-2
CTHERM6 4 3 6.5e-2
CTHERM7 3 2 2.0e-1
CTHERM8 2 1 1

RTHERM1 9 8 3.5e-2
RTHERM2 8 7 8.5e-2
RTHERM3 7 6 3.5e-1
RTHERM4 6 5 1.85
RTHERM5 5 4 2.75
RTHERM6 4 3 15
RTHERM7 3 2 30
RTHERM8 2 1 50

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CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3
DenseTrench™	GTO™	Power247™	SuperSOT™-6
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™
E²CMOS™	LittleFET™	QS™	TinyLogic™
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™
FACT™	MicroPak™	Quiet Series™	UHC™
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H4