General Description

The RSC-4x represents Sensory's next generation speech processor designed to bring advanced audio features to cost sensitive embedded and consumer products. Based on an 8-bit microcontroller, the RSC-4x integrates speech-optimized digital and analog processing blocks into a single chip solution capable of accurate speech recognition as well as high quality, low data-rate compressed speech. Products can use one or all features in a single application.

The RSC-4x supports Sensory Speech™ 7, which includes advanced algorithms that add features and increase accuracy. Capable of running both HMM and sophisticated neural network technology, on-chip speech recognition algorithms reach an accuracy of greater than 97% for speaker-independent recognition and greater than 99% for speaker-dependent recognition.

In addition to the improved recognition performance, the RSC-4x provides further on-chip integration of features, including a preamplifier, twin-DMA units, vector accelerator, hardware multiplier, 3 timers, and 4.8 Kbytes of RAM. A complete system may be built with minimal additional parts other than a battery, speaker, microphone, and a few resistors and capacitors.

Multiple ROM options are available.

Features

Full Range of Sensory Speech™ 7 Capabilities

- Enhanced word spotting capability (5 SI or 10 SD words) in parallel
- Speaker independent and dependent recognition
- High quality, 5Kbps (typ) speech synthesis and sound effects
- Speaker verification
- Four voice music synthesis
- Voice record & playback
- Amplitude wake up from standby

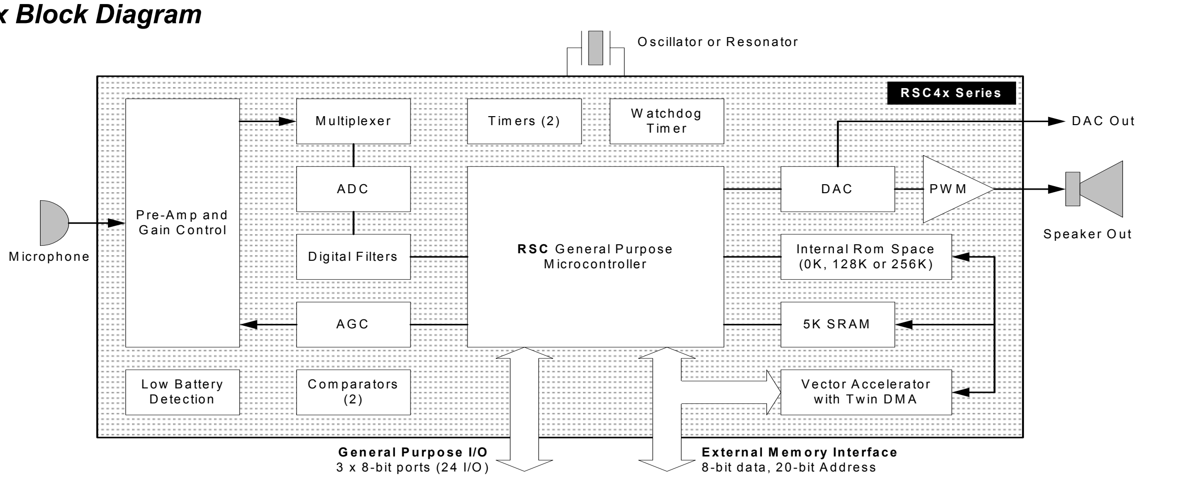
Integrated Single-Chip Solution

- 8-bit microcontroller
- On-chip 16 bit ADC, 10 bit DAC and mic pre-amp
- Uses low cost 3.58MHz crystal (internal PLL)
- 4.8 KB total RAM (256Bytes user-RAM)
- Three independent timers (3 GP, 1 Watchdog)
- Twin-DMA, Vector accelerator, and 24x24 multiplier
- External memory bus: 20-bit Address, 8-bit Data
- On chip storage for SD, SV, templates
- Code security through no ROM dump capability
- Built-in Analog Comparator Unit
- Low EMI design for FCC and CE requirements
- 24 I/O lines with 10 mA (typ) outputs
- Fully nested interrupt structure with up to 6 sources

Long Battery Life

- 2.4 – 3.6V operation
- Low battery detection
- 10mA (typ) operating current at 3V
- 2 low power modes; <5 μA standby current

RSC-4x Block Diagram



RSC-4x Overview

The RSC-4x is a member of the Interactive Speech™ line of products from Sensory. It features a high-performance 8-bit microcontroller with on-chip A/D, D/A, preamplifier, RAM, ROM (except on ROM-less version), and optimized audio processing blocks. The RSC-4x is designed to bring a high degree of integration and versatility into low-cost, power-sensitive applications. Various functional units have been integrated onto the CPU core in order to reduce total system cost and increase system reliability.

The RSC-4x operates in tandem with Sensory Speech™ 7 firmware, an ultra compact suite of recognition and synthesis technologies. This reduced software footprint enables, for example, products with over 150 seconds of compressed speech, multiple speaker dependent and independent vocabularies, speaker verification, and all application code built into the RSC-4128 as a single chip solution.

The CPU core embedded in the RSC-4x is an 8-bit, variable-length-instruction microcontroller. The instruction set is somewhat similar to the 8051 microcontroller, and has a variety of addressing mode *mov* instructions. The RSC-4x processor avoids the limitations of dedicated A, B, and DPTR registers by having completely symmetrical source and destinations for all instructions.

Speech Recognition

The RSC-4x is capable of executing both HMM (Hidden Markv Modelling) as well as a neural network to perform speech recognition. Speaker-dependent recognition may require external memory to store speech recognition information (e.g., SRAM, Serial EEPROM, Flash Memory). Speaker independent recognition requires on-chip or off-chip ROM to store the words to be recognized. The RSC-4x has several additional speech recognition features as described below:

- *Speaker independent* recognition requires no training. The RSC-4x can recognize up to 16 words in an active set (number of sets is limited only by internal ROM or external memory).
- *Speaker dependent* recognition allows the user to create custom vocabularies. Up to 100 words can be recognized in an active set (number of sets is limited only by internal ROM or external memory).
- *Continuous listening* allows the chip to continuously listen for a specific word. With this feature, a product can be used in a normal environment and only "activates" when a specific word, preceded by quiet, is spoken.
- Word spotting allows the chip to continuously listen for up to 5 SI or 10 SD words at a time. In word spotting mode, the word does not require termination by silence.

The RSC-4x can store up to 6 SD words on-chip, or more with external memory.

Speech and Music Synthesis

The RSC-4x provides high-quality speech synthesis using state of the art frequency domain techniques. Typical data rates are 5000 bits per second. Speech synthesis requires on-chip or off-chip ROM to store audio sound data for synthesis.

The RSC-4x provides high-quality, low-cost four-voice music synthesis which allows multiple, simultaneous instruments for harmonizing. The RSC-4x uses a MIDI-like system to generate music.

Record and Playback

The RSC-4x can perform audio record and playback at various compression levels depending on the quantity and quality of playback desired. Data rates of under 14,000 bits per second are achievable while maintaining very high quality reproduction. The RSC-4x also performs silence removal to improve sound quality and reduce memory requirements.

Speaker Verification

The RSC-4x can also perform text-dependent speaker verification. After a speaker trains the chip on a specific word, the chip is able to identify whether that word is spoken by the original speaker, thus providing biometric security. The RSC-4x can store up to 6 SV words on-chip, or more with external memory.

RSC-4x Architecture

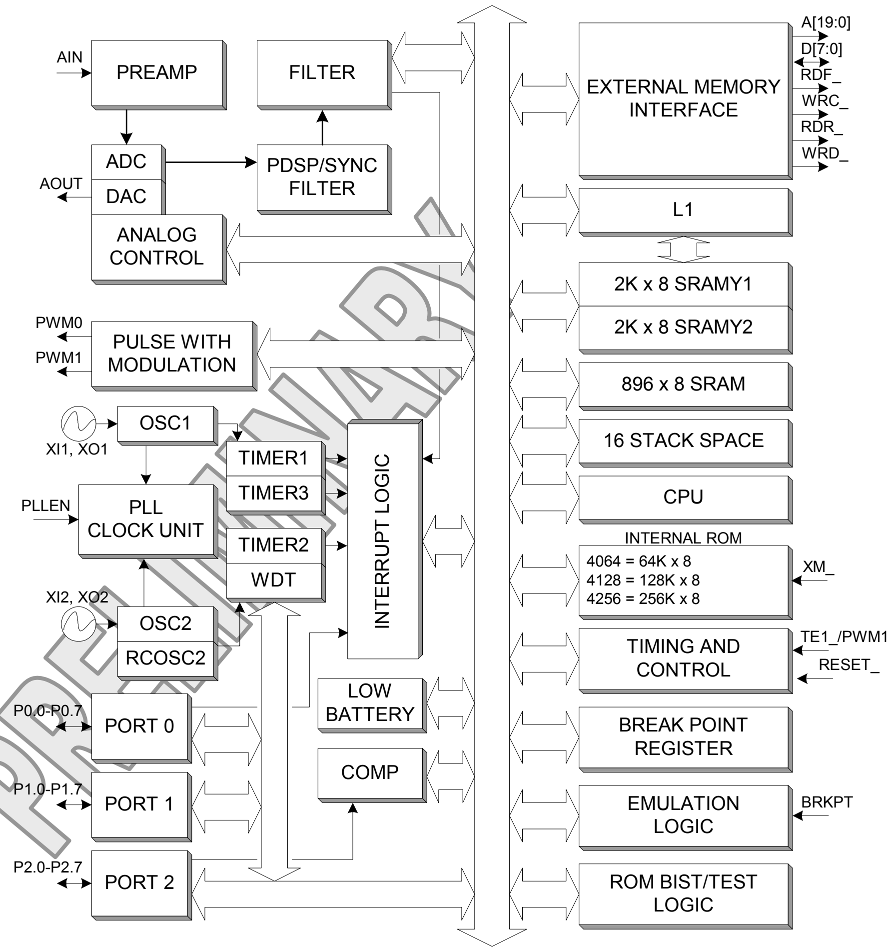
The RSC-4x is a highly integrated device that combines:

- 8-bit microcontroller
- On-chip ROM (except on RSC-4000) and RAM (4.8 Kbytes), and the ability to address off-chip RAM, ROM, EPROM or Flash (RSC4000 only)
- 16 bit A/D converter and 10 bit D/A converter
- Input preamp and Pulse Width Modulator (speaker driver)

The RSC-4000 has 20-bit address and 8-bit data busses for interfacing with external memory. Members of the RSC-4x family with internal ROM contain an XM_ input pin capable of enabling or disabling the internal ROM.
Note that neither the XM_ input pin nor the extended memory busses are available on packaged versions of the RSC-4x family with internal ROM.

Three bi-directional ports provide 24 general-purpose I/O pins to communicate with external devices.

The RSC-4x has a high frequency (14.32 MHz) oscillator as well as a low frequency (32,768 Hz) oscillator suitable for timekeeping applications (the high frequency clock can be derived from a low-cost 3.58 Mhz crystal). The processor clock can be selected from either source, with a selectable divider value. The device performs speech recognition when running at 14.32 MHz. The RSC-4x also supports programmable wait states to allow the use of slower external devices.

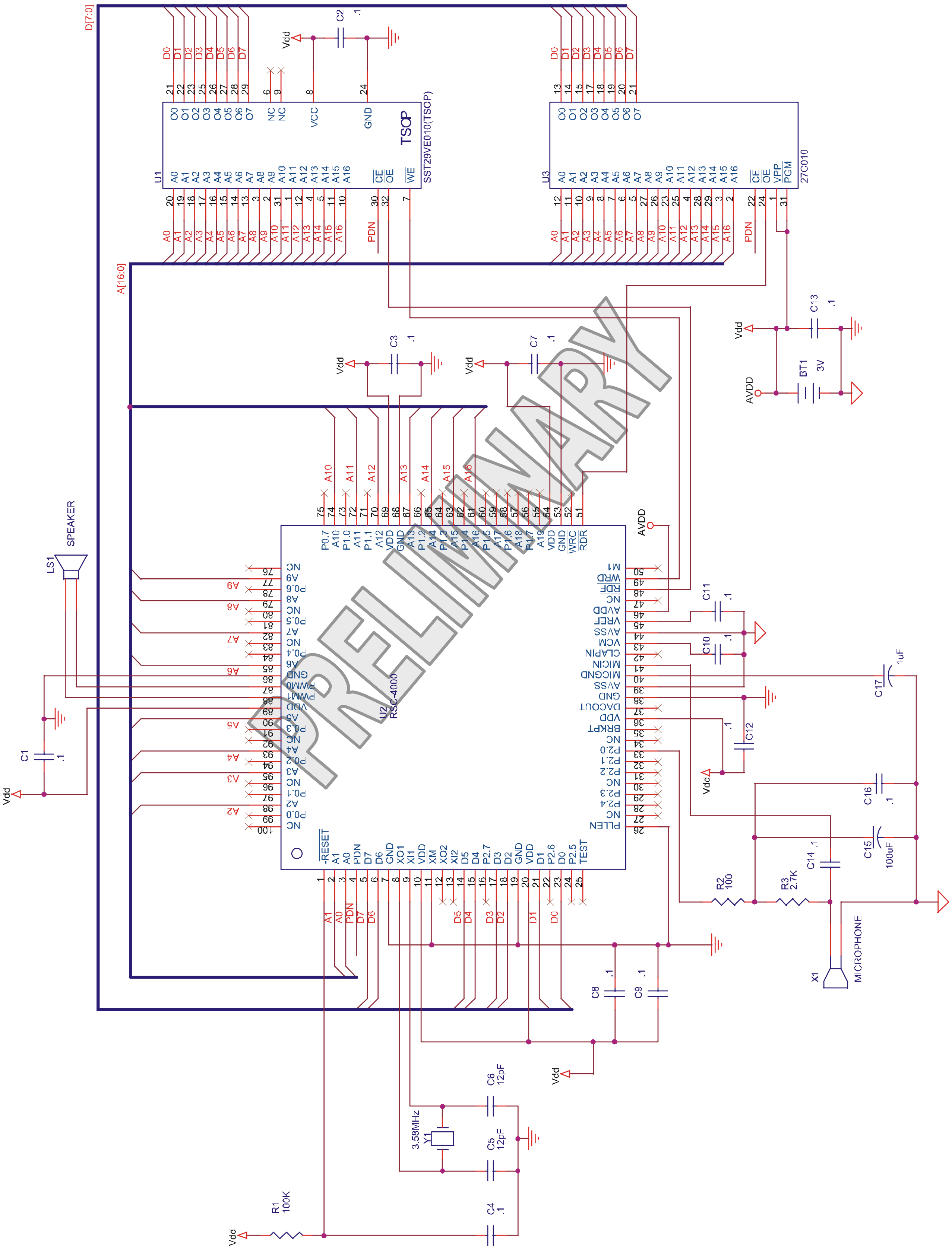


RSC-4x Block Diagram

There are three programmable 8-bit counters / timers; timer 1 and 3 are derived from OSC1 and timer 2 and watchdog from OSC2.

An external microphone passes an audio signal to the preamplifier and ADC (Analog-to-Digital Converter) to convert the incoming speech signal into digital data. The output audio signal of the RSC-4x is derived from a DAC (Digital-to-Analog Converter) or PWM (Pulse Width Modulator).

Reference Schematic



Using the RSC-4x

Creating applications using the RSC-4x requires the development of electronic circuitry, software code, and speech/music data files. Software code for the RSC-4x can be developed by Sensory or by external programmers using the RSC-4x Development Kit. For more information about development tools and services, please contact Sensory. A typical product will require about $0.30 - $1.00 (in high volume) of additional components, in addition to the RSC-4x.

Instruction Set

The instruction set for the RSC-4x has 60 instructions comprising 13 move, 7 rotate, 11 branch, 22 arithmetic, and 7 miscellaneous instructions. All instructions are 3 bytes or fewer, and no instruction requires more than 10 clock cycles to execute.

Power

The typical operating current is 10 mA operating with a main clock rate of 14.32 MHz at 3V. Lowering clock frequency reduces power consumption, although speech recognition requires a 14.32 MHz clock (derived from the 3.58 MHz oscillator #1 crystal). Standby current is <5µA in power down mode.

Two power-down modes are available. In SLEEP mode everything is stopped, and only an I/O, audio, or reset event can initiate a wake-up. In IDLE mode oscillator #2 and timer #2 continue to run, and a timer #2 overflow can also generate a wake-up. To minimize power consumption, most operational blocks on the chip have individual power controls that may be selectively enabled or disabled, as well as gated by the PDN bit.

General Purpose I/O

The RSC-4x has 24 general-purpose I/O pins (P0.0-P0.7, P1.0-P1.7, P2.0-P2.7). Each pin can be programmed as an input with weak pull-up (~200kΩ equivalent device); input with strong pull-up (~10kΩ equivalent device); input without pull-up, or as an output.

External Memory

The RSC-4000 includes an external memory interface that allows connection with memory devices for speaker-dependent speech recognition, audio record/playback, and extended durations of speech and music synthesis.

Separate data and address buses allow use of standard EPROMs, ROMs, SRAMs, and Flash memory with little or no additional decoding. Support for separate read and write signals for each external memory space further simplifies interfacing. The RSC-4000 includes 8 data lines (D[7:0]) and 20 address lines (A[19:0]), and associated control signals for memory interfacing.

Oscillators

Two independent oscillators in the RSC-4x provide a high-frequency clock and a 32kHz time-keeping clock. The oscillator characteristics are:

OSC	FREQ	PLL	PINS	SOURCES
1	3.58 MHz	4X	XI1 XO1	Crystal Ceramic resonator LC
2	32768 Hz	N/A	XI2 XO2	Crystal Internal RC

Clock

The RSC-4x uses a fully static core – the processor can be stopped (by removing the clock source) and restarted without causing a reset or losing contents of internal registers. Static operation is guaranteed from DC to 14.32 MHz.

The 3.58 MHz oscillator #1 is frequency quadrupled to produce the 14.3 MHz Clock #1 signal. This creates internal RAM cycles of 70 nsec duration and internal ROM (except on RSC-4000) or external cycles of 140 nsec duration. Careful design may allow operation with memories having access times as slow as 120 nsec.

The 32768 Hz oscillator #2 generates the clock #2 signal at the same frequency. Either clock can be disabled to reduce power consumption when the other clock is selected as the processor clock.

Timers/Counters

The two independent oscillators of the RSC-4x provide counts to three internal timers. Each of the three timers consists of an 8-bit reload value register and a 4-bit decoded prescaler register. The reload register is readable and writeable by the processor.
To provide a safeguard against supply fluctuations, a separate 17-bit watchdog counter is derived from the 32768 Hz oscillator #2.

Interrupts

The RSC-4x allows for six interrupt sources, as selected by software. Each has its own mask bit and request bit in the IMR and IRQ registers respectively. The following events can generate interrupts:

1. Positive edge on Port 0, bit 0
2. Overflow of Timer 1
3. Overflow of Timer 2
4. Overflow of Timer 3
5. Sensory reserved functions
6. Completion of PWM sample period

Analog input

The analog front end for the RSC-4x consists of a microphone preamplifier, a 16-bit analog-to-digital converter, AGC, and an associated reference. All of this circuitry can be powered down to conserve battery life. The low-level signal from an electret microphone is amplified by a 26dB gain preamp.

A band-gap reference circuit supplies regulated analog power for the microphone, the preamp, and the analog modulator, and it also provides the low-voltage detector (brownout) reference voltage.

Analog Output

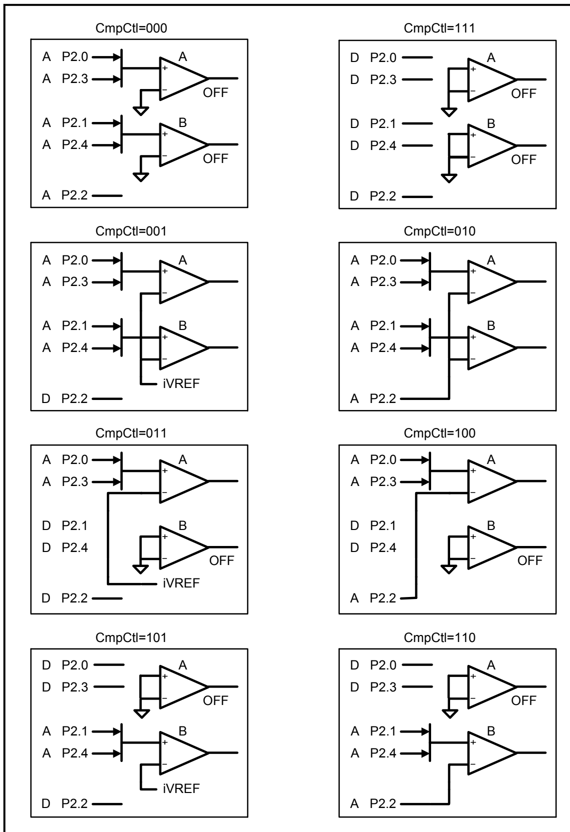
The RSC-4x offers two separate options for analog output. The DAC (Digital to Analog Converter) output provides a general-purpose 10-bit analog output that may be used for speech output (with an additional audio amplifier), or other purposes requiring an analog waveform. For speech applications that require driving a small speaker, the PWM (Pulse-Width Modulator) output can be used instead of the DAC output. The PWM has 10-bits of resolution, offers a low EMI design, and can directly drive an 8 to 32-ohm speaker.

Comparator Unit

Two analog comparators (A and B) can provide level information under software control for four external analog signals.

Each comparator can be separately enabled or disabled. When a comparator is disabled, inputs are isolated from any circuitry common to both comparators, the inputs are grounded, and the comparator power is turned off.

Each comparator "+" input has an analog mux that selects between one of two external signals. The "-" inputs of both comparators are connected together. This common "-" input can be muxed to either an external signal or the Comparator Reference Voltage (CRV).



Comparator Unit

Emulation features

A breakpoint interrupt, BRKPT, may be used by emulator logic to cause a breakpoint at any time. In applications this interrupt should be bonded to the supply ground.

In addition, output pin M1 provides a signal that is active for the entire instruction fetch cycle.
Note that in case the ship is running with 0 wait states the M1 provide a signal that is active for one clock cycle at the beginning of each instruction.

DC Characteristics

(T_O = -20°C to +70°C, V_{DD} = 2.4V – 3.6V)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.1		0.75	V	
V_{IH}	Input High Voltage	0.8*Vdd		Vdd+0.3	V	
I_{IL}	Input Leakage Current		<1	10	µA	$V_{ss}<V_{pin}<V_{dd}$
I_{ACT}	Supply Current, Active		10	20	mA	Hi-Z Outputs
I_{IDLE}	Supply Current, Idle		4	7	µA	Hi-Z Outputs
I_{SLEEP}	Supply Current, Sleep		1	4	µA	Hi-Z Outputs
R_{PU}	Pull-up resistance					
	P0.0-P0.7, P1.0-P1.7, P2.0- P2.7		10, 200, Hi-Z		kΩ	Software selectable
	A0-A19, D0-D7, PLLEN, RESET_, XM_RDR_, RDF_, WRC_, WRD_		100		kΩ	Fixed
	PWM0, PWM1		10		kΩ	Fixed
R_{PO}	Pull-down resistance TEST		10		kΩ	Fixed
I_{OL}	Output Low Current					
	A0-A19, D0-D7, RDR_, RDF_, WRC_, WRD_, PDN	4			mA	V_{OL} = 0.5V, V_{DD} = 2.4V
	P0.0-P0.7, P1.0-P1.7, P2.0-P2.7	8			mA	V_{OL} = 0.5V, V_{DD} = 2.4V
	PWM0, PWM1		160		mA	V_{OL} = 0.8V, V_{DD} = 3.3V
I_{OH}	Output High Current					
	A0-A19, D0-D7, RDR_, RDF_, WRC_, WRD_, PDN	-2.5			mA	V_{OH} = 1.8V, V_{DD} = 2.4V
	P0.0-P0.7, P1.0-P1.7, P2.0-P2.7	-5			mA	V_{OH} = 1.8V, V_{DD} = 2.4V
	PWM0, PWM1		80		mA	V_{OH} = 2.5V, V_{DD} = 3.3V

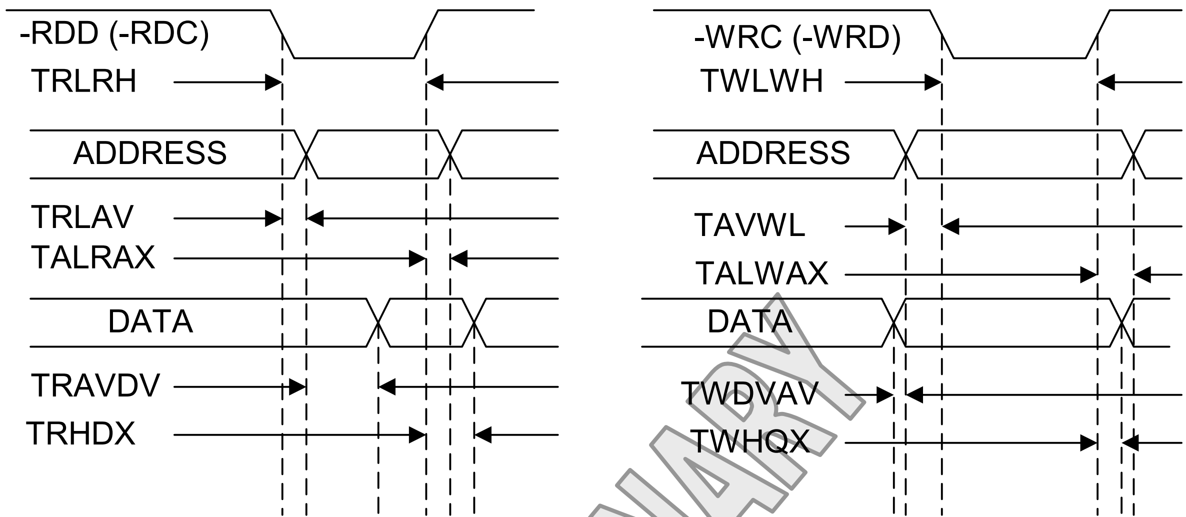
A.C. Characteristics (External memory accesses)

(T_O = 0°C to +70°C, V_{DD} = 3.3V; load capacitance for outputs = 30 pF; Osc=14.32 MHz)

SYMBOL	PARAMETER	CPU=osc/1, 1 WS		CPU=osc/2, 0WS		UNITS
		MIN	MAX	MIN	MAX	
1/TCL1	Processor Clock frequency		14.32		7.16	MHz
TRLRH	-RDC (-RDD) Pulse Width		140		140	ns
TRLAV	-RDC (-RDD) Low to Address valid		5		5	ns
TALRAX	Address hold after -RDC (-RDD)		0		0	ns
TRAVDV	Address valid to Valid Data In		135		135	ns
TRHDX	Data Hold after -RDC (-RDD)	0		0		ns
TWLWH	-WRC (-WRD) Pulse Width		140		140	ns
TAVWL	Address Valid to -WRC (-WRD)	35		70		ns
TALWAX	Address Hold after -WRC (-WRD)	35		70		ns
TWDVAV	Write Data Valid to Address Valid		5		5	ns
TWHQX	Data Hold after -WRC (-WRD)	35		70		ns

Timing Diagrams

Note that the -RDC signal does not necessarily pulse for every read from code space, but may stay low for multiple cycles.



External Read Timing **External Write Timing**

Absolute Maximum Ratings

Any pin to GND:	-0.1V to +4.5V
Operating temperature (T_O):	0°C to +70°C
Soldering temperature:	260°C for 10 sec
Power dissipation:	1 W
Operating Conditions:	0°C to +70°C; V_{DD} = 2.4 -3.6V V_{SS} = 0V

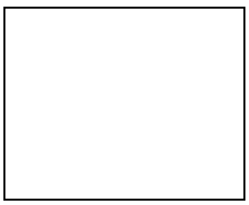
WARNING:
Stressing the RSC-4x beyond the “Absolute Maximum Ratings” may cause permanent damage. These are stress ratings only.
Operation beyond the “Operating Conditions” is not recommended and extended exposure beyond the “Operating Conditions” may affect device reliability.

Package Options

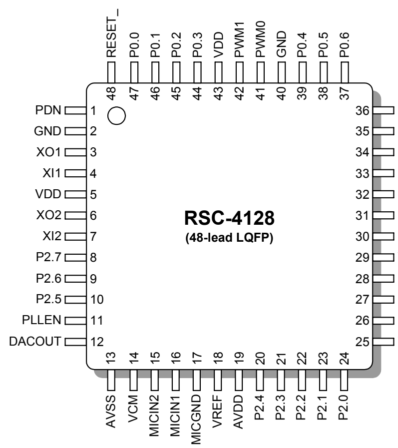
The RSC-4x can be purchased in a 100-lead LQFP (RSC-4000), 48 lead LQFP (RSC-4xxx) packages, or as unpackaged die (all versions).

DIE

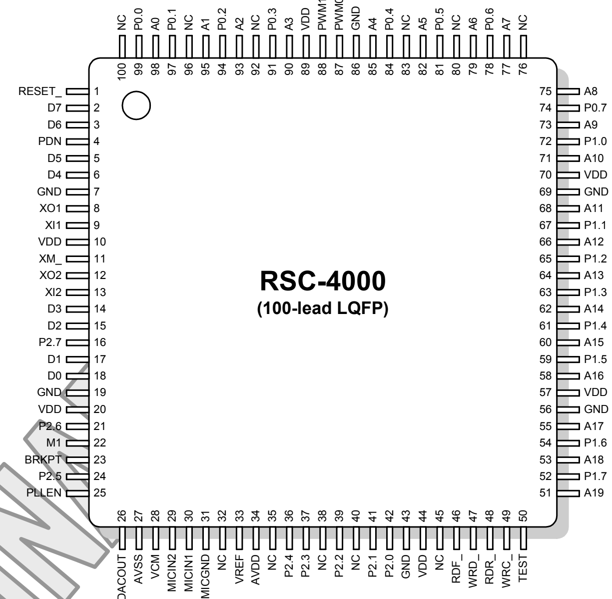
(pinout tbd)



48-lead LQFP



100-lead LQFP



DIE Pad #	48 LQFP Pin #	100 LQFP Pin #	Pin Name	Description	Signal Type
-	48	1	RESET_	Reset (active low)	Input, 100k pull-up resistor
-		2	D7	External Data Bus	Output, 100k pull-up
-		3	D6	External Data Bus	Output, 100k pull-up
-	1	4	PDN	Power Down (active high when powered down)	Output
-		5	D5	External Data Bus	Output, 100k pull-up
-		6	D4	External Data Bus	Output, 100k pull-up
-	2	7	GND	Ground	GND
-	3	8	XO1	Oscillator 1 output	Output
-	4	9	XI1	Oscillator 1 input	Input
-	5	10	VDD	Supply Voltage	PWR
-		11	XM_	External Memory Enable (active low)	Input, 100k pull-up resistor
-	6	12	XO2	Oscillator 2 output	Output
-	7	13	XI2	Oscillator 2 input	Input
-		14	D2	External Data Bus	Output, 100k pull-up
-		15	D3	External Data Bus	Output, 100k pull-up
-	8	16	P2.7	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		17	D1	External Data Bus	Output, 100k pull-up
-		18	D0	External Data Bus	Output, 100k pull-up
-		19	GND	Ground	GND
-		20	VDD	Supply Voltage	PWR
-	9	21	P2.6	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		22	M1	DO NOT USE	DO NOT USE
-		23	BRKP	DO NOT USE	-DO NOT USE
-	10	24	P2.5	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-	11	25	PLLEN	PLL Enable	Input, 100k pull-up resistor
-	12	26	DACOUT	DAC output	Analog out
-	13	27	AVSS	Analog ground	(A) GND
-	14	28	VCM	Common mode REFERENCE	Analog
-	15	29	MICIN2	Microphone input for audio wakeup	Analog IN
-	16	30	MICIN1	Microphone input	Analog IN
-	17	31	MICGND	Microphone amplifier input ground	Analog IN
-		32	NC	Not connected	
-	18	33	VREF	Voltage reference	Analog OUT

DIE Pad #	48 LQFP Pin #	100 LQFP Pin #	Pin Name	Description	Signal Type
-	19	34	AVDD	Analog Supply Voltage	(A) PWR
-		35	NC	Not connected	
-	20	36	P2.4	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-	21	37	P2.3	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		38	NC	Not connected	
-	22	39	P2.2	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		40	NC	Not connected	
-	23	41	P2.1	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-	24	42	P2.0	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		43	GND	Ground	GND
-		44	VDD	Supply Voltage	PWR
-		45	NC	Not connected	
-		46	RDF_	External Data Read Strobe (active low)	Output, 100k pull-up resistor
-		47	WRD_	External Data Write Strobe (active low)	Output, 100k pull-up resistor
-		48	RDR_	External Code Read Strobe (active low)	Output, 100k pull-up resistor
-		49	WRC_	External Code Write Strobe (active low)	Output, 100k pull-up resistor
-	25	50	TEST	Test Mode	Input, 10k pull-down resistor
-		51	A19	External Memory Address Bus	Output, 100k pull-up resistor
-	26	52	P1.7	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		53	A18	External Memory Address Bus	Output, 100k pull-up resistor
-	27	54	P1.6	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		55	A17	External Memory Address Bus	Output, 100k pull-up resistor
-	28	56	GND	Ground	GND
-	29	57	VDD	Supply Voltage	PWR
-		58	A16	External Memory Address Bus	Output, 100k pull-up resistor
-	30	59	P1.5	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		60	A15	External Memory Address Bus	Output, 100k pull-up resistor
-	31	61	P1.4	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		62	A14	External Memory Address Bus	Output, 100k pull-up resistor
-	32	63	P1.3	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		64	A13	External Memory Address Bus	Output, 100k pull-up resistor
-	33	65	P1.2	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		66	A12	External Memory Address Bus	Output, 100k pull-up resistor
-	34	67	P1.1	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		68	A11	External Memory Address Bus	Output, 100k pull-up resistor
-		69	GND	Ground	GND
-		70	VDD	Supply Voltage	PWR
-		71	A10	External Memory Address Bus	Output, 100k pull-up resistor
-	35	72	P1.0	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		73	A9	External Memory Address Bus	Output, 100k pull-up resistor
-	36	74	P0.7	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		75	A8	External Memory Address Bus	Output, 100k pull-up resistor
-		76	NC	Not connected	
-		77	A7	External Memory Address Bus	Output, 100k pull-up resistor
-	37	78	P0.6	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		79	A6	External Memory Address Bus	Output, 100k pull-up resistor
-		80	NC	Not connected	
-	38	81	P0.5	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		82	A5	External Memory Address Bus	Output, 100k pull-up resistor
-		83	NC	Not connected	
-	39	84	P0.4	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		85	A4	External Memory Address Bus	Output, 100k pull-up resistor
-	40	86	GND	Ground	GND
-	41	87	PWM0	Pulse Width Modulator Output 0	Output
-	42	88	PWM1	Pulse Width Modulator Output 1	Output
-	43	89	VDD	Supply Voltage	PWR
-		90	A3	External Memory Address Bus	Output, 100k pull-up resistor
-	44	91	P0.3	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		92	NC	Not connected	
-		93	A2	External Memory Address Bus	Output, 100k pull-up resistor
-	45	94	P0.2	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		95	A1	External Memory Address Bus	Output, 100k pull-up resistor
-		96	NC	Not connected	
-	46	97	P0.1	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		98	A0	External Memory Address Bus	Output, 100k pull-up resistor
-	47	99	P0.0	General Purpose I/O that can act as a “wake-up” input	I/O, 10k and 200k pull-up resistor or tri-state
-		100	NC	Not connected	

RSC4128 Instruction Set

This is the RSC-3x/4x instructions set. Instructions new to RSC-4128 are marked with “*”.

MOV Group:

```
MOV   dest_reg,source_reg   ; register to register move
MOV   @dest_reg, source_reg ; register to register-indirect move
MOV   dest_reg, @source_reg ; register-indirect to register move
MOV   dest_reg,#immediate   ; immediate data to register move
MOVC  dest_reg,@reg_pair    ; code space to register, indirect
MOVC  @reg_pair,source_reg  ; register to code space, indirect
MOVX  dest_reg,@reg_pair    ; data space to register, indirect
MOVX  @reg_pair,source_reg  ; register to data space, indirect
*MOVD dest_reg, source_reg  ; 16-bit register to register direct mov
PUSH  @reg--, source_reg    ; register to register-data stack push
POP   dest_reg, ++@reg      ; register to register-data stack pop
```

MOVC, MOVX, and MOVY instructions require a register pair to contain a 16-bit address. The register that specifies the pair must always be on an even address and will contain the low byte of the address. The next, odd, register will contain the high byte of the address. A single byte is moved.
The MOVD instruction requires both registers to be on even address boundaries. The contents of src+0 are moved to dest+0, and the contents of src+1 are moved to dest+1. MOVD also works with SFRs.
The PUSH instruction operates similar to the instruction pair {MOV @reg, source_reg, DEC reg}. POP functions similar to the instruction pair {INC reg, MOV dest_reg, @reg}. The sign, carry, and zero flag bits are unaffected by mov group instructions (including push and pop)

Branch Group:

```
JC    address               ; jump on carry = 1
JNC   address               ; jump on carry = 0
JZ    address               ; jump on zflag = 1
JNZ   address               ; jump on zflag = 0
JS    address               ; jump on sflag = 1
JNS   address               ; jump on sflag = 0
JMP   address               ; unconditional jump
JMPR  @reg_pair             ; indirect jump
CALL  address               ; unconditional subroutine call
RET                         ; return from subroutine
IRET                        ; return from interrupt: restore flags from
                            ;   hold register, then pop address stack
```

Note: The Conditional Branch instructions use direct addresses rather than offsets to define the branch target address.

Shift/Rotate Group:
In each of the following instructions the carry flag will be updated but the sign and zero flags are unaffected.

```
RL    register              ; rotate left. carry and bit0 set from original bit 7.
RR    register              ; rotate right. carry and bit7 set from original bit 0.
RLC   register              ; rotate left through carry (9-bit rotate).
RRC   register              ; rotate right through carry (9-bit rotate)
SHL   register              ; shift left. carry set from original bit 7.
                            ;   bit 0 becomes 0
SHR   register              ; shift right. carry set from original bit 0.
                            ;   bit 7 becomes 0.
SAR   register              ; shift right arithmetic. carry set from
                            ;   original bit 0. bit 7 duplicated (sign extension).
```


Arithmetic/Logical Group:
In each of the following instructions the sign and zero flags are updated based on the result of the operation. The carry flag is updated by the arithmetic operations (ADD, ADC, SUB, SUBC, CP, INC, DEC) but it is not affected by the logical operations (AND, TM, OR, XOR).
Note: the carry is set **high** by SUB, CP, SUBC, DEC when a borrow is generated.

```
AND   dest_reg, source_reg   ; dest_reg = dest_reg & source_reg
TM    dest_reg,source_reg    ; like AND, but dest_reg unchanged, flags updated
OR    dest_reg,source_reg    ; dest_reg = dest_reg | source_reg
XOR   dest_reg,source_reg    ; dest_reg = dest_reg ^ source_reg
SUB   dest_reg,source_reg    ; dest_reg = dest_reg - source_reg
CP    dest_reg,source_reg    ; like SUB,  but dest_reg unchanged, flags updated
SUBC  dest_reg,source_reg    ; dest_reg = dest_reg - source_reg - carry
ADD   dest_reg,source_reg    ; dest_reg = dest_reg + source_reg
ADC   dest_reg,source_reg    ; dest_reg = dest_reg + source_reg + carry
INC   register               ; register = register + 1
DEC   register               ; register = register - 1

AND   dest_reg,#immediate    ; dest_reg = dest_reg & immediate
TM    dest_reg,#immediate    ; like AND, but dest_reg unchanged, flags updated
OR    dest_reg,#immediate    ; dest_reg = dest_reg | immediate
XOR   dest_reg,#immediate    ; dest_reg = dest_reg ^ immediate
SUB   dest_reg,#immediate    ; dest_reg = dest_reg - immediate
CP    dest_reg,#immediate    ; like SUB,  but dest_reg unchanged, flags updated
SUBC  dest_reg,#immediate    ; dest_reg = dest_reg - immediate - carry
ADD   dest_reg,#immediate    ; dest_reg = dest_reg + immediate
ADC   dest_reg,#immediate    ; dest_reg = dest_reg + immediate + carry

*INCD      register          ; 16-bit register_pair increment.
                             ;   Flags set on 16-bit result.
*CPD  dest_reg, src_reg      ; 16-bit compare. Flags set on 16-bit result.
```

The CPD instruction requires both registers to be on even address boundaries. The contents of src+0 are compared to dest+0, and the contents of src+1 are compared to dest+1. The flags bits are set based on the 16-bit compare. The INCD instruction requires the register to be on an even address boundary. The effect of INCD is the same as the program sequence:

```
inc register+0
adc register+1, #0
```

Miscellaneous Group

```
CLC        ; clear carry
STC        ; set carry
CMC        ; complement carry
CLI        ; disable interrupts
STI        ; enable interrupts
NOP        ; nop operation
*WDC       ; enable/clear watchdog timer
```

Instruction Set Opcodes and Timing Details

The RSC4128 instruction set has 58 instructions comprising 11 move, 7 rotate, 11 branch, 13 register arithmetic, 9 immediate arithmetic, and 7 miscellaneous instructions. All instructions are 3 bytes or fewer, and no instruction requires more than 10 clock cycles to execute. The column "Cycles" indicates the number of clock cycles required for each instruction when operating with zero wait states. Wait states may be added to lengthen all accesses to external addresses or to the internal ROM (but not internal SRAM). The column "+Cycles/Waitstate" shows the number of additional cycles added for each additional wait state. Opcodes are in HEX.

MOVE Group Instructions

Register-indirect instructions accessing code (*movc*), data (*movx*), technology (*movy*) or register (*mov*) space locations use an 8-bit operand ("@source" or "@dest") to designate an SRAM register pointer to the 16-bit target address. The "source" or "dest" indirect pointer register must be at an even address unless it is a 8-bit pointer (indirect *mov*). The LOW byte of the target address is contained at the pointer address, and the HIGH byte of the target address is contained at the pointer address+1. Unless the flags register is the destination, the carry, sign, and zero flags are not affected by *mov* instructions.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles/Waitstate
MOV	10	dest	Source	register to register	3	5	3
MOV	11	@dest	Source	register to register-indirect	3	5	3
MOV	12	dest	@source	register-indirect to register	3	6	3
MOV	13	dest	#immed	immediate data to register	3	4	3
MOVC	14	dest	@source	code space to register	3	7	4
MOVC	15	@dest	Source	register to code space	3	8	4
MOVX	16	dest	@source	data space to register	3	7	4*
MOVX	17	@dest	Source	register to data space	3	8	4*
POP	18	dest	@++source	register to register data stack pop (source pre-incremented)	3	10	3
PUSH	19	@dest--	Source	register to register data stack push (dest post-decremented)	3	9	3
MOVD	1C	dest_pair	source_pair	register to register, direct, 16-bit mov	3	7	3

*MOVX instructions may have additional added wait states.

ROTATE Group Instructions

Rotate group instructions apply only directly to register space SRAM locations. The carry flag is affected by these instructions, but the sign and zero flags are unaffected.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles/Waitstate
RL	30	dest	-	rotate left, c set from b7	2	5	2
RR	31	dest	-	rotate right, c set from b0	2	5	2
RLC	32	dest	-	rotate left through carry	2	5	2
RRC	33	dest	-	rotate right through carry	2	5	2
SHL	34	dest	-	shift left, c set from b7, b0=0	2	5	2
SHR	35	dest	-	shift right, c set from b0, b7=0	2	5	2
SAR	36	dest	-	shift right arithmetic, c set from b0, b7 duplicated	2	5	2

BRANCH Group Instructions

The branch instructions use direct address values rather than offsets to define the target address of the branch. This implies that binary code containing branches is not relocatable. However, object code produced by the RSC4128 assembler contains address references that are resolved at link time, so .OBJ modules *are* relocatable. The indirect jump instruction uses an 8-bit operand ("@dest") to designate an SRAM register pointer to the 16-bit target address. The "dest" pointer register must be at an even address. The LOW byte of the target address is contained at the pointer address, and the HIGH byte of the target address is contained at the pointer address+1.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles/Waitstate
JC	20	dest low	dest high	jump on carry = 1	3	3	3
JNC	21	dest low	dest high	jump on carry = 0	3	3	3
JZ	22	dest low	dest high	jump on zflag = 1	3	3	3
JNZ	23	dest low	dest high	jump on zflag = 0	3	3	3
JS	24	dest low	dest high	jump on sflag = 1	3	3	3
JNS	25	dest low	dest high	jump on sflag = 0	3	3	3
JMP	26	dest low	dest high	jump unconditional	3	3	3
CALL	27	dest low	dest high	direct subroutine call	3	3	3
RET	28	-	-	return from call	1	2	1
IRET	29	-	-	return from interrupt	1	2	1
JMPR	2A	@dest	-	jump indirect	2	4	2

ARITHMETIC/LOGICAL Group Instructions

Arithmetic and logical group instructions apply only to Register Space SRAM locations. The results of the instruction are always written directly to the SRAM "dest" register. All but the INCrement and DECrement instructions have both register source and immediate source forms.

In each of the following instructions the sign and zero flags are updated based on the result of the operation. The carry flag is updated by the arithmetic operations (ADD, ADC, SUB, SUBC, CP, INC, DEC) but it is *not* affected by the logical operations (AND, TM, OR, XOR). Note: the carry is set **high** by SUB, CP, SUBC, DEC when a borrow is generated.

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles/Waitstate
AND	40	dest	source	logical and	3	6	3
TM	41	dest	source	like AND, destination unchanged	3	6	3
OR	42	dest	source	logical or	3	6	3
XOR	43	dest	source	exclusive or	3	6	3
SUB	44	dest	source	subtract	3	6	3
CP	45	dest	source	like SUB, destination unchanged	3	6	3
SUBC	46	dest	source	subtract w/carry	3	6	3
ADD	47	dest	source	add	3	6	3
ADC	48	dest	source	add w/carry	3	6	3
INC	49	dest	-	increment	2	5	2
DEC	4A	dest	-	decrement	2	5	2
AND	50	dest	#immed	logical and	3	5	3
TM	51	dest	#immed	like AND, destination unchanged	3	5	3
OR	52	dest	#immed	logical or	3	5	3
XOR	53	dest	#immed	exclusive or	3	5	3
SUB	54	dest	#immed	subtract	3	5	3
CP	55	dest	#immed	like SUB, destination unchanged	3	5	3

SUBC	56	dest	#immed	subtract w/carry	3	5	3
ADD	57	dest	#immed	add	3	5	3
ADC	58	dest	#immed	add w/carry	3	5	3
INCD	69	pair	-	register pair 16-bit increment.	2	8	2
CPD	66	dest_pair	source_pair	16-bit compare.	3	10	3

MISCELLANEOUS Group Instructions

Instruction	Opcode	Operand 1	Operand 2	Description	Bytes	Cycles	+Cycles/Waitstate
NOP	00	-	-	no operation	1	2	1
CLC	01	-	-	clear carry	1	2	1
STC	02	-	-	set carry	1	2	1
CMC	03	-	-	complement carry	1	2	1
CLI	04	-	-	disable interrupts	1	2	1
STI	05	-	-	enable interrupts	1	2	1
WDC	06	-	-	enable/restart watchdog timer	1	2	1

Special Functions Registers Summary

Address	R/W	Name	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FF	R/W	flags	0000 0000	carry	zero	sign	trap	stkoflo	stkfull	---	gie
FE	R/W*	IRQ	--00 0000	MTtimer	p0.2	block	timer3	p0.0	endmark	timer2	timer1
FD	R/W	IMR	--00 0000	MTtimer	p0.2	block	timer3	p0.0	endmark	timer2	timer1
FC	R/W	bank	1110 0000	ws2	ws1	ws0	(bank4)	bank3	bank2	bank1	bank0
FB	W	test mode	--00 0000	cntBypass	movC/WC	compOut	portFlip	BIST	filtRAM	filtRAMD	filtsumzc
	R	status	?u?0 --??	cksum	brownout	wd_timed	wd_on	---	---	fastClk	BIST busy
FA	R/W	DAC	0000 0000	dh7	dh6	dh5	dh4	dh3	dh2	dh1	dh0
F9	R/W	brkhi	1111 1111	brk15	brk14	brk13	brk12	brk11	brk10	brk09	brk08
F8	R/W	brklo	1111 1111	brk07	brk06	brk05	brk04	brk03	brk02	brk01	brk00
F7	R/W	stkData	0000 0000	stdk7	stkd6	stkd5	stkd4	stkd3	stkd2	stkd1	stkd0
F6	R/W	stkNdx	--00 0000	---	---	stkind5	stkind4	stkind3	stkind2	stkind1	stkind0
F5		RESERVED									
		RESERVED									
F4		RESERVED									
		RESERVED									
F3		RESERVED									
F2		RESERVED									
F1		RESERVED									
		RESERVED									
F0		RESERVED									
EF	W	anctl	--00 00-0	0	---	lsb1	lsb0	d2a_half	rc_osc2	---	afe_on
	W		---- 0000	1	---	---	---	~~osc2_res1~~	~~osc2_res0~~	~~osc2_inv1~~	~~osc2_inv0~~
	R			0	---	lsb1	lsb0	d2a_half	rc_osc2	---	afe_on
EE	W**	t2v	0000 0000	<t2r7	<t2r6	<t2r5	<t2r4	<t2r3	<t2r2	<t2r1	<t2r0
	R			t2v7	t2v6	t2v5	t2v4	t2v3	t2v2	t2v1	t2v0
ED	R/W	t2r	0000 0000	t2r7	t2r6	t2r5	t2r4	t2r3	y2r2	t2r1	t2r0
EC	W**	t1v	0000 0000	<t1r7	<t1r6	<t1r5	<t1r4	<t1r3	<t1r2	<t1r1	<t1r0
	R			t1v7	t1v6	t1v5	t1v4	t1v3	t1v2	t1v1	t1v0
EB	R/W	t1r	0000 0000	t1r7	t1r6	t1r5	t1r4	t1r3	t1r2	t1r1	t1r0
EA	R/W	wake1	0000 0000	w1.7	w1.6	w1.5	w1.4	w1.3	w1.2	w1.1	w1.0
E9	R/W	wake0	0000 0000	w0.7	w0.6	w0.5	w0.4	w0.3	w0.2	w0.1	w0.0
E8	R/W	ckctl	0000 1000	pdn	t2wake	fclk_on	clk_div1	clk_div0	slow_pclk	osc2_on	osc1_off
E7	R/W	p0ctlb	0000 0000	ctlb0.7	ctlb0.6	ctlb0.5	ctlb0.4	ctlb0.3	ctlb0.2	ctlb0.1	ctlb0.0
E6	R/W	p0ctla	0000 0000	ctla0.7	ctla0.6	ctla0.5	ctla0.4	ctla0.3	ctla0.2	ctla0.1	ctla0.0
E5	R	p0in	xxxx xxxx	pin0.7	pin0.6	pin0.5	pin0.4	pin0.3	pin0.2	pin0.1	pin0.0
E4	R/W	p0out	0000 0000	pout0.7	pout0.6	pout0.5	pout0.4	pout0.3	pout0.2	pout0.1	pout0.0
E3	R/W	p1ctlb	0000 0000	ctlb1.7	ctlb1.6	ctlb1.5	ctlb1.4	ctlb1.3	ctlb1.2	ctlb1.1	ctlb1.0
E2	R/W	p1ctla	0000 0000	ctla1.7	ctla1.6	ctla1.5	ctla1.4	ctla1.3	ctla1.2	ctla1.1	ctla1.0
E1	R	p1in	xxxx xxxx	pin1.7	pin1.6	pin1.5	pin1.4	pin1.3	pin1.2	pin1.1	pin1.0
E0	R/W	p1out	0000 0000	pout1.7	pout1.6	pout1.5	pout1.4	pout1.3	pout1.2	pout1.1	pout1.0

Address	R/W	Name	Reset	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DF	R/W	p2ctlb	0000 0000	ctlb2.7	ctlb2.6	ctlb2.5	ctlb2.4	ctlb2.3	ctlb2.2	ctlb2.1	ctlb2.0
DE	R/W	p2ctla	0000 0000	ctla2.7	ctla2.6	ctla2.5	ctla2.4	ctla2.3	ctla2.2	ctla2.1	ctla2.0
DD	R	p2in	xxxx xxxx	pin2.7	pin2.6	pin2.5	pin2.4	pin2.3	pin2.2	pin2.1	pin2.0
DC	R/W	p2out	0000 0000	pout2.7	pout2.6	pout2.5	pout2.4	pout2.3	pout2.2	pout2.1	pout2.0
DB	W**	t3v	0000 0000	<t3r7	<t3r6	<t3r5	<t3r4	<t3r3	<t3r2	<t3r1	<t3r0
	R			t3v7	t3v6	t3v5	t3v4	t3v3	t3v2	t3v1	t3v0
DA	R/W	t3r	0000 0000	t3r7	t3r6	t3r5	t3r4	t3r3	t3r2	t3r1	t3r0
D9	W	t3ctl	0000 000	t3_on	polarity	p0.1_src	t3_gated	t3_ps3	t3_ps2	t3_ps1	t3_ps0
D8	R/W	pwmData	0000 0000	pwmd09	pwmd08	pwmd07	pwmd06	pwmd05	pwmd04	pwmd03	pwmd02
D7	R/W	pwmCtrl	0000 00-0	pwmd01	pwmd00	tenBits	---	period1	period0	---	pwm_on
D6	R/W	clkExt	0000 0000	rom_0Ws	MTclk_on	movx_4ws	L1clk_on	t1_ps3	t1_ps2	t1_ps1	t1_ps0
D5	R/W	sysctl	0000 0---	wd_ps1	wd_ps0	brnout	afe_g1	afe_g0	---	p02Edge	p00Edge
D4	W	cmpCtl	---- 0000	---	---	---	---	mux_sel	ccs2	ccs1	ccs0
	R			compA+	compB+	---	---	mux_sel	ccs2	ccs1	ccs0
D3	R/W	cmpRef	---- 0000	---	---	---	---	crv03	crv02	crv01	crv00
D2	R/W	ExtAdd	--00 0000	---	---	cb1	rw	eda19	eda18	eda17	eda16
D1	R/W	Debug1	0000 0000								
D0	R/W	Debug0	0000 0000								
CF	R/W	flagsHold	0000 0000	carry	zero	sign	trap	---	---	---	gie
CE	W	awcCtl	0000 0000	pwrl	---	thrh2	thrh1	thrh0	thrl2	thrl1	thrl0
	R			pwrl	detect	thrh2	thrh1	thrh0	thrl2	thrl1	thrl0
CD	W	awmode	---0 0000	---	---	---	md1	md0	cfg2	cfg1	cfg0
	R			aws2	aws1	aws0	md1	md0	cfg2	cfg1	cfg0
CC		(unused)									
CB		(unused)									
CA		(unused)									
C9		(unused)									
C8		RESERVED									
		RESERVED									
C7		RESERVED									
C6		RESERVED									
C5		RESERVED									
C4		RESERVED									
C3		RESERVED									
		RESERVED									
C2		RESERVED									
		RESERVED									
C1		RESERVED									
		RESERVED									
C0		RESERVED									
		RESERVED									

Ordering Information

Part	Shipping P/N	Marketing P/N	Description
RSC-4000 Die	65-xxxx	C4xxxx	Tested, Singulated RSC-4000 die in waffle pack
RSC-4128 Die	65-xxxx	C4xxxx	Tested, Singulated RSC-4128 die in waffle pack
RSC-4256 Die	65-xxxx	C4xxxx	Tested, Singulated RSC-4256 die in waffle pack
RSC-4000 LQFP	65-xxxx	C4xxxx	RSC-4000 100 pin 14 x 14 x 1.4 mm LQFP
RSC-4128 LQFP	65-xxxx	C4xxxx	RSC-4128 48 pin 7 x 7 x 1.4 mm LQFP
RSC-4256 LQFP	65-xxxx	C4xxxx	RSC-4256 48 pin 7 x 7 x 1.4 mm LQFP

The Interactive Speech™ Product Line

The Interactive Speech line of ICs and software was developed to "bring life to products" through advanced speech recognition and audio technology.
The Interactive Speech Product Line was designed for consumer telephony products and cost-sensitive consumer electronic applications such as home electronics, personal security, and personal communication.
The product line includes award-winning RSC series general-purpose microcontrollers and tools, SC series of speech microcontrollers, plus a line of easy-to-implement chips that can be pin-configured or controlled by an external host microcontroller. Sensory's software technologies run on a variety of microcontrollers and DSPs.

RSC Microcontrollers and Tools

The RSC product line contains low-cost 8-bit speech-optimized microcontrollers designed for use in consumer electronics. All members of the RSC family are fully integrated and include A/D, pre-amplifier, D/A, ROM, and RAM circuitry. The RSC family can perform a full range of speech/audio functions including speech recognition, speaker verification, speech and music synthesis, and voice record/playback. The family is supported by a complete suite of evaluation tools and development kits.

SC Microcontrollers and Tools

The **SC-6x** product line features the highest quality speech synthesis ICs at the lowest data rate in the industry. The line includes a 12.32 MIPS processor for high-quality low data-rate speech compression and MIDI music synthesis, with plenty of power left over for other processor and control functions. Members of the SC-6x line can store as much as 37 minutes of speech on chip and include as much as 64 I/O pins for external interfacing. Integrating this broad range of features onto a single chip enables developers to create products with high quality, long duration speech at very competitive price points.

Application Specific Standard Products (ASSPs)

- ***Voice Direct™ 364*** provides inexpensive speaker-dependent speech recognition and speech synthesis. This easy-to-use, pin-configurable chip requires no custom programming and can recognize up to 60 trained words in slave mode, and 15 words in stand-alone mode. Ideal for speaker-dependent command and control of household consumer products, Voice Direct 364 is part of a complete product line that includes the IC, module, and Voice Direct 364 Speech Recognition Kit.
- ***Voice Extreme™*** simplifies the creation of fully custom speech-enabled products by offering developers the capability of programming the chip in a high-level C-like language. Program code, speech data, and even record and playback information can be stored on a single off-chip Flash memory. Based on Sensory's RSC-364 speech processor, Voice Extreme includes a highly efficient on-chip code interpreter, and is supported by a comprehensive suite of low-cost development tools.

Software and Technology

- ***Voice Activation™*** micro footprint software provides advanced speech technology on a variety of microcontroller and DSP platforms. A flexible design with a broad range of technologies allows manufacturers to easily integrate speech functionality into consumer electronic products.
- ***Fluent Speech™*** small footprint software recognizes up to 50,000 words; offers Animated Speech with the ability to automate enunciation and articulation; performs text-to-speech synthesis in either male or female voices; provides noise and echo cancellation, performs Wordspotting for natural language usage; offers telephone barge-in; and provides continuous digit recognition.

Important notices

Reasonable efforts have been made to verify the accuracy of information contained herein, however no guarantee can be made of accuracy or applicability. Sensory reserves the right to change any specification or description contained herein.

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