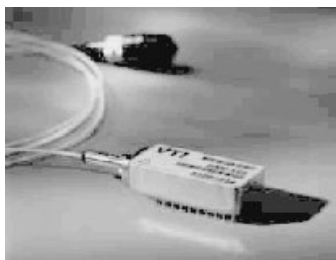


# Optical Receiver Products

## RX-180 (Formerly SRM and RXM Product Families)



**Description:** The RX-180 is a single-rate fully integrated fiber-optic receiver module available with SAW based clock & data retiming. It is ideally suited for SONET/SDH and other fiber optic transport applications that demand superior performance and stability.

### Features

- SONET OC-3 and OC-12 and SDH STM-1/STM-4 Compatible
- SAW Filter Clock Recovery and Data Retiming Available
- 10ps Typical Output Jitter (@622MHz)
- PECL Clock and Data Outputs
- Multisource 20 pin DIL Footprint
- Single +5 Volt Supply
- CMOS Loss of Signal Flag
- Operation at 1300nm and 1500nm
- +45° to -85°C Operation
- Wide Dynamic Range
- Custom Data Rates Available from 124 to 750 Mb/s.

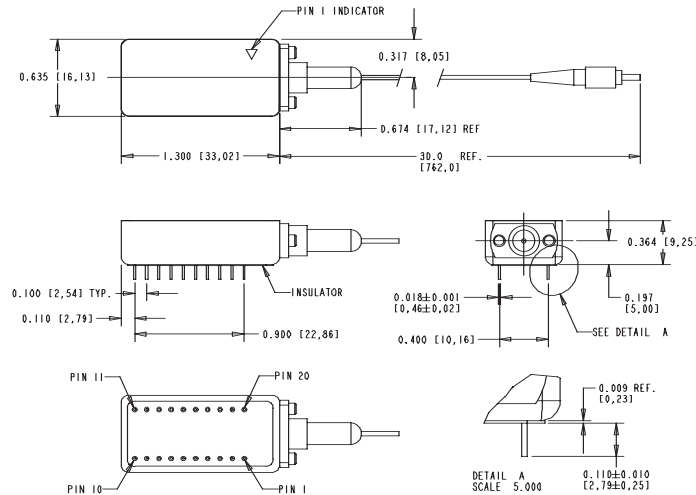
### Performance Characteristics

Parameter	Symbol	Min.	Typical	Max	Unit
Input Rate <sup>1</sup> 155 Mb 622 Mb	fo fo	155.486 621.950	155.520 622.080	155.551 622.204	Mb/s Mb/s
Operating Temperature	To	-40		+85	°C
Power Supply Voltage	Vcc	4.5	5.0	5.0	V
Pin Detector Bias Voltage (pin10)	V <sub>D</sub> V <sub>D</sub>	0 0	0 5.0	5.0 5.5	V V
Power Supply Current	Icc			300	mA
Data and Clock Output Level <sup>2</sup> Low High	VOL VOH	Vcc-1.95 Vcc-1.03		Vcc-1.63 Vcc-0.88	V V
Clock to Data Alignment <sup>3</sup>	TCDA	-100		+100	ps
Data and Clock Output Rise and Fall Times <sup>4</sup>	tr, tf	275	375	575	ps
Output Clock Duty Cycle	Duty	45	50	55	%
155 Mb Received Power Level Flag Decreasing Optical Power Increasing Optical Power 622 Mb Decreasing Optical Power Increasing Optical Power	LOS		-39 -36 -34 -31		dBm dBm dBm dBm
Flag Hysteresis	Hyst		3		dB
Acquisition Time <sup>5</sup>	TA			2	ms
Output Clock Random Jitter <sup>6</sup> 155 Mb 622 Mb	Jc Jc		17 10		ps rms ps rms
Minimum Average Sensitivity <sup>7</sup> 155 Mb 622 Mb	Sens Sens	-34 -31	-37 -33		dBm dBm
Maximum Optical Input <sup>7</sup> 155 Mb 622 Mb Input Wavelength	P <sub>MAX</sub> P <sub>MAX</sub> λ	1100		0 -6 1580	dBm dBm nm

1. Other data rates are available in the 124 to 750 Mb/s range. Please contact VI for further details.
2. Measured with a load of  $R_L = 50\Omega$  to  $V_{cc} - 2V$ . See PECL and ECL interfaces. ECL levels are specified for dc measurement, an additional tolerance of 50 mV should be included for dynamic measurements.
3. Alignment of clock and data outputs.
4. Measured at 20% to 80% levels.
5. Time required to achieve valid data and clock outputs with a transition density of at least 50%.
6. Measured with an input data pseudorandom word  $2^{23}-1$ . For a BER less than  $1E-10$  measured using  $2^{23}-1$  pseudorandom word and a 10% average optional duty cycle and a 10dB extinction ratio.
7. For a BER less than  $1E-10$  measured using a  $2^{23}-1$  pseudorandom word and a 50% average optical duty cycle and a 10dB extinction ratio.

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### Outline Drawing



### Pin out information

4	Clock	PECL Recovered Clock Output. (NUC for non-CDR version)
5	Clock	PECL Complementary Recovered Clock Output. (NUC for non-CDR version)
7	Data	PECL Retimed Data Output.
9	Data	PECL Complementary Retimed Data Output.
10	V <sub>D</sub>	Detector Anode. Bias. Ground or apply +5 Volt bias through a series resistor for received optical power monitoring <sup>1</sup> .
11	V <sub>CC</sub>	+5 Volt Supply Voltage.
12	Flag	Input Signal Level Status. This CMOS output switches low when the received optical power falls below the status minimum optical power level.
14	Flag	Complementary Input Signal Status. CMOS complement of Flag.
1,2,3,6,8,13,15,16.	GND	Ground
17,18,19,20	NC	No User Connection.

1. By connecting pin 10 to +5 Volt through a series resistor (e.g. 1kΩ), the received optical power can be monitored as a voltage drop across the resistor.

Optical

### Ordering Information

