ROCKWELL SCIENTIFIC

RDA012

12 Bit 1 GS/s DAC

Features

- 12 Bit 1 GS/s D/A Converter
- 65 dB SFDR (f_o = 333 MHz, f_{clk} = 1GHz)
- 10 Bit Static Linearity
- ECL Compatible Data Inputs
- Power Supply: -5.2V ± 0.3V
- Input Code Format: Offset Binary
- Output Swing: 600 mV @ 50 Ω Termination
- Reference I/O Pin for Accurate Full-Scale Adjustment
- Available in 32-Pin QFP or Die
- Evaluation Board and Test Fixture Available

Applications

- Test Instrumentation Equipment
- Radar
- Software Radio
- Display Generation
- Waveform and Signal Synthesis
- Video Signal Reconstruction
- Cellular Base Stations
- Direct Digital Synthesis

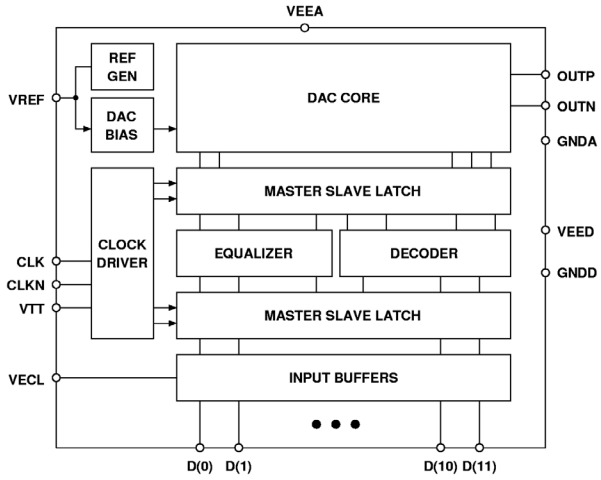


Figure 1. Functional Diagram

Product Description

The RDA012 is a high performance 12 Bit digital-to-analog converter (DAC) with a data update rate over 1GS/s. Fabricated in an 80 GHz f_T GaAs HBT process, the RDA012 has been optimized for ultra-high speed applications, achieving 65dB of spurious-free dynamic range (SFDR) at 1 GS/s and f_o of 333MHz. The DAC utilizes a segmented current source to reduce glitch energy and to achieve high linearity performance. For better dynamic performance, the DAC outputs are internally terminated with 50Ω resistance. It outputs a nominally full-scale current of 12mA when terminated with external 50Ω resistors.

Absolute Maximum Ratings

Supply Voltages
VEE to GND ..... -6 V to +1 V

Input Voltages
Data, VTT.....-6V to +1 V
CLK, CLKB.....-3V to +1 V

Output Voltages
Output Termination Voltage..... ±1 V

Temperature
Operating Temperature ..... -40 to +70 °C
Case Temperature ..... -15 to +85 °C
Junction Temperature ..... +125 °C
Lead, Soldering (10 Seconds)..... +220°C
Storage ..... -40 to 125 °C

Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, Note	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		12			Bits
Linearity	INL			± 4		LSB
Spurious Free Dynamic Ranges						
SFDR1		See Note 1	60	65		dBc
SFDR2		See Note 2	60	65		dBc
ANALOG OUTPUTS						
Full-Scale Output Range	V_{FSRS}	Single ended @ 50 Ω		600		mV
Full-Scale Output Range	V_{FSRD}	Differential @ 50 Ω		1200		mV
Output Current	I_{OUT}	See notes 3, 4	11.4	12.0	12.6	mA
CLOCK INPUTS						
Type		Differential ECL				
Clock Input Resistance	R_{CLK}		45	50	55	Ω
Maximum Frequency	FI_{MAX}		1000		1200	MHz
DATA INPUTS						
Data Input Level		ECL compliant, see Input Specifications				
POWER SUPPLY						
Negative Supply	VEED, VEEA		-5.5	-5.2	-4.9	V
Power Dissipation	P_D			1.8	1.9	W
OPERATING TEMPERATURE						
Junction Temperature	T_J	See note 5	-40		125	°C
Ambient Temperature	T_A		-40		70	°C

[1] SFDR1 is the ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over the frequency band 1/8 f_{clk} - 3/8 f_{clk} with the output frequency equal to 1/4 or 1/3 f_{clk} + 5MHz, with internal reference.

[2] SFDR2 is the spurious free dynamic range measured over the entire RDA012 spectrum.

[3] The DAC current is generated from an internal reference that is both temperature and supply dependent. Internal reference can change up to ±2% by changing the supply voltage within the specified range, and also can change up to ±5% according to operating temperature changes.

[4] The change in temperature and supply can be minimized by using a precision external voltage reference source with an additional pin. Refer the operating diagram in figure 3.

[5] The part is designed to function within a junction temperature range of -55 ~ 125°C. For the best performance, operation within the specified temperature range with a proper heat sink attached to the device is recommended.

Input Specifications

Input Level	Notes	MIN	TYP	MAX	UNITS
VECL	Emitter Coupled Logic reference Voltage	-2	-1.3	-0.5	V
V_{IHD}	Differential Input Voltage High	150			mV
V_{ILD}	Differential Input Voltage Low			-150	mV
V_{IH}	Input Voltage High			-0.3	V
V_{IL}	Input Voltage Low	-2.2			V

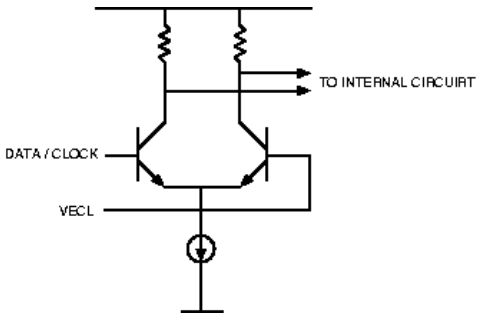


Figure 2. The internal data and clock input circuit of the RDA012 DAC

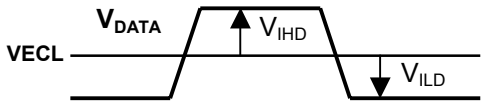


Figure 3. Input voltage level diagram for the RDA012 DAC

Pin Description and Pin Out

P/I/O	NAME	FUNCTION
P	GND	Power Supply Ground
I	D0.....D11	Digital Data Input
P	VEEA	Negative Analog Power Supply, -5.2V ± 5%
O	OUT	Analog Output
O	OUTN	Complementary Analog Output
P	VECL	-1.3V Voltage Reference
P	VREF	-2 V External Voltage Reference
I	CLK	Input Clock
I	CLKB	Complementary Input Clock
P	VTT	Termination Node
P	VEED	Negative Digital Power Supply, -5.2V ± 5%

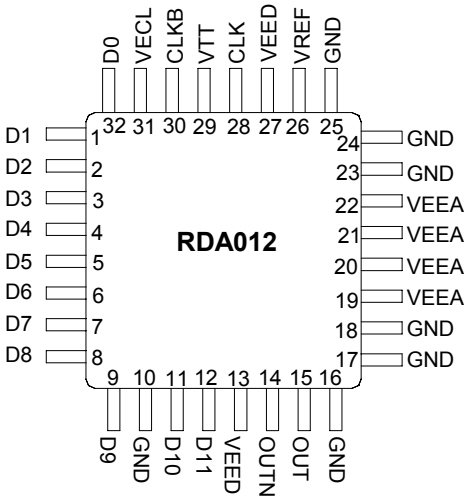


Figure 4. Pin configuration (top view, not to scale) 32-lead glass-wall metallized ceramic quad flat pack

Theory of Operation

For best dynamic and static performance, the RDA012 DAC employs 4 Bit segmentation. The ECL compatible 12 Bit digital data inputs are latched by master-slave flip-flops immediately after the input buffer to reduce the data skew. The 4 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 8 LSB data bits are transported through the delay equalizer block. The digital data are then synchronized again by a second master-slave flip-flop to reduce the switching glitch. The decoded 4 MSB data drive 15 identical current switches, and the 8 LSB data drive 8 current switches. The output nodes from the LSB current switches are connected to the analog output through an R-2R ladder to generate the binary output.

The RDA012 DAC provides output terminated at 50Ω, illustrated in an equivalent circuit in Figure 5. The output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF.}$ An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience, and the reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

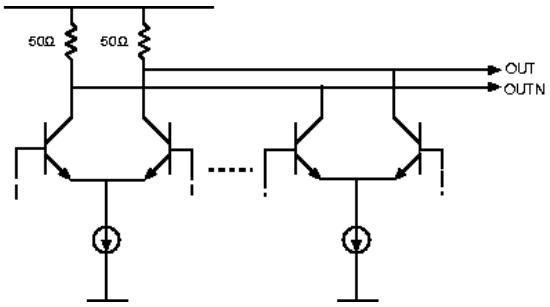


Figure 5. The RDA012 equivalent output circuit

Typical Operating Circuit

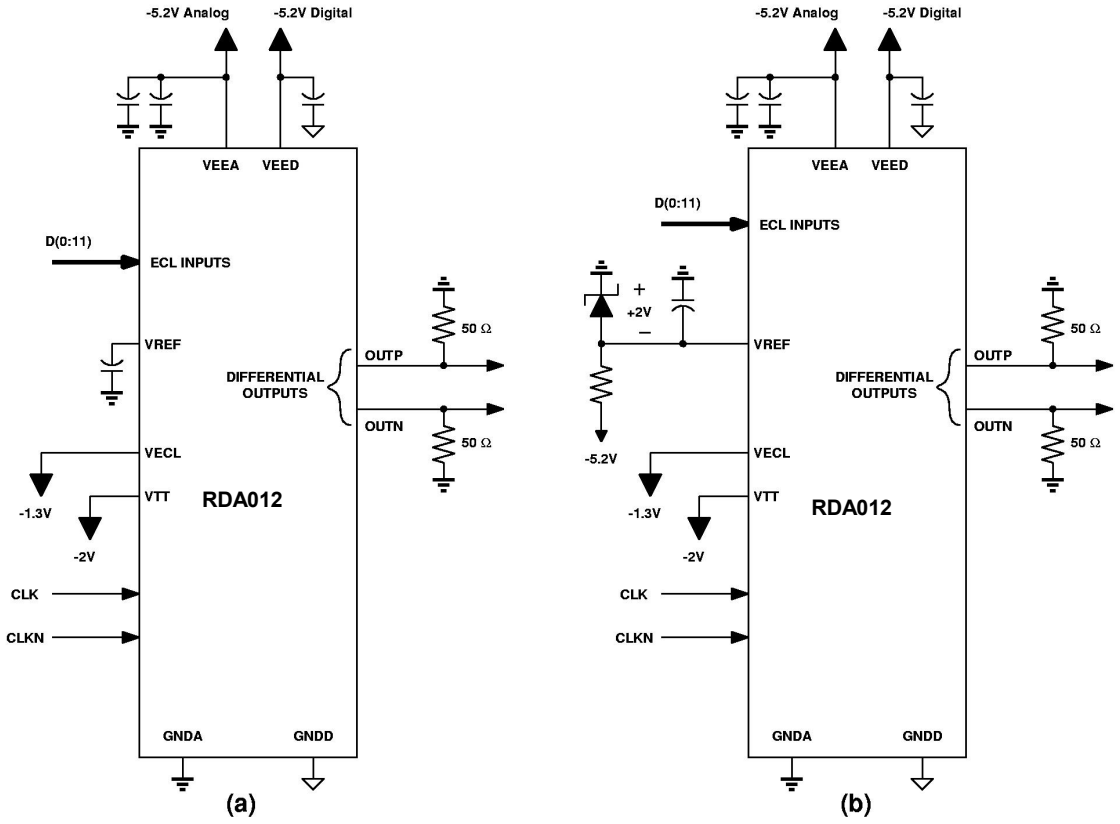


Figure 6. Typical operating circuit (a) using internal reference and (b) external voltage reference

Die Plot and Pad Arrangement

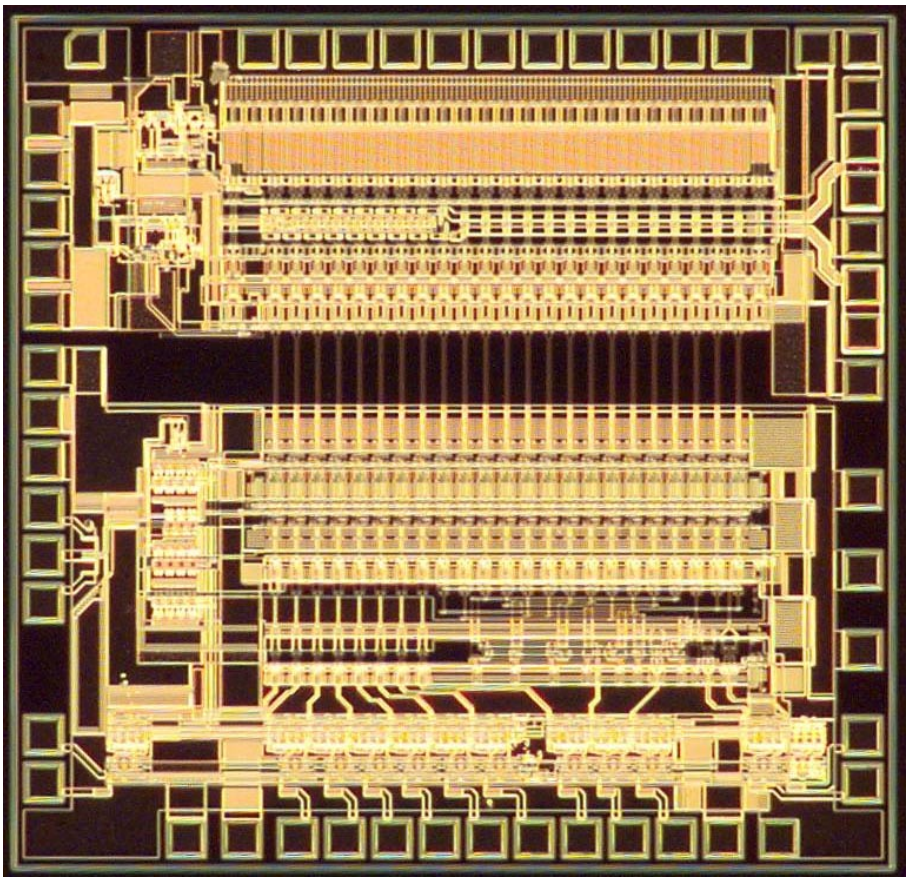
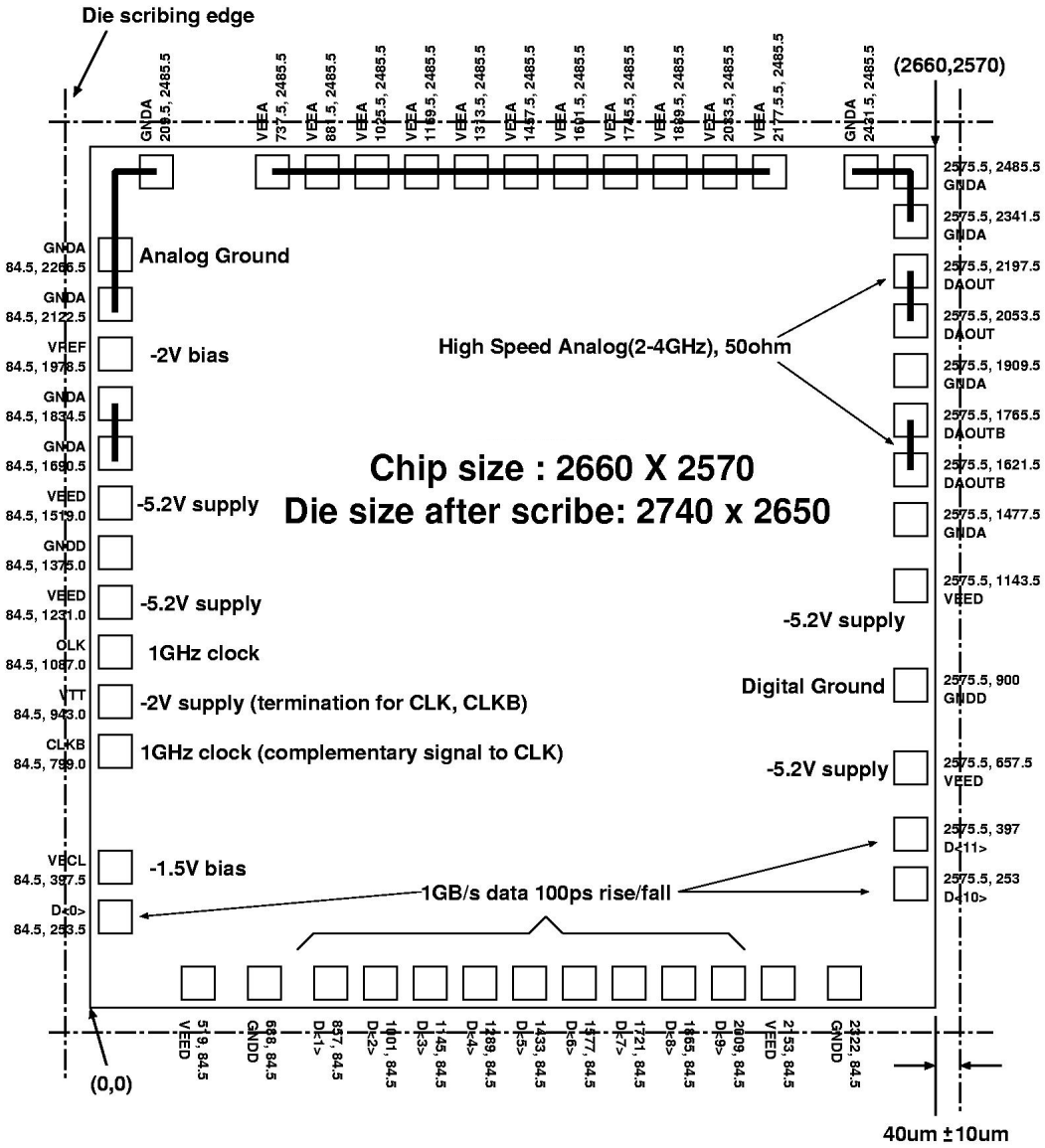


Figure 7. RDA012 Die Photo, after scribe, 2.740mm x 2.650mm



Note : Pad location is relative to the Chip size.
Die will be scribed with the scribe lane width of 80um, resulting in a 40um space on each side.

Figure 8. Pad Arrangement Block Diagram

Typical† Performance Characteristics

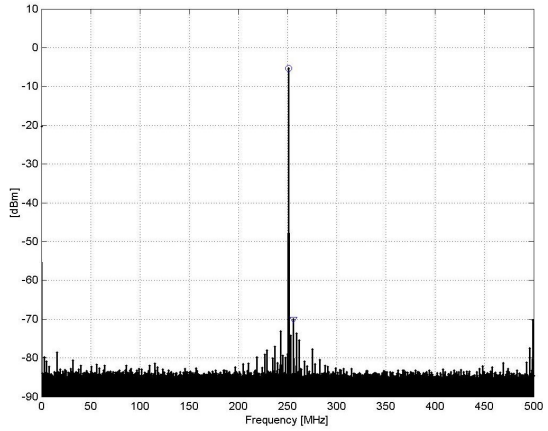


Figure 9. DAC output spectrum, f_o = 250 MHz, f_{clk} = 1GHz

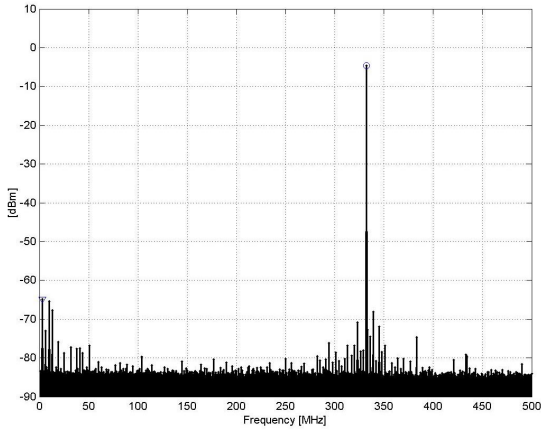


Figure 10. DAC output spectrum, f_o = 333 MHz, f_{clk} = 1GHz

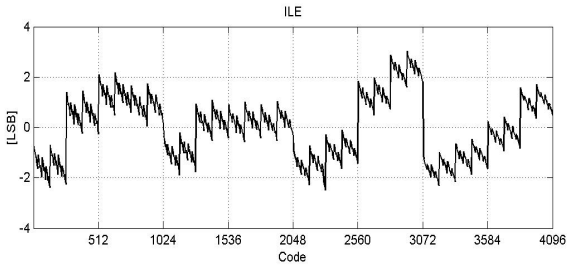


Figure 11. DAC integral linearity error in 12 bit scale

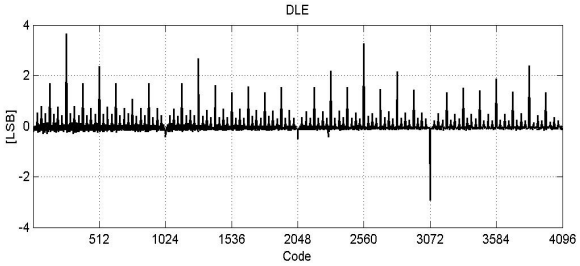


Figure 12. DAC differential linearity error in 12 bit scale

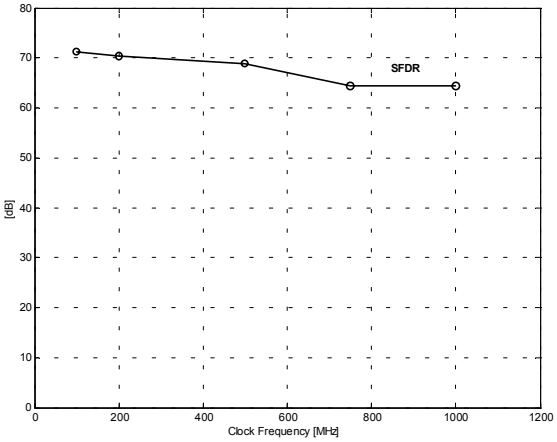


Figure 13. SFDR‡ vs. Clock Frequency, f_o = 1/3 f_{clk}

† VREF is –2V and output is Full-Scale Range (FSR)

‡ Spurious Free Dynamic Range (SFDR) is the ratio of the magnitude of the first (main) harmonic and the highest other harmonic measured over $1/8f_{clk}$ – $3/8f_{clk}$ bandwidth

Package Information

The RDA012 is packaged in a 32-lead metal-ceramic-base glass-sidewall Quad Flat-Pack (QFP), with a gull-winged lead form. The thermal impedance (junction to base) is approximately 15 °C/W. The lid is sealed with epoxy.

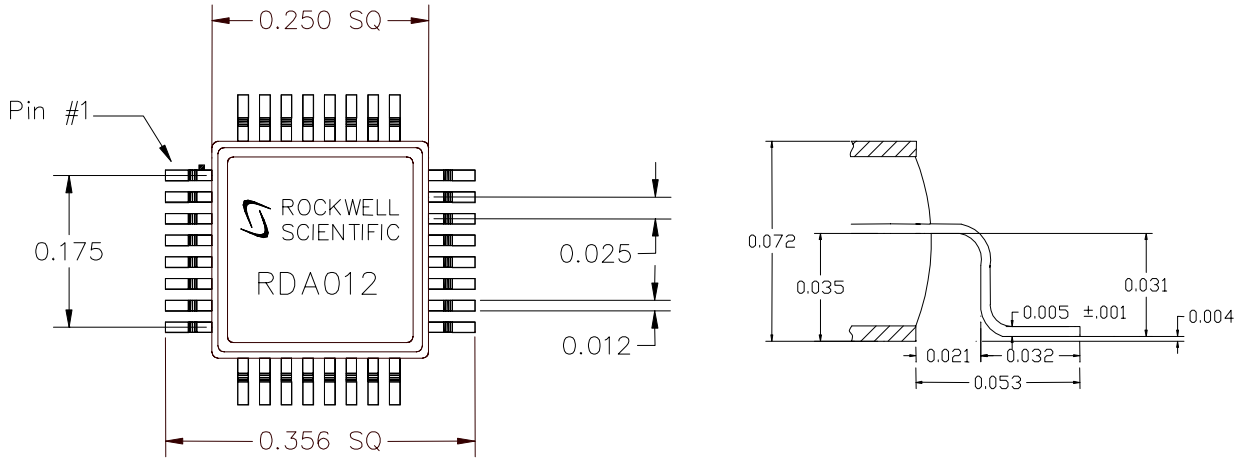


Figure 14. Metal-Ceramic Quad Flat Pack (QFP) with lead form. All dimensions are shown in inches, with tolerance ±0.002 inch.

Ordering Information

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
RDA012QFP	32-Lead QFP	-30 to +70 °C
RDA012DIE	Die	0 to +100 °C