Dual Regulators - Standard Buck PWM DC-DC and Linear Controller

General Description

The RT9204/A is a dual power controllers designed for high performance graphics cards and computer applications. The IC integrates a standard buck controller, a linear regulator driver and protection functions into a small 8-pin package.

The RT9204/A uses an internal compensated voltage mode PWM control for simple application design. An internal 0.8V reference allows the output voltage to be precisely regulated to low voltage requirement. A fixed 600kHz oscillator reduce the component size for saving board area.

The RT9204/A protects the converter and regulator by monitoring the output under voltage.

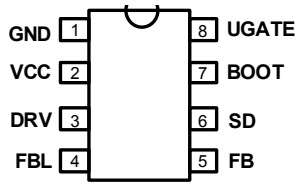
Applications

- Motherboard Power Regulation for Computers
- Subsystems Power Supplies
- Cable Modems, Set Top Box, and DSL Modems
- DSP and Core Communications Processor Supplies
- Memory Power Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

Features

- **Operate from 5V**
- **0.8V Internal Reference**
- **Voltage Mode PWM Control**
- **Fast Transient Response**
- **Fixed 600kHz Oscillator Frequency**
- **Full 0~100% Duty Cycle**
- **Internal Soft Start**
- **Internal PWM Loop Compensation**

Pin Configurations

Part Number	Pin Configurations
RT9204/ACS (Plastic SOP-8)	TOP VIEW 

Ordering Information

RT9204/A□ □

- Package Type
  - S : SOP-8
- Operating Temperature Range
  - C : Commercial Standard
- UVP : Hiccup Mode
- UVP : Latch Mode

Typical Application Circuit

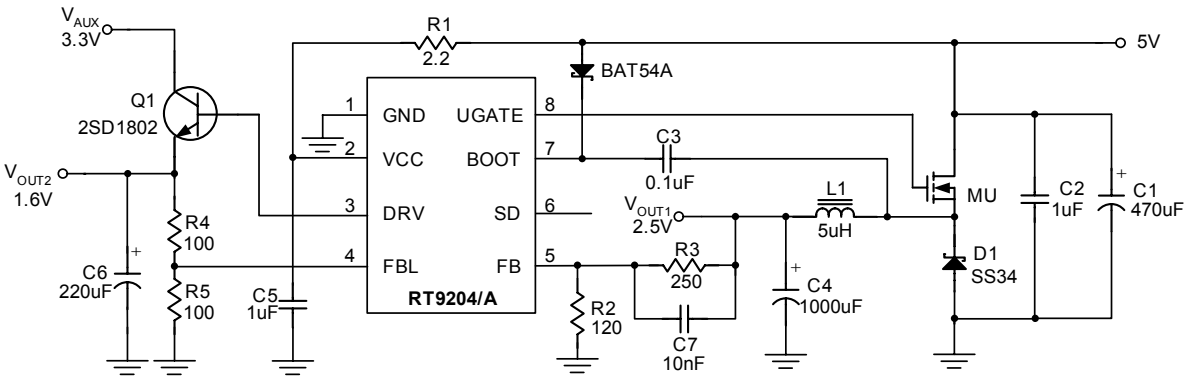


Fig.1 RT9204/A powered from 5V only

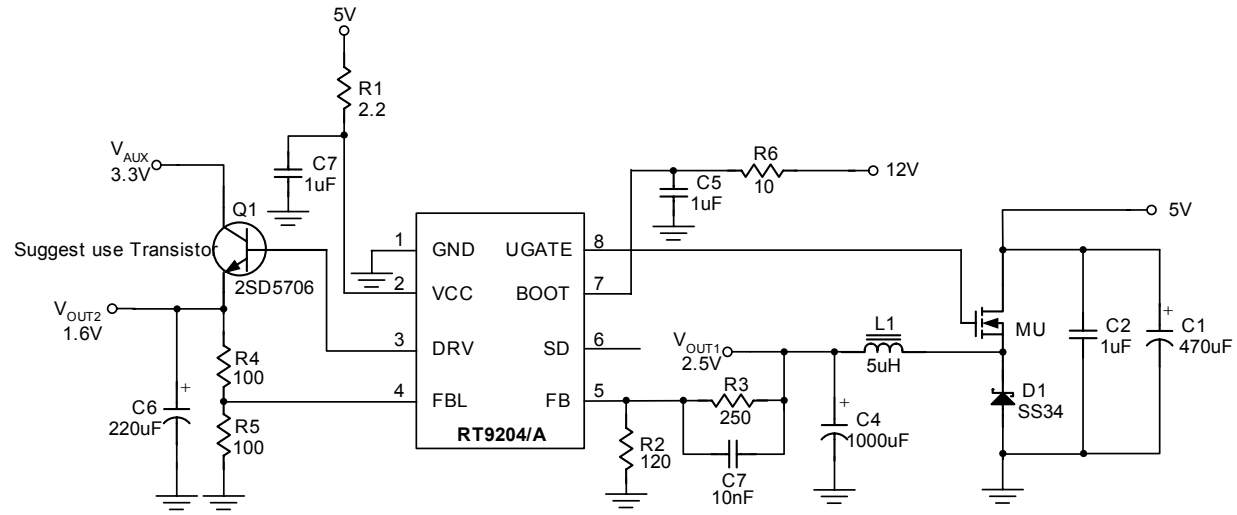
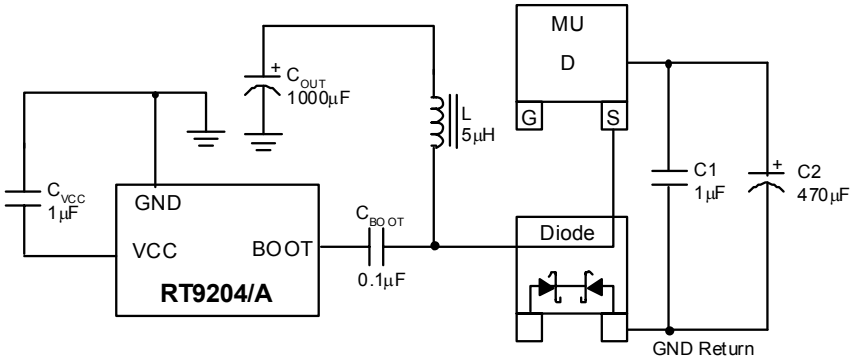


Fig.2 RT9204/A powered from 12V

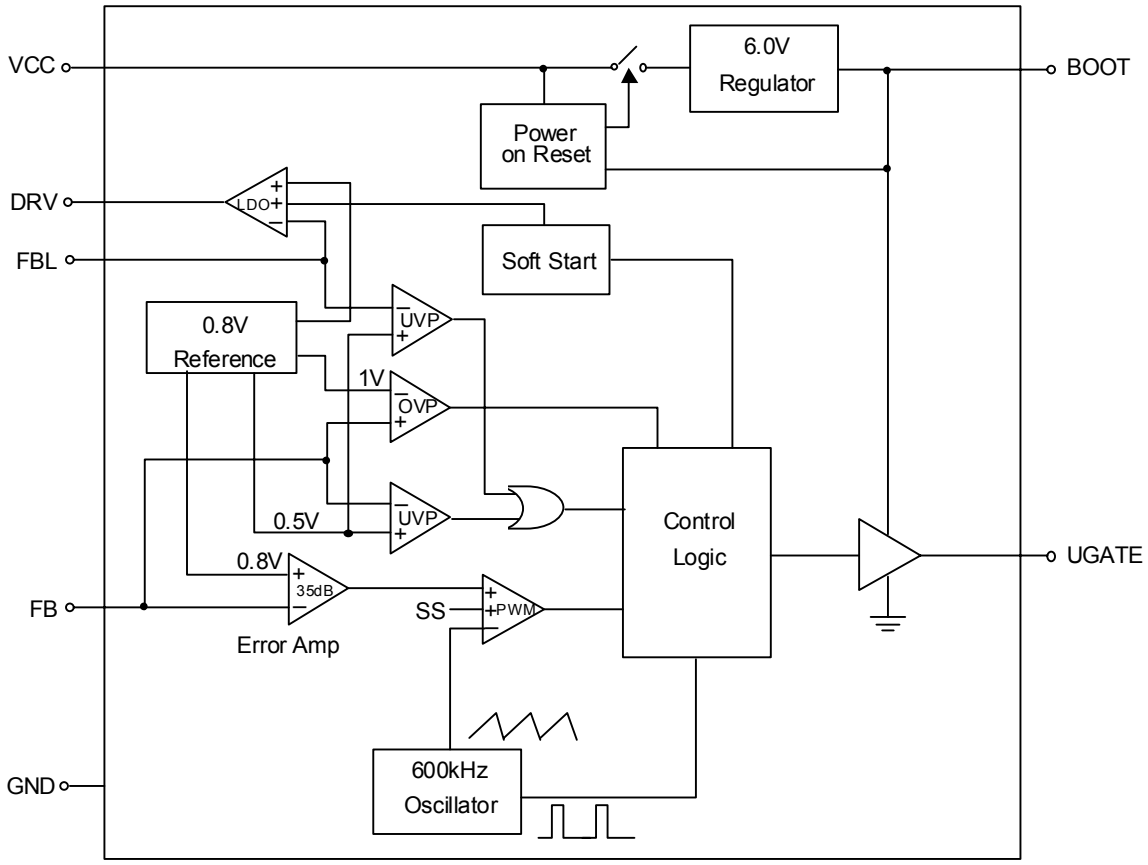


Layout Placement

Layout Notes

1. Put C_1 & C_2 to be near the MU drain and ML source nodes.
2. Put RT9204/A to be near the C_{OUT}
3. Put C_{BOOT} as close as to BOOT pin
4. Put C_{VCC} as close as to VCC pin

Function Block Diagram



Absolute Maximum Ratings

- Supply Voltage VCC ---------- 7V
- BOOT & UGATE to GND ---------- 15V
- Input, Output or I/O Voltage ---------- GND−0.3V ~ 7V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 ---------- 0.625W
- Package Thermal Resistance
  SOP-8, θ_{JA} ---------- 160°C/W
- Ambient Temperature Range ---------- 0°C ~ +70°C
- Junction Temperature Range ---------- -40°C ~ +125°C
- Storage Temperature Range ---------- -65°C ~ +150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C

CAUTION:

Stresses beyond the ratings specified in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

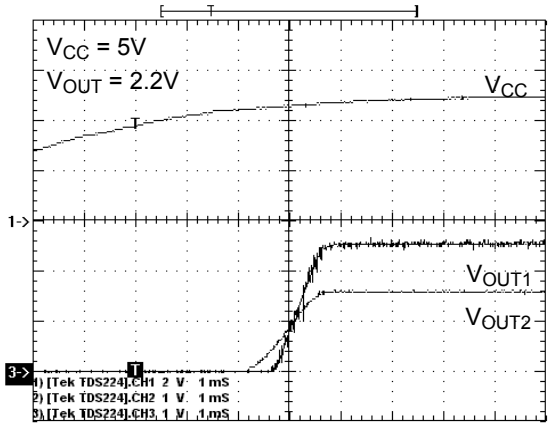
Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, Unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
VCC Supply Current						
Nominal Supply Current	I_{CC}	UGATE, LGATE open	--	3	--	mA
VCC Regulated Voltage	V_{CC}	V_{BOOT}=12V	--	6	--	V
Power-On Reset						
Rising VCC Threshold			3.75	4.1	4.35	V
VCC Threshold Hysteresis			--	0.5	--	V
Reference						
Reference Voltage		Both FB & FBL	0.784	0.8	0.816	V
Oscillator						
Free Running Frequency			550	600	650	KHz
Ramp Amplitude	ΔV_{OSC}		--	1.75	--	V_{P-P}
PWM Error Amplifier						
DC Gain			--	35	--	dB
PWM Controller Gate Driver						
Upper Drive Source	R_{UGATE}	V_{BOOT} = 12V; V_{BOOT} - V_{UGATE} = 1V	--	7	--	Ω
Upper Drive Sink	R_{UGATE}	V_{UGATE} = 1V	--	5	--	Ω
Linear Regulator						
DRV Driver Source		V_{DRV} = 2V	100	--	--	mA
Protection						
FB Over-Voltage Trip		FB Rising	--	1	--	V
FB & FBL Under-Voltage Trip		FB & FBL Falling	--	0.5	--	V
Soft-Start Interval			--	1	--	mS
SD Pin Threshold		VCC = 5V	--	1.5	--	V
SD pin Sink Current		VCC = 5V	--	40	--	μA

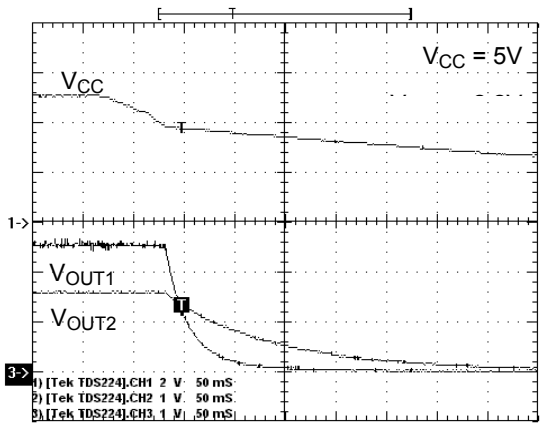
Typical Operating Characteristics

Power On



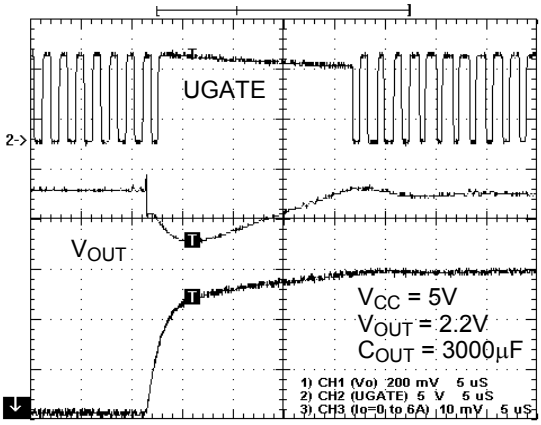
Time

Power Off



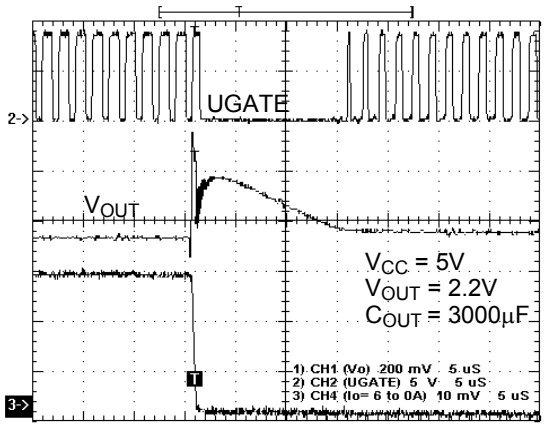
Time

Load Transient



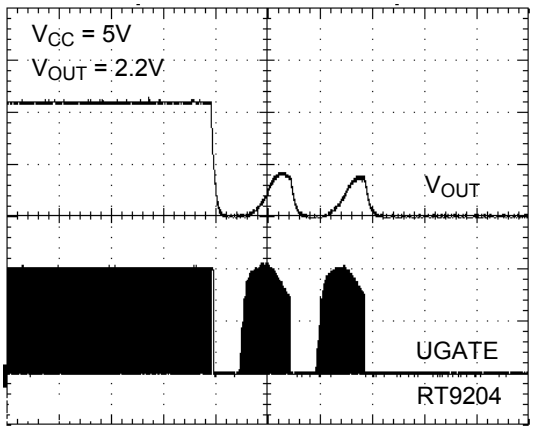
Time

Load Transient



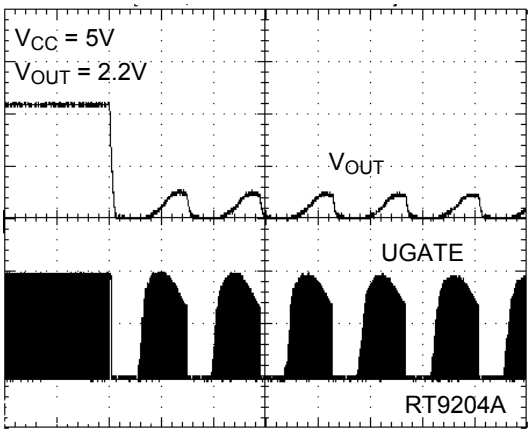
Time

Short Hiccup (Latch Mode)



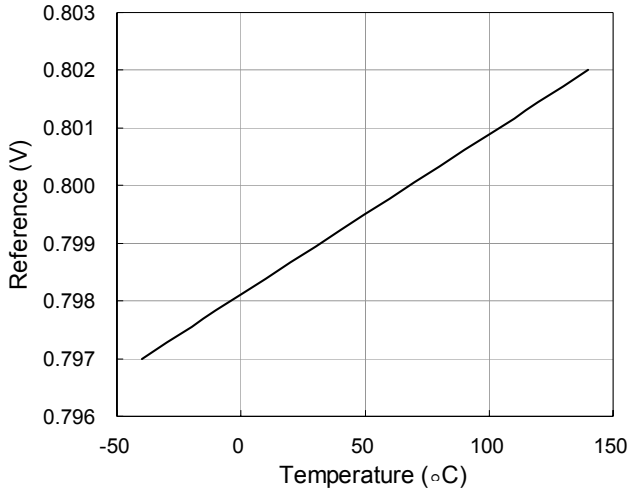
Time (5ms/Div)

Short Hiccup

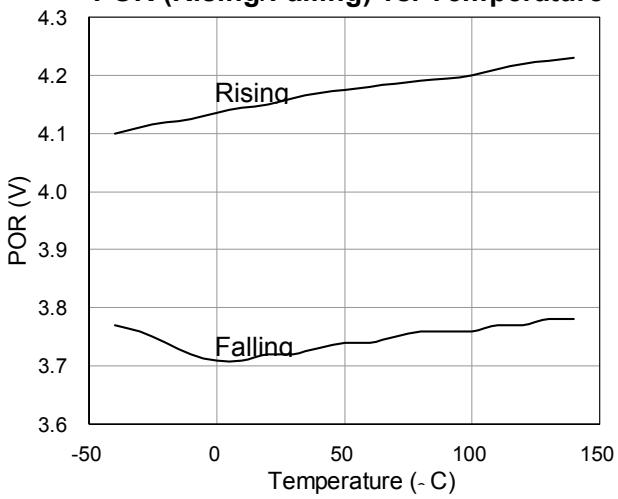


Time (2ms/Div)

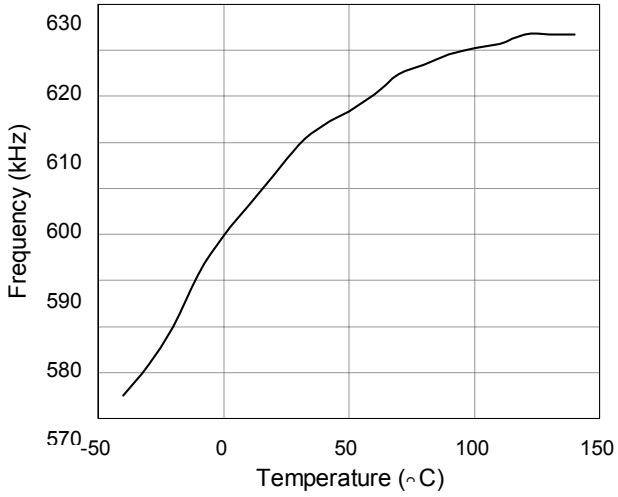
Reference vs. Temperature



POR (Rising/Falling) vs. Temperature



Oscillator Frequency vs. Temperature



Functional Pin Description

GND (Pin 1)

Signal and power ground for the IC. All voltage levels are measured with respect to this pin.

VCC (Pin 2)

This is the main bias supply for the RT9204/A. This pin also provides the gate bias charge for the lower MOSFETs gate. The voltage at this pin monitored for power-on reset (POR) purpose. This pin is also the internal 6.0V regulator output powered from BOOT pin when BOOT pin is directly powered from ATX 12V.

DRV (Pin 3)

This pin is linear regulator output driver. Connect to external bypass NPN transistor base or NMOSFET gate terminal.

FBL (Pin 4)

This pin is connected to the linear regulator output divider. This pin also connects to internal linear regulator error amplifier inverting input and protection monitor.

FB (Pin 5)

This pin is connected to the PWM converter's output divider. This pin also connects to internal PWM error amplifier inverting input and protection monitor.

SD (Pin 6)

Active low design with a 40μA pull low current source. Pull this pin to VCC to shutdown both PWM and linear regulator.

BOOT (Pin 7)

This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-channel MOSFET when operating at a single 5V power supply. This pin also could be powered from ATX 12V, in this situation, an internal 6.0V regulator will supply to VCC pin for internal voltage bias.

UGATE (Pin 8)

Connect UGATE pin to the PWM converter's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.

Functional Description

The RT9204/A operates at either single 5V power supply with a bootstrap UGATE driver or 5V/12V dual-power supply form the ATX SMPS. The dual-power supply is recommended for high current application, the RT9204/A can deliver higher gate driving current while operating with ATX SMPS based on dual-power supply.

The Bootstrap Operation

In a single power supply system, the UGATE driver of RT9204/A is powered by an external bootstrap circuit, as the Fig.3. The boot capacitor, C_{BOOT}, generates a floating reference at the PHASE node. Typically a 0.1μF C_{BOOT} is enough for most of MOSFETs used with the RT9204/A. The voltage drop between BOOT and PHASE node is refreshed to a voltage of VCC – diode drop (V_D) while the low side MOSFET turning on.

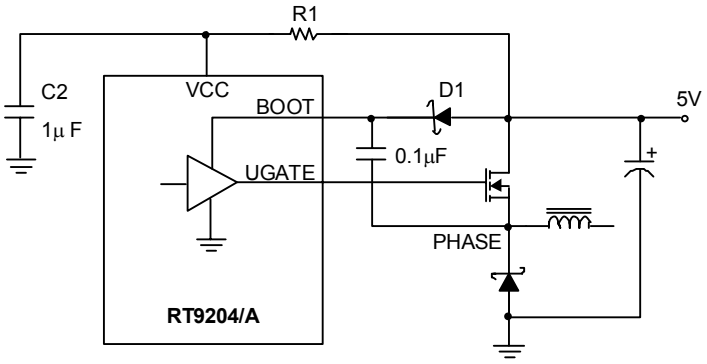


Fig.3 Single 5V power Supply Operation

Dual Power Operation

The RT9204/A was designed to regulate a 6.0V at VCC pin automatically when BOOT pin is powered by 12V. In a system with ATX 5V/12V power supply, the RT9204 is ideal for higher current application due to the higher gate driving capability, V_{UGATE} = 7V. A RC (10Ω/1μF) filter is also recommended at BOOT pin to prevent the ringing induced from fast power on, as shown in Fig.4.

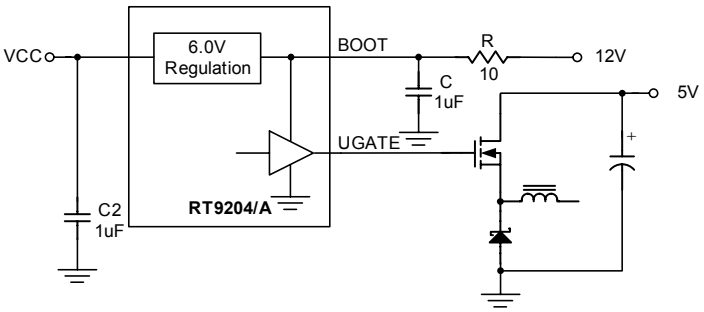


Fig.4 Dual Power Supply Operation

Power On Reset

The Power-On Reset (POR) monitors the supply voltage (normal +5V) at the VCC pin and the input voltage at the OCSET pin. The VCC POR level is 4.1V with 0.5V hysteresis and the normal level at OCSET pin is 1.5V (see over-current protection). The POR function initiates soft-start operation after all supply voltages exceed their POR thresholds.

Soft Start

A built-in soft-start is used to prevent surge current from power supply input during power on. The soft-start voltage is controlled by an internal digital counter. It clamps the ramping of reference voltage at the input of error amplifier and the pulse-width of the output driver slowly. The typical soft-start duration is 2mS.

Under Voltage and Over Voltage Protection

The voltage at FB pin is monitored and protected against OC (over current), UV (under voltage), and OV (over voltage). The UV threshold is 0.5V and OV-threshold is 1.0V. Both UV/OV detection have 30μS triggered delay. When OC or UV trigged, a hiccup re-start sequence will be initialized, as shown in Fig.5. For RT9204, only 3 times of trigger are allowed to latch off. But for RT9204A, UVP will be kept hiccup mode. Hiccup is disabled during soft-start interval.

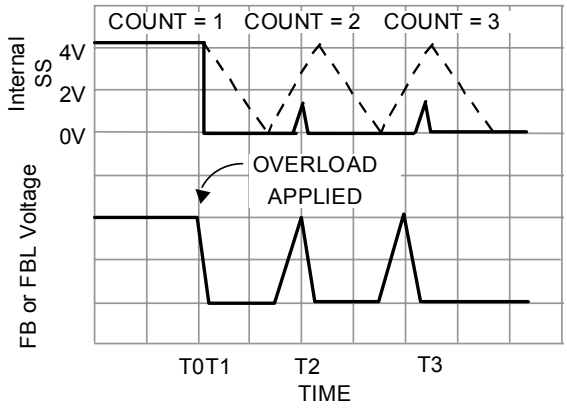


Fig. 5

Applications Information

Inductor Selection

The RT9204/A was designed for V_{IN} = 5V, step-down application mainly. Fig.6 shows the typical topology and waveforms of step-down converter.

The ripple current of inductor can be calculated as follows:

$IL_{RIPPLE} = (5V - V_{OUT})/L \times T_{ON}$

Because operation frequency is fixed at 600kHz,

$T_{ON} = 3.33 \times V_{OUT}/5V$

The V_{OUT} ripple is

$V_{OUT\ RIPPLE} = IL_{RIPPLE} \times ESR$

ESR is COUT capacitor equivalent series resistor

Table 1 shows the ripple voltage of V_{OUT}: VIN = 5V

*Refer to Sanyo low ESR series (CE, DX, PX…)

The suggested L and C are as follows:

2μH with ≥ 1500μF C_{OUT}

5μH with ≥ 1000μF C_{OUT}

Shutdown

Pulling high the SD pin by a small single transistor can shutdown the RT9204/A PWM controller as shown in typical application circuit. Normally SD pin can be floating because an internal 40μA current source will pull low the SD shutdown pin voltage.

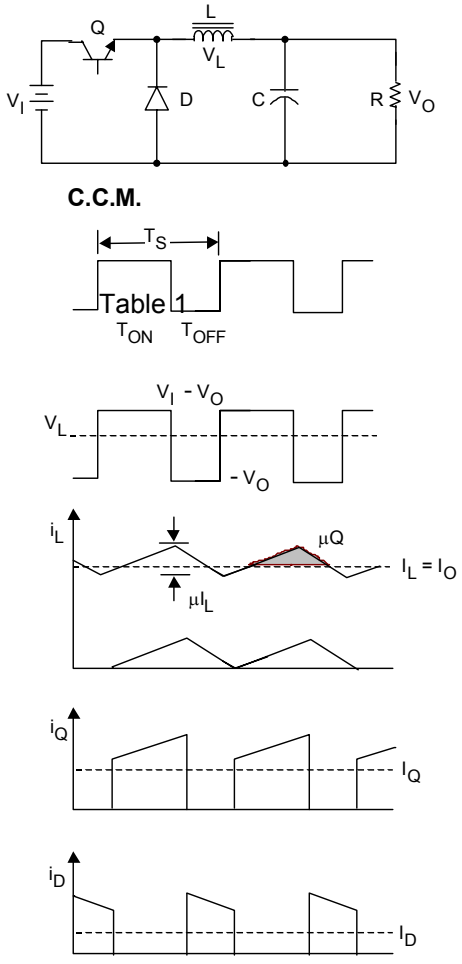


Fig.6

V_{OUT}	3.3V		2.5V		1.5V	
Inductor	2μH	5μH	2μH	5μH	2μH	5μH
1000μF (ESR = 53mΩ)	100mV	40mV	110mV	44mV	93mV	37mV
1500μF (ESR = 33mΩ)	62mV	25mV	68mV	28mV	58mV	23mV
3000μF (ESR = 21mΩ)	40mV	16mV	43mV	18mV	37mV	15mV

Input / Output Capacitor

High frequency/long life decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance to the PCB trace, as it could eliminate the performance from utilizing these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

The output capacitors are necessary for filtering output and stabilizing the close loop (see the PWM loop stability). For powering advanced, high-speed processors, it is required to meet with the requirement of fast load transient, high frequency capacitors with low ESR/ESL capacitors are recommended.

Another concern is high ESR induced ripple may trigger UV or OV protections.

Linear Regulator Driver

The linear regulator of RT9204/A was designed to drive bipolar NPN or MOSFET pass transistor. For MOSFET pass transistor, normally DRV need to provide minimum V_{OUT2}+VT+gate-drive voltage to keep V_{OUT2} as setting voltage. When driving MOSFET operating at 5V power supply system, the gate-drive will be limited at 5V. In this situation shown in Fig. 5, low VT threshold MOSFET (VT = 1V) and Vout2 setting below 2.5V were suggested. In V_{BOOT} = 12V operation condition as Fig. 8, VCC is regulated as higher to 6V providing more gate-drive for pass MOSFET transistor, V_{OUT2} can be set as ≤ 3.3V.

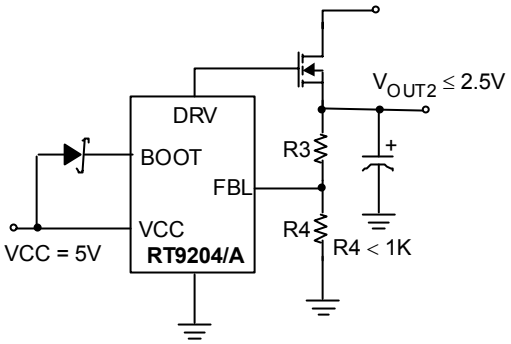


Fig. 7

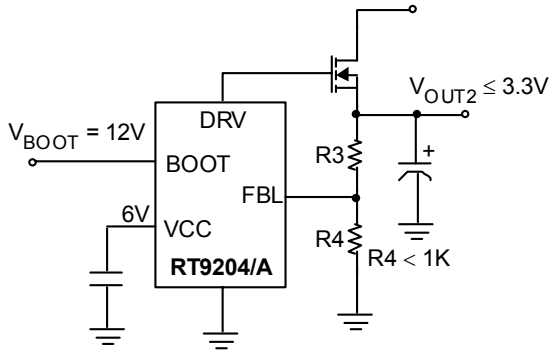


Fig. 8

PWM Loop Stability

The RT9204/A is a voltage mode buck controller designed for 5V step-down applications. The gain of error amplifier is fixed at 35dB for simplified design.

The output amplitude of ramp oscillator is 1.6V, the loop gain and loop pole/zero are calculated as follows:

DC loop gain $G_A = 35dB \times \frac{5}{1.6} \times \frac{0.8}{VOUT}$

LC filter pole $P_O = \frac{1}{2\pi\sqrt{LC}}$

Error Amp pole P_A = 300kHz

ESR zero $Z_O = \frac{1}{2\pi ESR \times C}$

The RT9204/A Bode plot as shown Fig.9 is stable in most of application conditions.

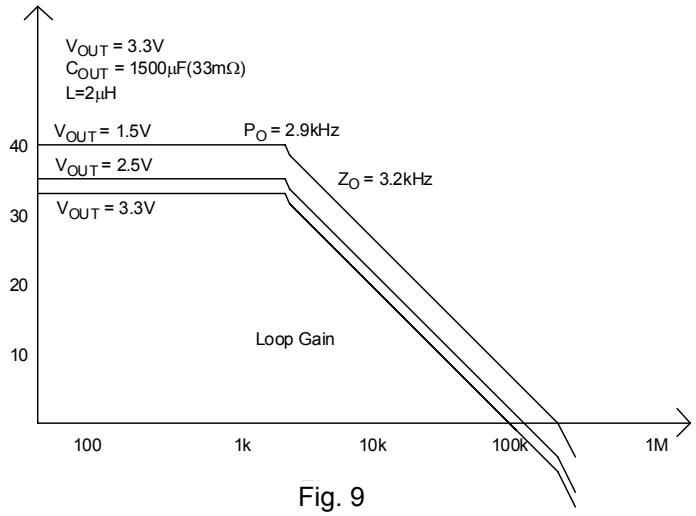


Fig. 9

Reference Voltage

Because RT9204/A use a low 35dB gain error amplifier, shown in Fig. 10. The voltage regulation is dependent on V_{IN} & V_{OUT} setting. The FB reference voltage of 0.8V were trimmed at V_{IN} = 5V & V_{OUT} = 2.5V condition. In a fixed V_{IN} = 5V application, the FB reference voltage vs. V_{OUT} voltage can be calculated as Fig. 11.

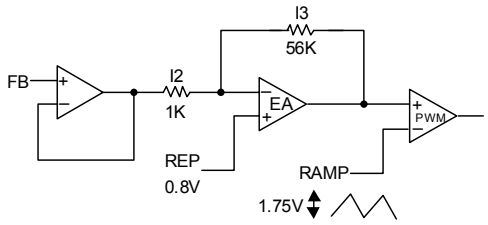


Fig. 10

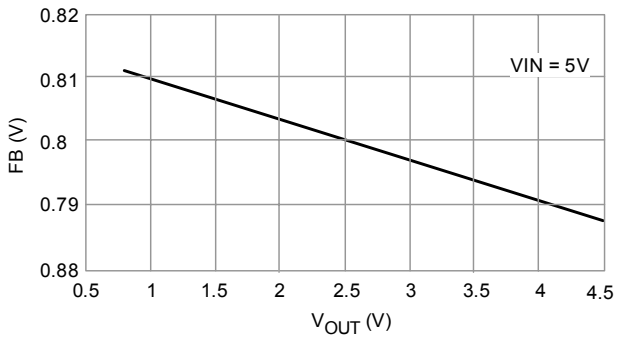


Fig. 11

Feedback Divider

The reference of RT9204/A is 0.8V. Both the PWM and LDO output voltages can be set using a resistor based divider as shown in Fig.12. Put the R1&R2 and R3&R4 as close as possible to FB pin and R2&R4 should be less than 1 kΩ to avoid noise coupling. The C1 capacitor is a speed-up capacitor for reducing output ripple to meet with the requirement of fast transient load. Typically a 1nF ~ 0.1μF is enough for C1.

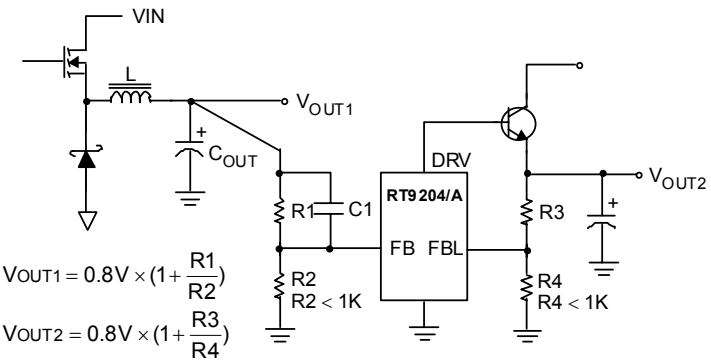


Fig. 12

PWM Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise, that results in ocer-voltage stress on devices. Careful component placement layout and printed circuit design can minimize the voltage spikes induced in the converter. Consider, as an example, the turn-off transition of the upper MOSFET prior to turn-off, the upper MOSFET was carrying the full load current. During turn-off, current stops flowing in the upper MOSFET and is picked up by the low side MOSFET or Schottky diode. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selections, layout of the critical components, and use shorter and wider PCB traces help in minimizing the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using the RT9204/A. The switching power components are most critical because they switch large amounts of energy, and as such, they tend to generate equally large amounts of noise. The critical small signal components are those connected to sensitive nodes or those supplying critical bypass current.

The power components and the PWM controller should be placed firstly. Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, close to the power switches. Place the output inductor and output capacitors between the MOSFETs and the load. Also locate the PWM controller near by MOSFETs.

A multi-layer printed circuit board is recommended. Fig.13 shows the connections of the critical components in the converter. Note that the capacitors CIN and COUT each of them represents numerous physical capacitors. Use a dedicated grounding plane and use vias to ground all critical components to this layer. Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the PHASE node, but it is not necessary to oversize this particular island. Since the PHASE node is subjected to very high dV/dt voltages, the stray capacitance formed between these island and the surrounding circuitry will tend to couple switching noise. Use the remaining printed circuit layers for small signal routing. The PCB traces between the PWM controller and the gate of MOSFET and also the traces connecting source of MOSFETs should be sized to carry 2A peak currents.

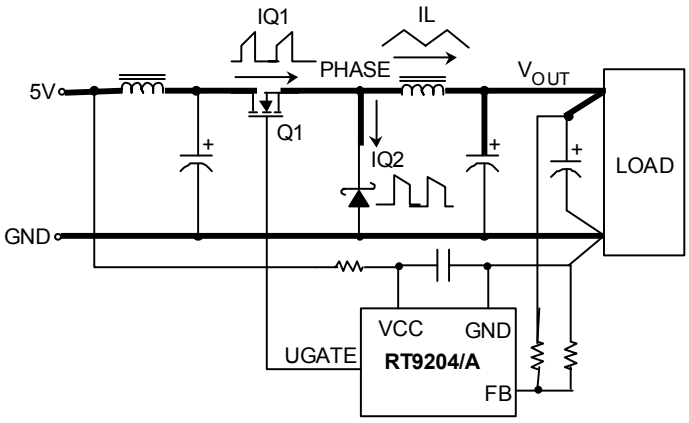
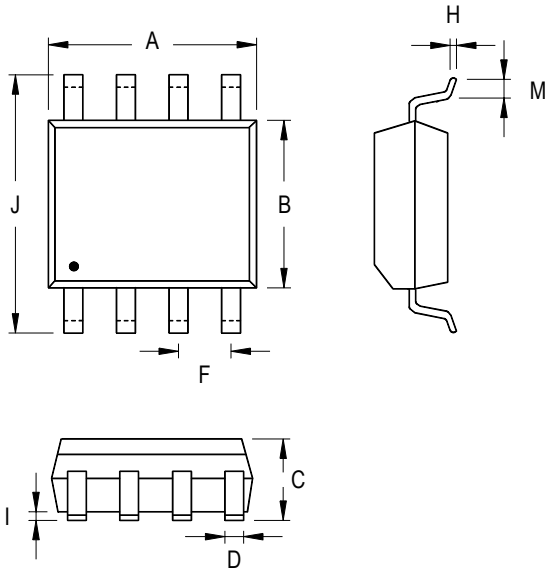


Fig. 13

Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

8–Lead SOP Plastic Package

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