RF2401

LOW NOISE AMPLIFIER/MIXER

Typical Applications

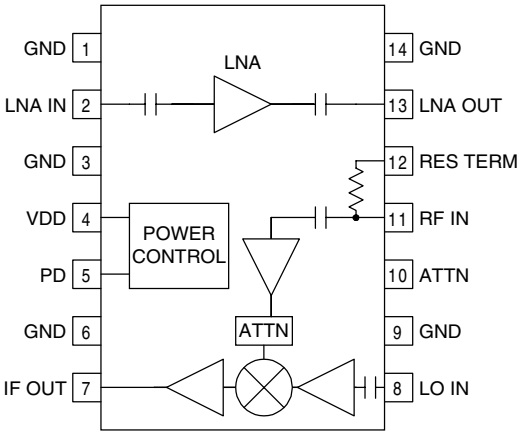
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery Powered Equipment
- General Purpose Frequency Conversion

Product Description

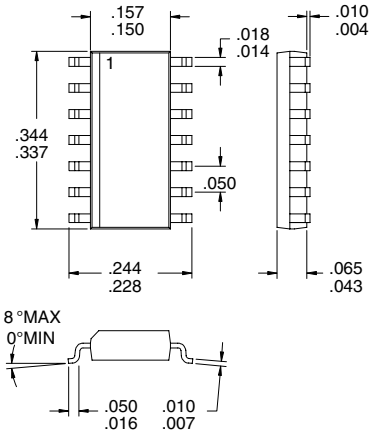
The RF2401 is a monolithic integrated UHF receiver front-end. The IC contains all of the required components to implement the front-end functions of the receiver except for the passive filtering and LO generation. It contains a high dynamic range LNA (low-noise amplifier), an attenuator to reduce signal level in the presence of large received signals, a second RF amplifier, a double balanced mixer, an LO buffer amplifier, and an IF output amplifier which will drive a 50Ω load. The output of the LNA is made available as an output to permit the insertion of a bandpass filter between the LNA and the attenuator. The mixer input is buffered to provide high isolation from the LO to the input port. Blocking capacitors are contained on the chip (except for the IF Output).

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☑ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Power Down Capability
- High Dynamic Range
- Low Current Drain
- High LO Isolation
- RF Attenuator for Large Signals
- 300MHz to 1100MHz Operation

Ordering Information

RF2401	Low Noise Amplifier/Mixer
RF2401 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

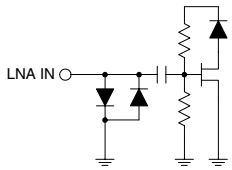
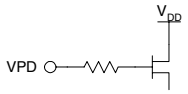
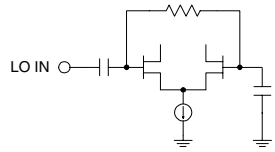
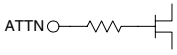
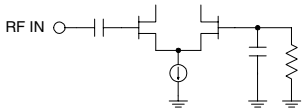
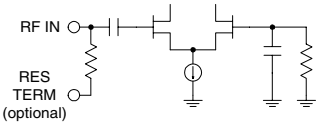
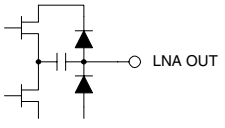
8 FRONT-ENDS

Absolute Maximum Ratings

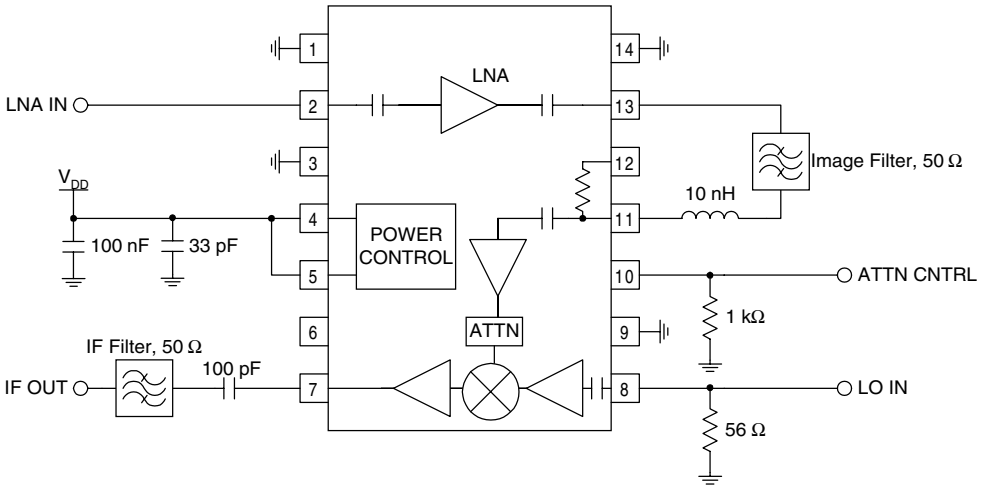
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
Ambient Operating Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{DD}=5V, RF=915MHz, LO=986MHz
Frequency Range		300 to 1100		MHz	
Cascade Gain	22	24		dB	RF=850MHz
Cascade IP3		-17		dBm	Referenced to input
Cascade Noise Figure		4.3		dB	Single sideband
LO to LNA Input Rejection		65		dB	
First Section (LNA)					
Noise Figure		2.9		dB	
Input VSWR		1.5:1			
Input IP3		-10		dBm	
Gain		11		dB	
Reverse Isolation		30		dB	
Output VSWR		1.3:1			
Second Section (RF Amp, Mixer, IF)					
Noise Figure		10		dB	Single sideband
Input VSWR		1.5:1			In order to achieve a low VSWR match at this input, a 10nH chip inductor is placed in series with this port. If direct coupling is used (no noise image filter between LNA OUT and RF IN ports), no inductor is necessary.
Input IP3		-7		dBm	
Conversion Gain		12		dB	ATTN=GND
Conversion Gain Change	-25	-21	-17	dB	ATTN=V_{DD}, RF=850MHz
Output Impedance		50		Ω	
LO Input					
LO Frequency		250 to 1150		MHz	
LO Level		-6 to +3		dBm	
LO to RF Rejection		25		dB	
LO to IF Rejection		30		dB	
LO Input VSWR		1.3:1			With external 75Ω termination
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage; Part is "ON"
Power Down "OFF"		0		V	Threshold voltage; Part is "OFF"
Power Supply					
Voltage		4.5 to 6.5		V	
Current Consumption		20	30	mA	On
Current Consumption		0.2	0.5	mA	Power Down

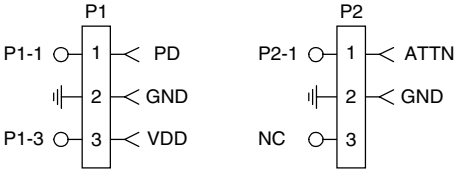
Pin	Function	Description	Interface Schematic
1	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
2	LNA IN	This pin has input protection diodes to protect the LNA from ESD and high RF levels. Because the diodes are present, an external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin.	
3	GND	Same as pin 1.	
4	VDD	Supply Voltage for the LNA, Mixer, and all three buffer amplifiers. An external RF bypass capacitor is required and an optional 0.01µF bypass capacitor will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
5	PD	Power Down control pin. With 0V connected to this pin, the part draws minimum current (<0.5mA). When connected to V_{DD}, the part is fully operational. For applications where VPD is not controlled, this pin is simply connected to V_{DD}.	
6	GND	Same as pin 1.	
7	IF OUT	50Ω buffered IF output port. This pin is NOT DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present, or a device that presents a finite DC impedance.	
8	LO IN	Mixer LO input. If approximately 0dBm of LO power is available, a shunt 56Ω resistor can be used for matching. If the available LO power is near -6dBm, then a reactive match may be required. A high pass matching network, such as a single shunt inductor is the recommended topology because it also rejects IF noise at the mixer input. This pin is internally DC blocked.	
9	GND	Same as pin 1.	
10	ATTN	Attenuation control for mixer RF input. When tied to V_{DD}, the mixer's conversion gain is reduced by approximately 20dB at 915MHz. When tied to ground, the mixer's conversion gain is at maximum (approximately 12dB at 915MHz).	
11	RF IN	Mixer RF Input port. For a 50Ω match at 900MHz use a 10nH series inductor. The mixer inputs are internally DC blocked. When pin 12 is tied to ground, an internal matching resistor is connected in parallel at the expense of increasing the mixer's noise figure and reducing its gain. There is an internal blocking capacitor between this pin and the mixer's input, but not between the pin and the internal matching resistor (see the functional block diagram).	
12	RES TERM	Connecting this pin to ground causes an internal matching resistor to be connected in parallel with the mixer's input. This eliminates the need for a matching inductor and matches the mixer input over a broad band, but the mixer's noise figure and gain will be degraded. When matching pin 11 with an inductor, pin 12 should be left unconnected.	
13	LNA OUT	This pin has protection diodes to protect the LNA from ESD and high RF levels. Because the diodes are present, an external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If pin 13 is connected directly to pin 11, then no blocking capacitor is required.	
14	GND	Same as pin 1.	

Application Schematic

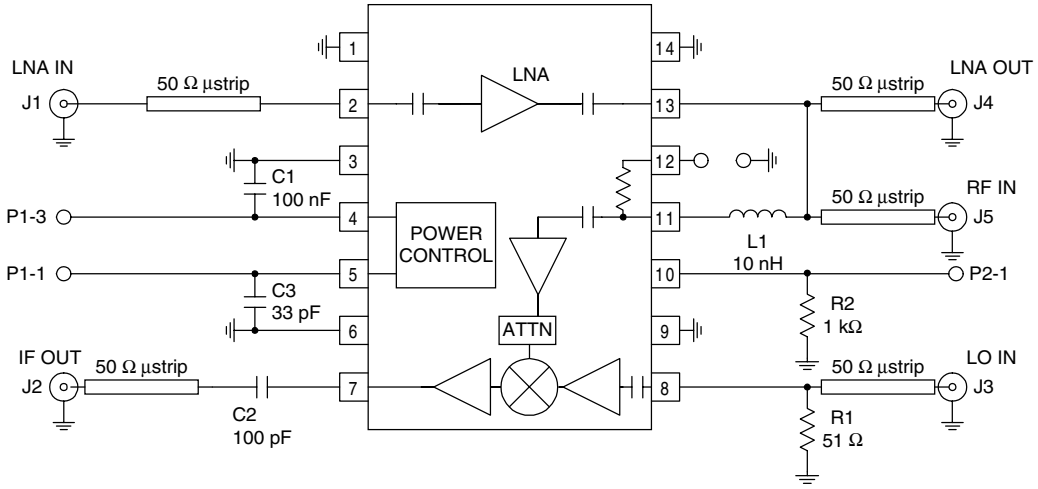


Evaluation Board Schematic

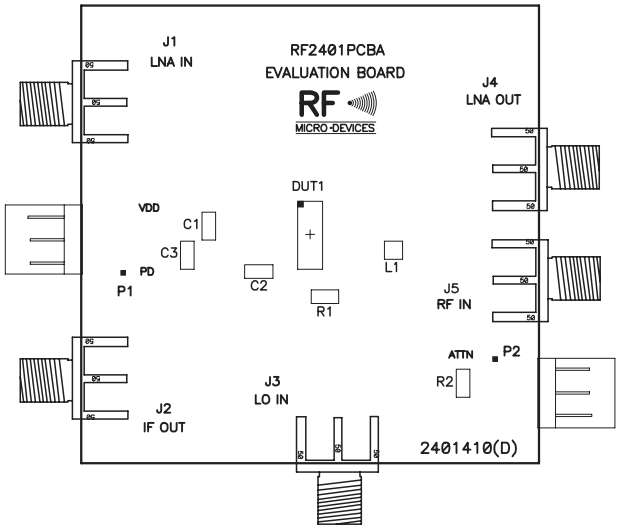
(Download Bill of Materials from www.rfmd.com.)

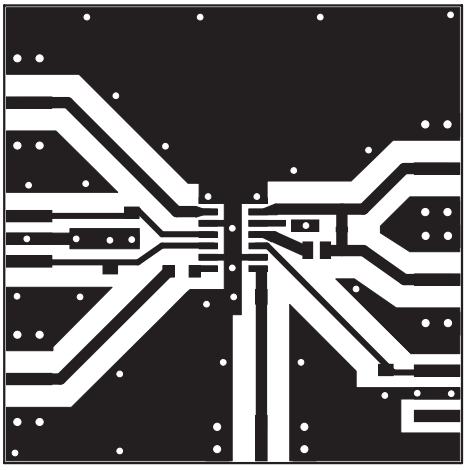


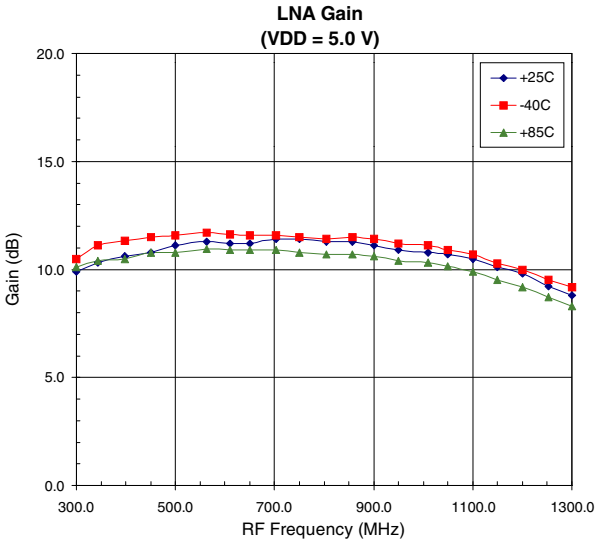
2401400 Rev E

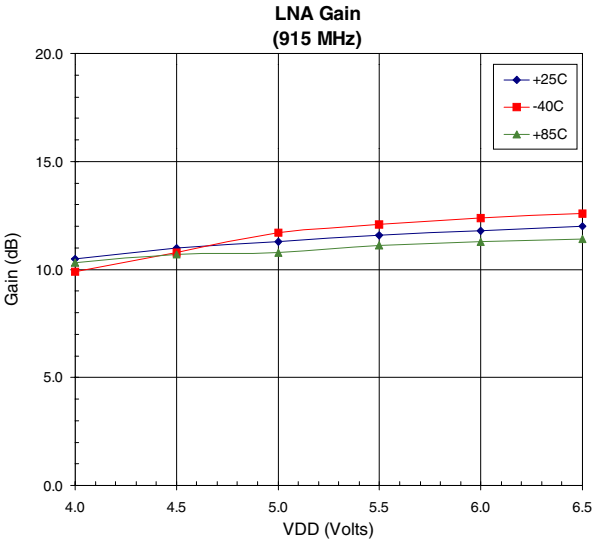


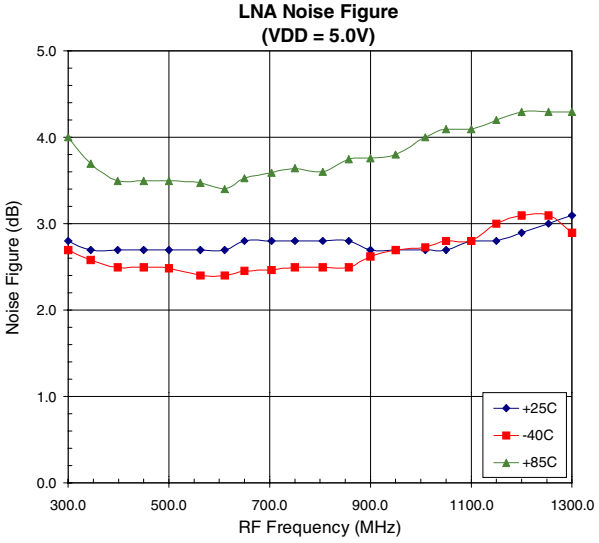
Evaluation Board Layout
Board Size 2.020” x 2.020”

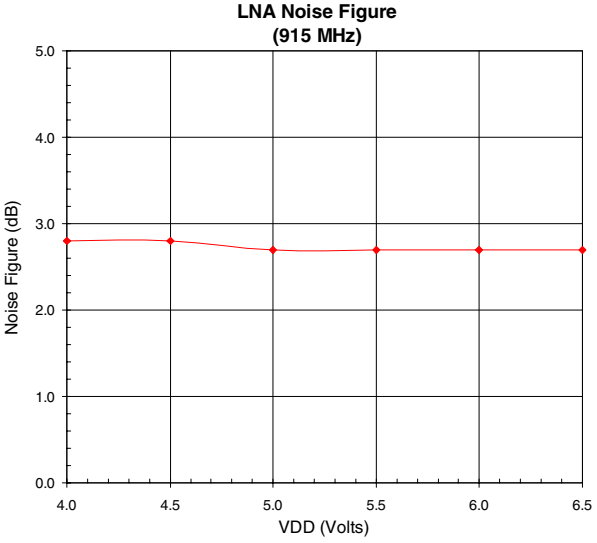


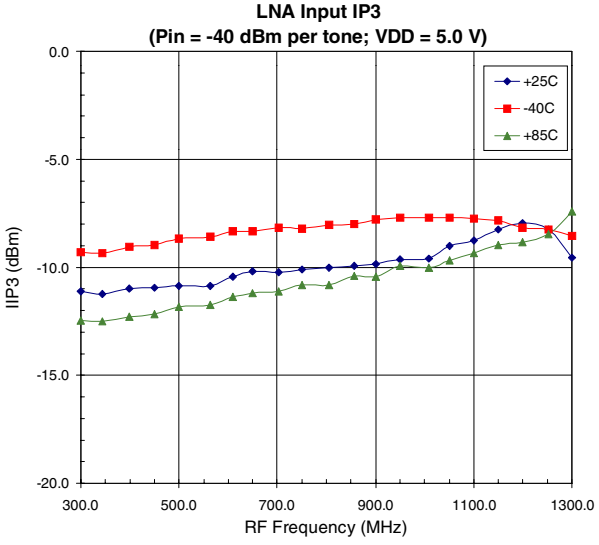


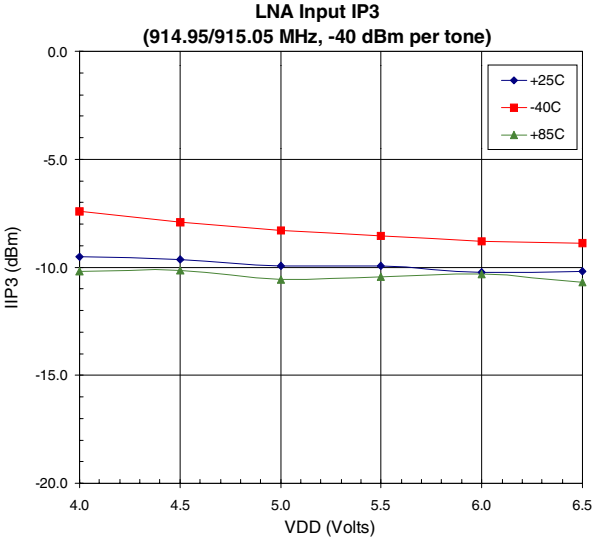

LNA Gain
(VDD = 5.0 V)
Gain (dB)
RF Frequency (MHz)
+25C
-40C
+85C


LNA Gain
(915 MHz)
Gain (dB)
VDD (Volts)
+25C
-40C
+85C

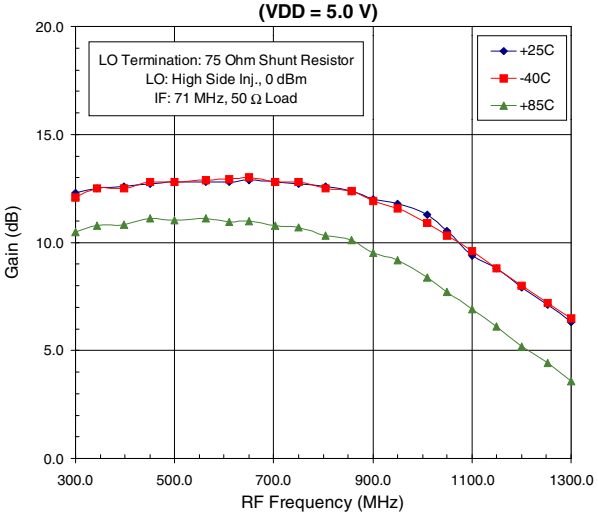

LNA Noise Figure
(VDD = 5.0V)
Noise Figure (dB)
RF Frequency (MHz)
+25C
-40C
+85C


LNA Noise Figure
(915 MHz)
Noise Figure (dB)
VDD (Volts)

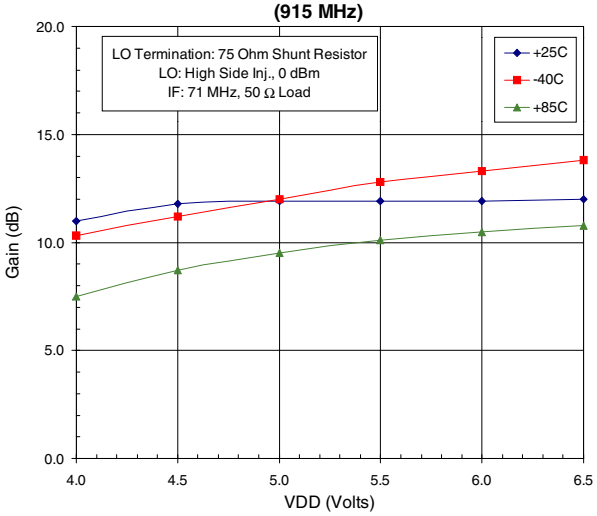

LNA Input IP3
(Pin = -40 dBm per tone; VDD = 5.0 V)
IIP3 (dBm)
RF Frequency (MHz)
+25C
-40C
+85C


LNA Input IP3
(914.95/915.05 MHz, -40 dBm per tone)
IIP3 (dBm)
VDD (Volts)
+25C
-40C
+85C

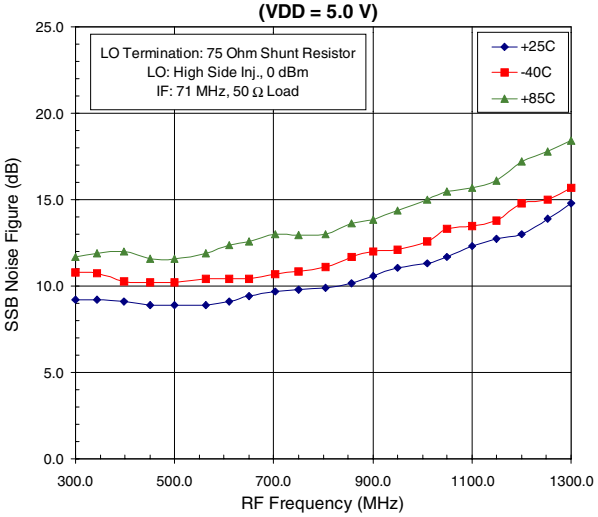
Mixer Power Gain
(VDD = 5.0 V)



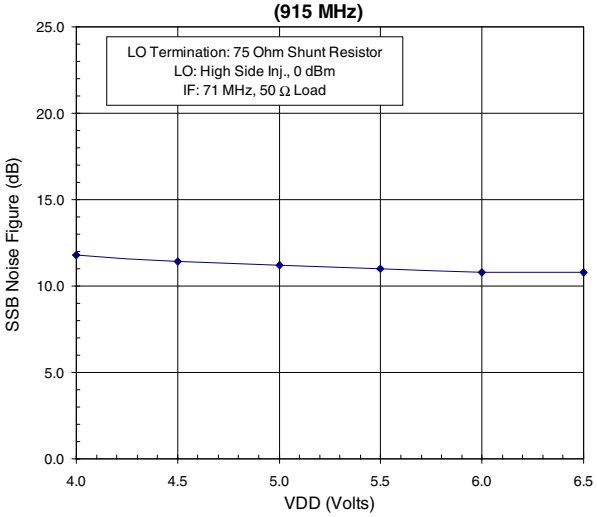
Mixer Power Gain
(915 MHz)



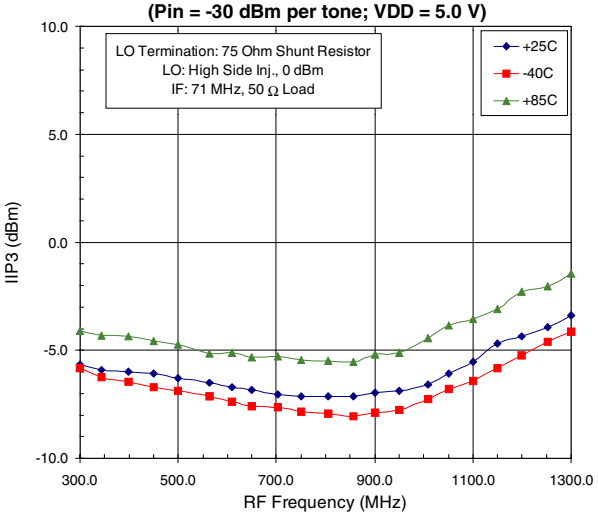
Mixer SSB Noise Figure
(VDD = 5.0 V)



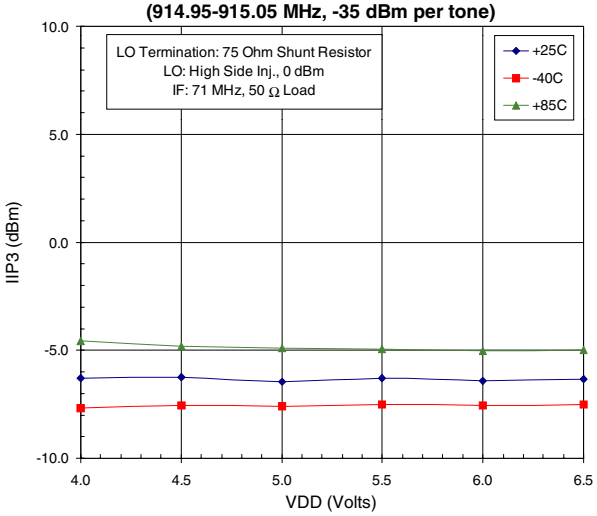
Mixer SSB Noise Figure
(915 MHz)



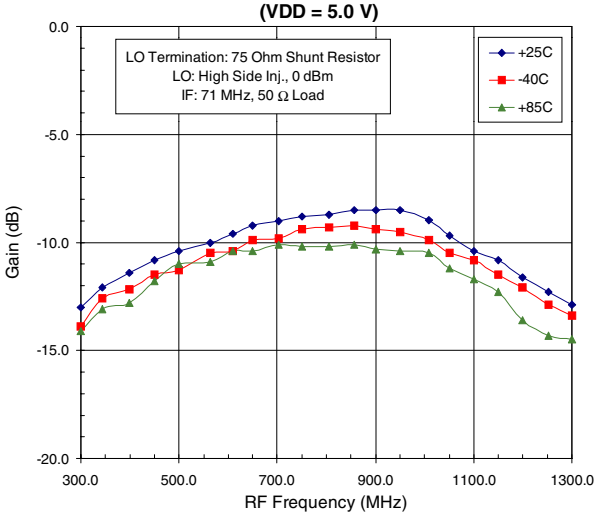
Mixer Input IP3
(Pin = -30 dBm per tone; VDD = 5.0 V)



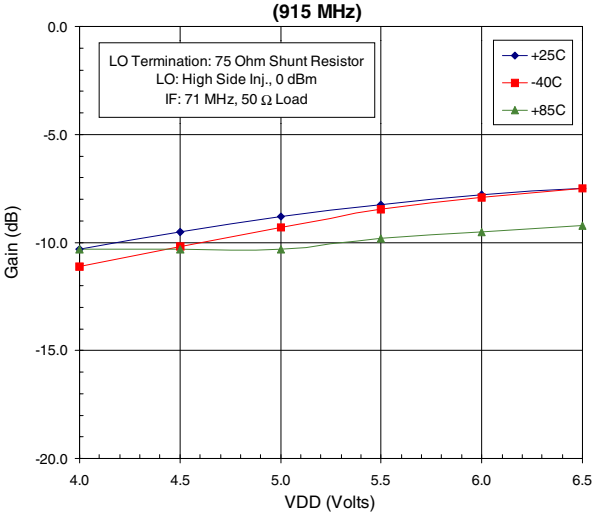
Mixer Input IP3
(914.95-915.05 MHz, -35 dBm per tone)



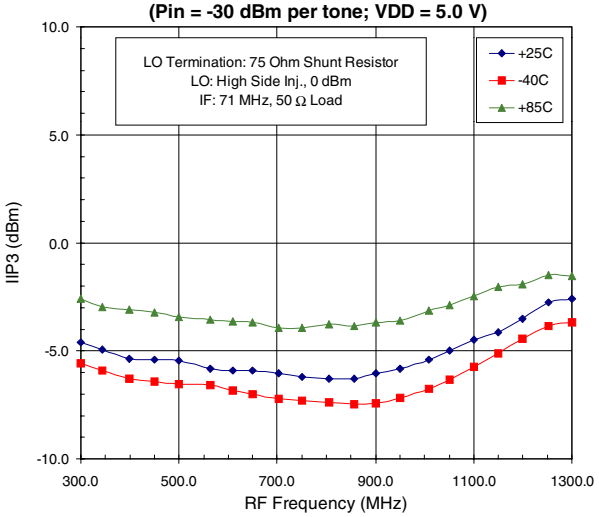
Mixer Power Gain, Attenuator On
(VDD = 5.0 V)



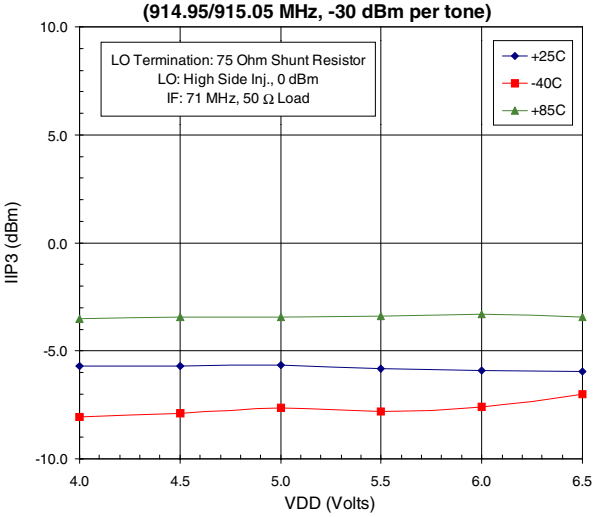
Mixer Power Gain, Attenuator On
(915 MHz)



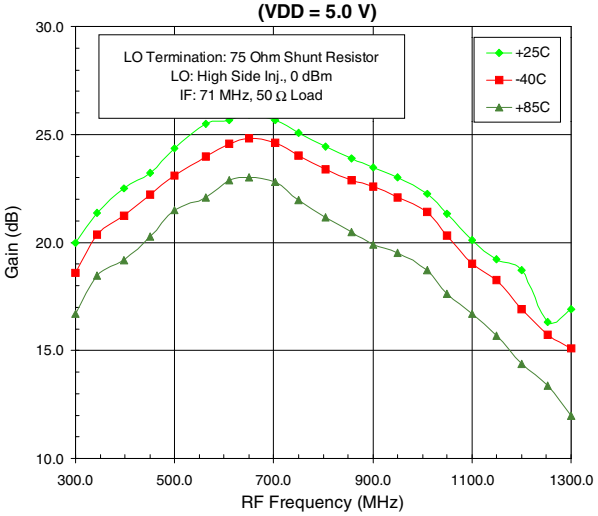
Mixer Input IP3, Attenuator On
(Pin = -30 dBm per tone; VDD = 5.0 V)



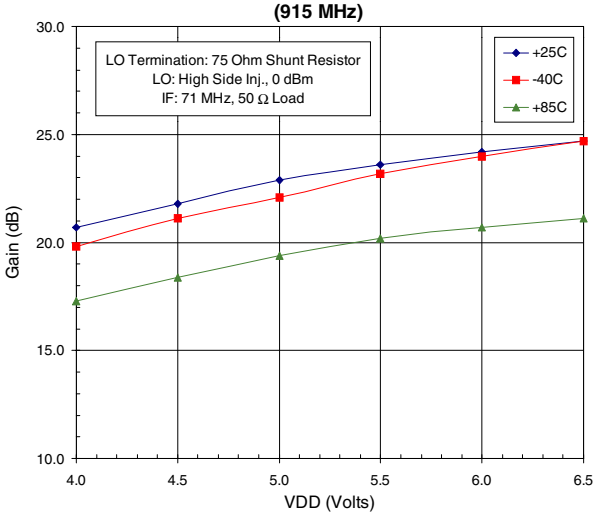
Mixer Input IP3, Attenuator On
(914.95/915.05 MHz, -30 dBm per tone)



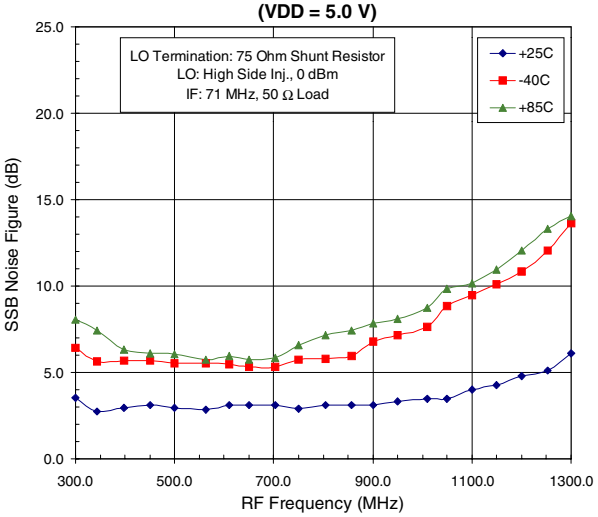
LNA + Mixer Power Gain
(VDD = 5.0 V)



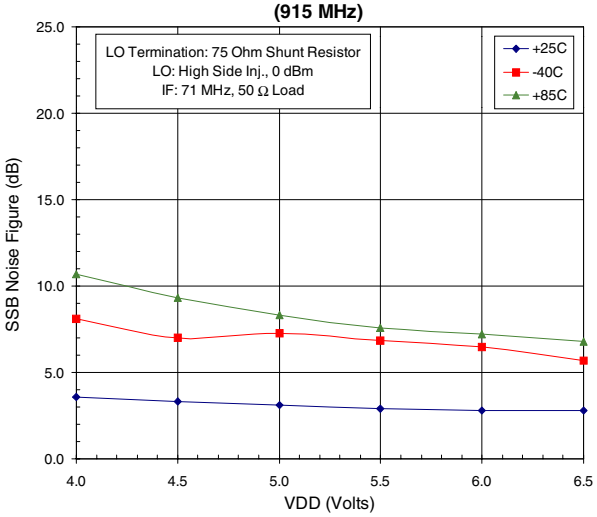
LNA + Mixer Power Gain
(915 MHz)



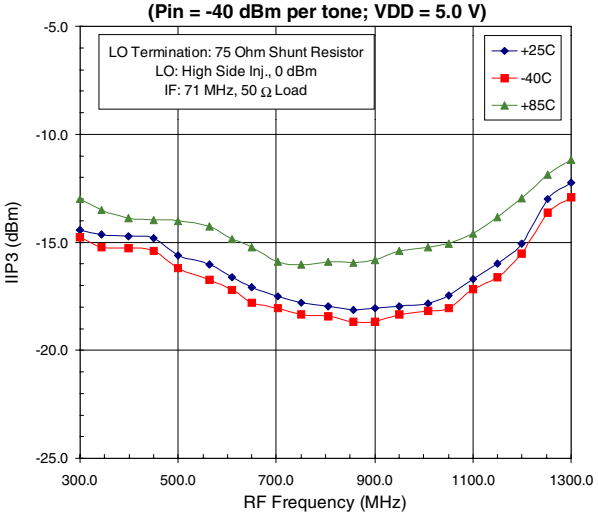
LNA + Mixer SSB Noise Figure
(VDD = 5.0 V)



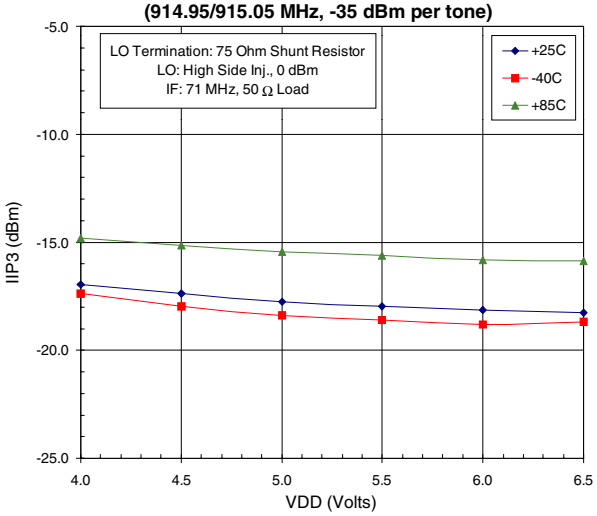
LNA + Mixer SSB Noise Figure
(915 MHz)



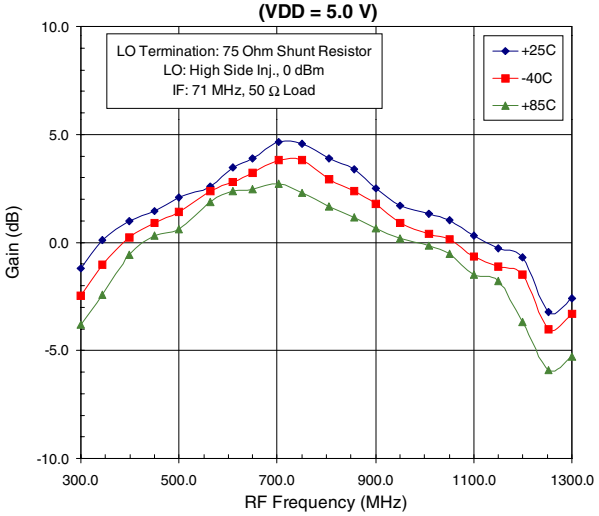
LNA + Mixer Input IP3
(Pin = -40 dBm per tone; VDD = 5.0 V)



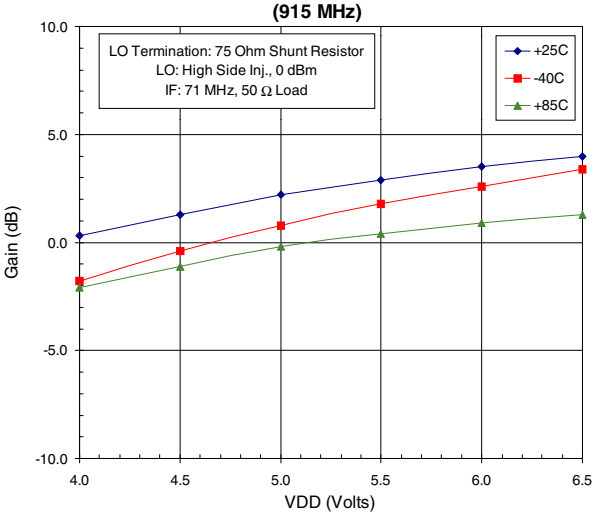
LNA + Mixer Input IP3
(914.95/915.05 MHz, -35 dBm per tone)



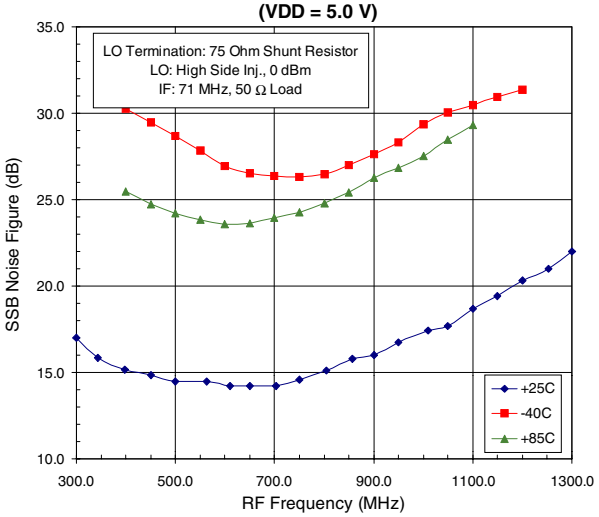
LNA + Mixer Power Gain, Attenuator On (VDD = 5.0 V)



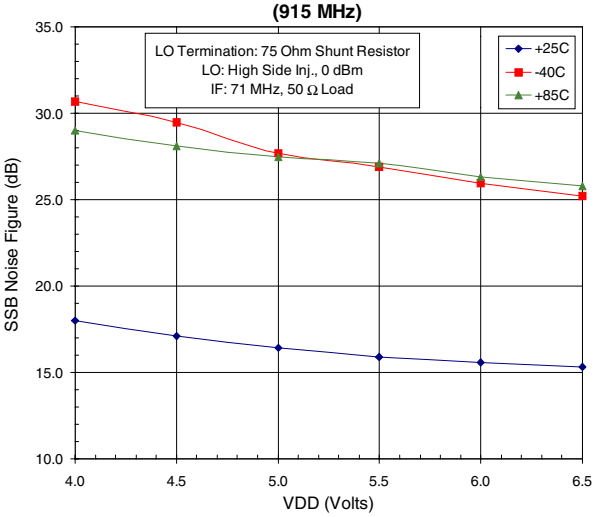
LNA + Mixer Power Gain, Attenuator On (915 MHz)



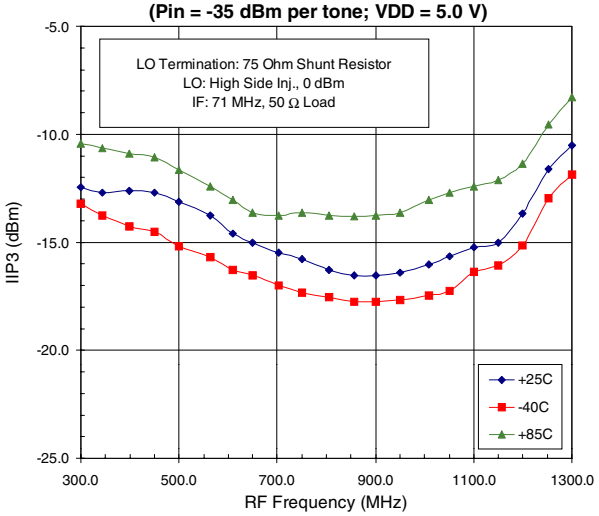
LNA + Mixer SSB Noise Figure, Attenuator On (VDD = 5.0 V)



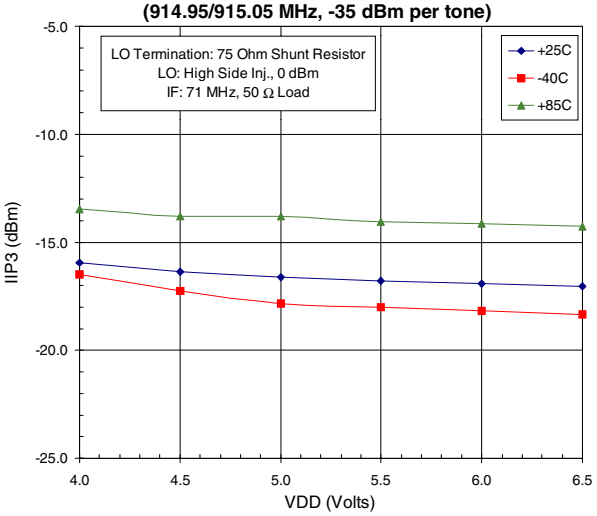
LNA + Mixer SSB Noise Figure, Attenuator On (915 MHz)



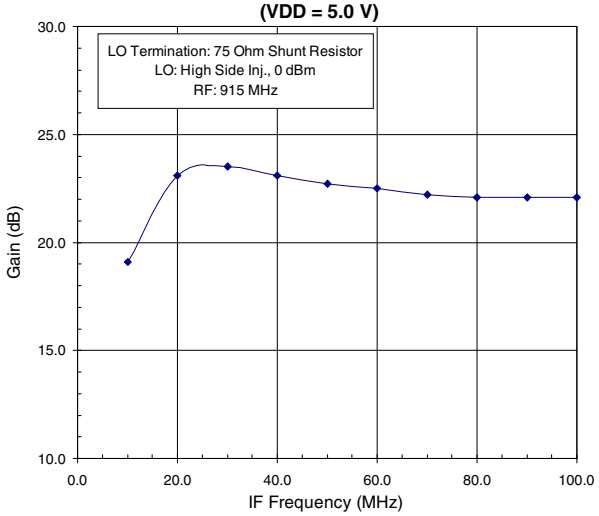
LNA + Mixer Input IP3, Attenuator On (Pin = -35 dBm per tone; VDD = 5.0 V)



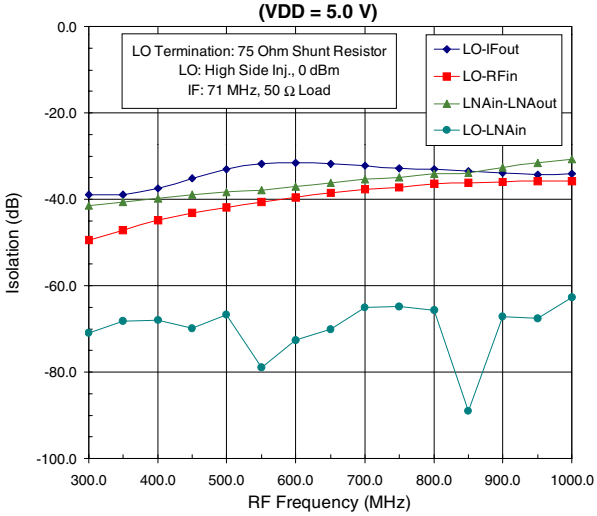
LNA + Mixer Input IP3, Attenuator On (914.95/915.05 MHz, -35 dBm per tone)



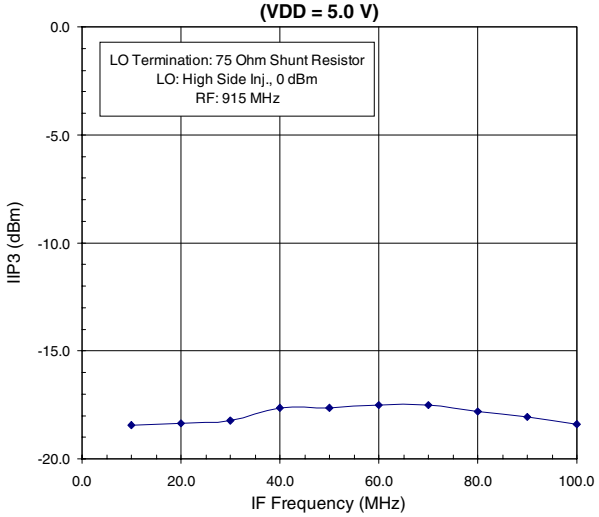
LNA + Mixer Power Gain versus IF Frequency (VDD = 5.0 V)



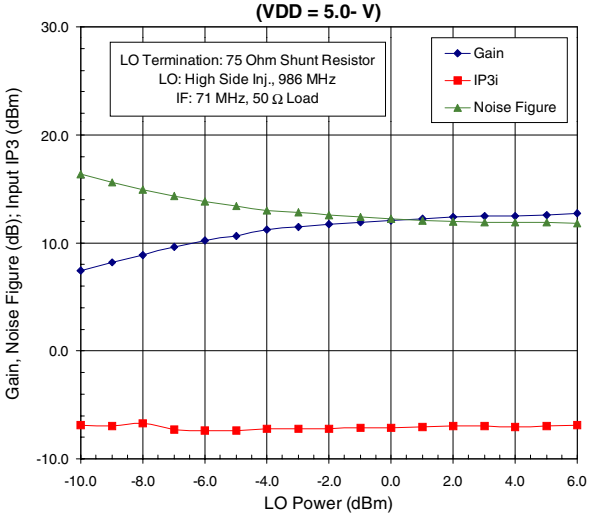
Isolation (VDD = 5.0 V)



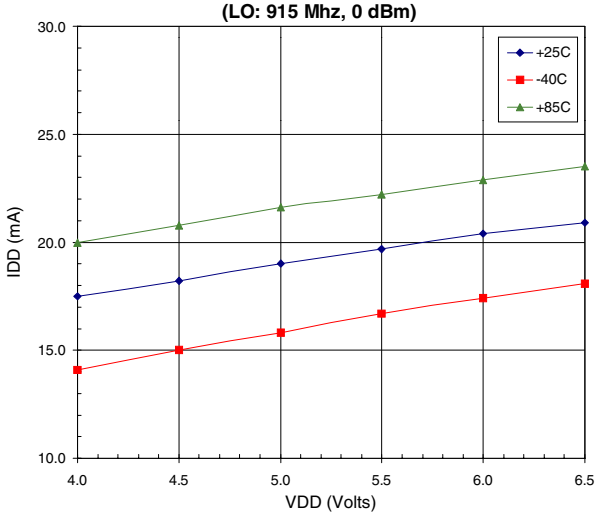
LNA + Mixer Input IP3 versus IF Frequency (VDD = 5.0 V)



Mixer Performance versus LO Power (VDD = 5.0- V)



IDD versus VDD (LO: 915 Mhz, 0 dBm)



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FRONT-ENDS