

RipTide™ RAMC001 and RAMC002 AMC '97 Audio Modem Codec (AMC)

1. Overview

The Rockwell RipTide™ Audio Modem Codec (AMC) combines two coder/decoder functions, compliant to Intel Audio Codec '97 2.0 Extensions for a combo audio modem codec (AMC'97), into a single package. The AMC is available in either an 80-pin PQFP, which supports two telephone lines (RAMC002), or a 64-pin TQFP, which supports one telephone line (RAMC001). The AMC is supplied with Rockwell WaveStream™ 64 (WS64) or Mega WaveStream software and optionally with Rockwell MMX-based SoftK56 V.90/K56flex™ modem software (see Table 1).

The AMC can be ordered by itself or as part of the Rockwell RipTide PCI Audio/Comm Device Family which also includes an Communications Controller (ACC) and optional Modem DSP and Rockwell RipTide V.90/K56flex™ modem software (see Product Description Order Number 1167).

2. Features

- **Combined Audio/Modem Codec (AMC)**
 - AC '97 Codec V2.0 compliant (AMC '97)
- **Advanced Power Management**
- **Audio**
 - Stereo Full-Duplex Codec with 18-bit resolution
 - Six Audio Analog Input Channels
 - Three Audio Analog Output Channels
 - 3D Spatialization and Bass Boost
- **Modem**
 - Full-Duplex Codec with 16-bit resolution
 - 1-Line (64-pin TQFP) or 2-Line (80-pin PQFP) Telephone Line Interface
 - Dedicated Handset ADC/DAC
 - Dedicated Microphone ADC
- **GPIO Lines**
- **Standard 64-pin TQFP and 80-pin PQFP**

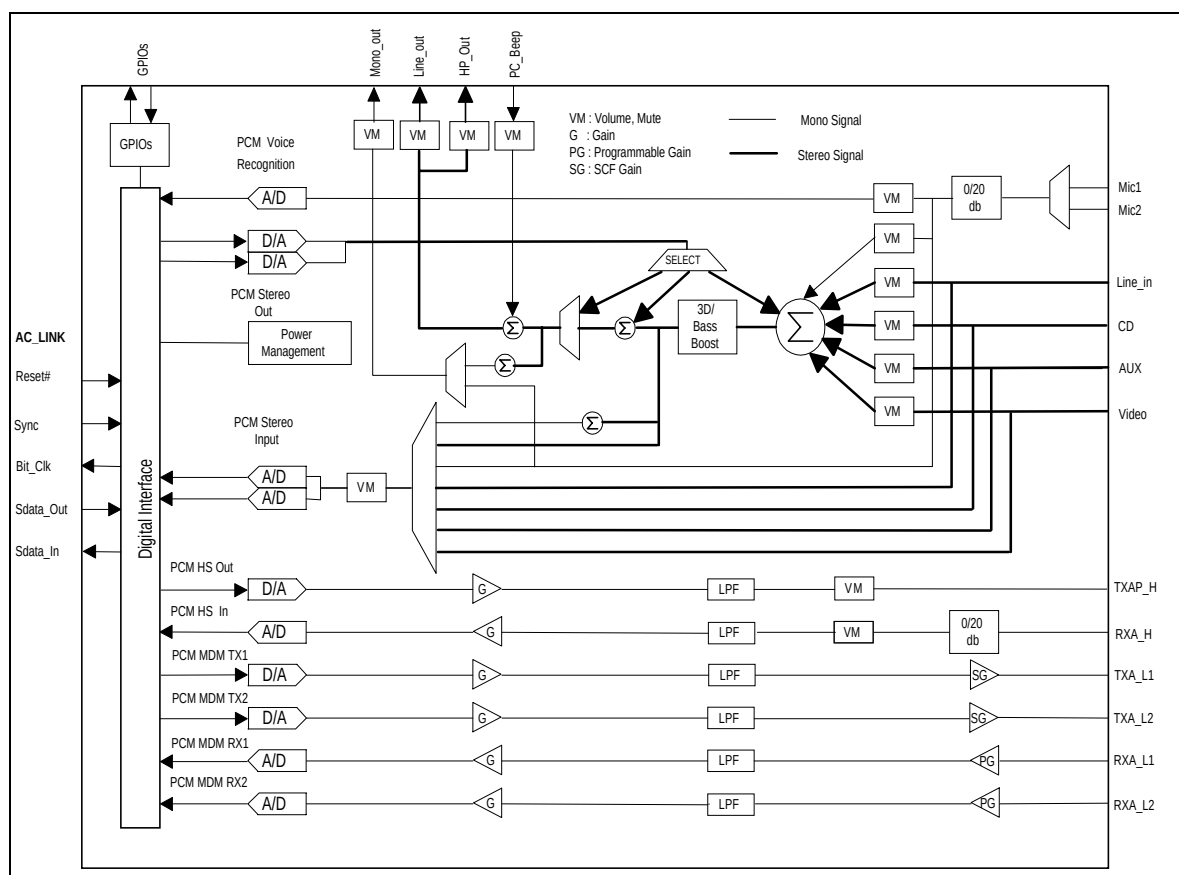


Figure 1. RipTide AMC Functional Block Diagram

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

2.1 Detailed Features

- Six Audio Analog Input Channels
 - Four Stereo Line-Level Inputs: Line_In, CD, Video, and AUX
 - Mono Mic Level Input Switchable from Two External Sources: Mic_1 and Mic_2
 - Mono PC Beep input
- Three Audio Analog Output Channels
 - Two Stereo Line-Level Outputs: Line_Out and Headphone_Out
 - Mono Output: Mono_Out

2.2 Ordering Information

Table 1. AMC Models and Options

Ordering Information		Package and Supported Functions				
Marketing Model No.	Order Number	AMC Package	No. of Telephone Lines	SoftK56 Modem Software	WaveStream 64 Software	Mega WaveStream Software
RAMC001	DSRT-L000-021	64-Pin TQFP	1	Y	Y	--
RAMC001	DSRT-L000-031	64-Pin TQFP	1	Y	--	Y
RAMC002	DSRT-L000-041	80-Pin PQFP	2	Y*	Y	--
RAMC002	DSRT-L000-051	80-Pin PQFP	2	Y*	--	Y
* 2-line SoftK56 modem software required (see Product Description Order No. 1166 for 2-line support by Modem DSP and SoftK56 modem software).						

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3. System Description

3.1 RipTide System Solution

A block diagram of the Rockwell RipTide Integrated PCI Audio/Communications System is shown in Figure 2. The three Rockwell devices in the system are the Audio and Modem Digital Controller (AMDC), Audio and Modem Codec (AMC) and optional Modem DSP (MDSP). The integrated RipTide system is described in Product Description Order Number 1167.

3.2 Audio and Modem Codec (AMC)

The AMC in 80-pin PQFP (RAMC002) supports two telephone lines and the AMC in 64-pin TQFP supports one telephone line (RAMC001). The AMC communicates to the RipTide AMDC or other AC '97-compatible controller through a digital serial link (AC-link). All digital data audio stream, modem data (telephone stream, handset, and microphone), GPIO data, and codec command/status information is transferred between the controller and the codec over this point-to-point serial channel.

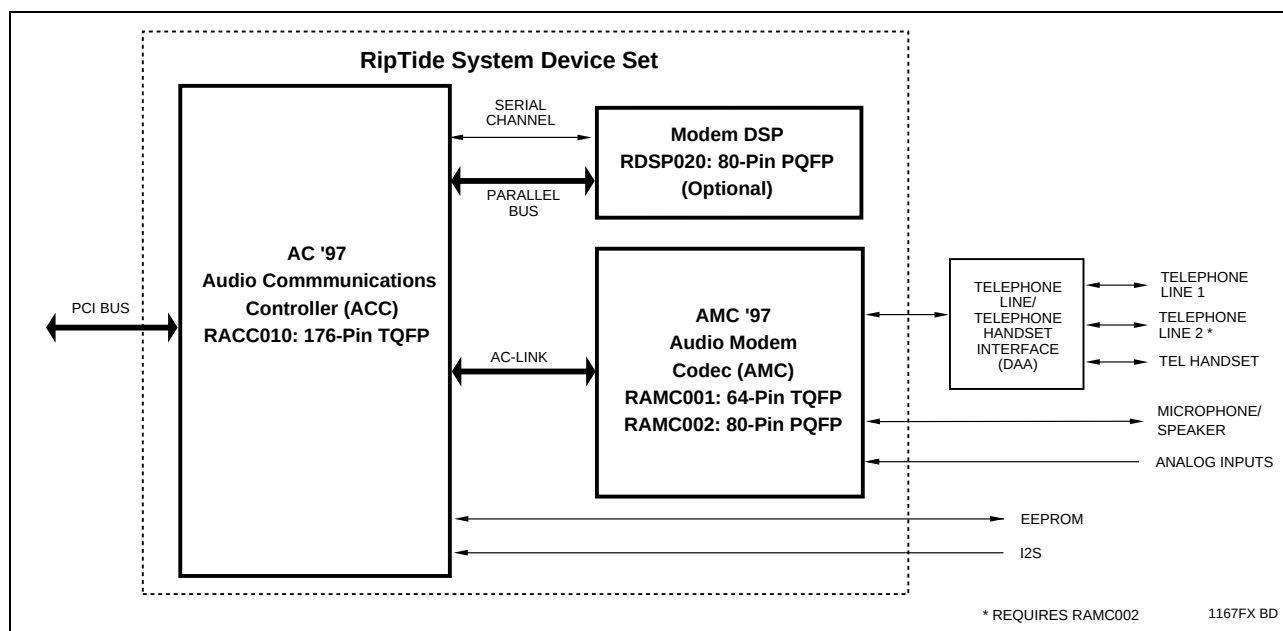


Figure 2. RipTide System Block Diagram

3.3 Reference Information

RipTide PCI Audio/Comm Device Family Product Description (Order No. 1167).

4. Hardware Interface Signals

4.1 AMC 64-Pin TQFP Pin Assignments

The pin assignments for the AMC in 64-pin TQFP are shown in Figure 3 and are listed in Table 2.

This package has enough GPIOs to support one phone line.

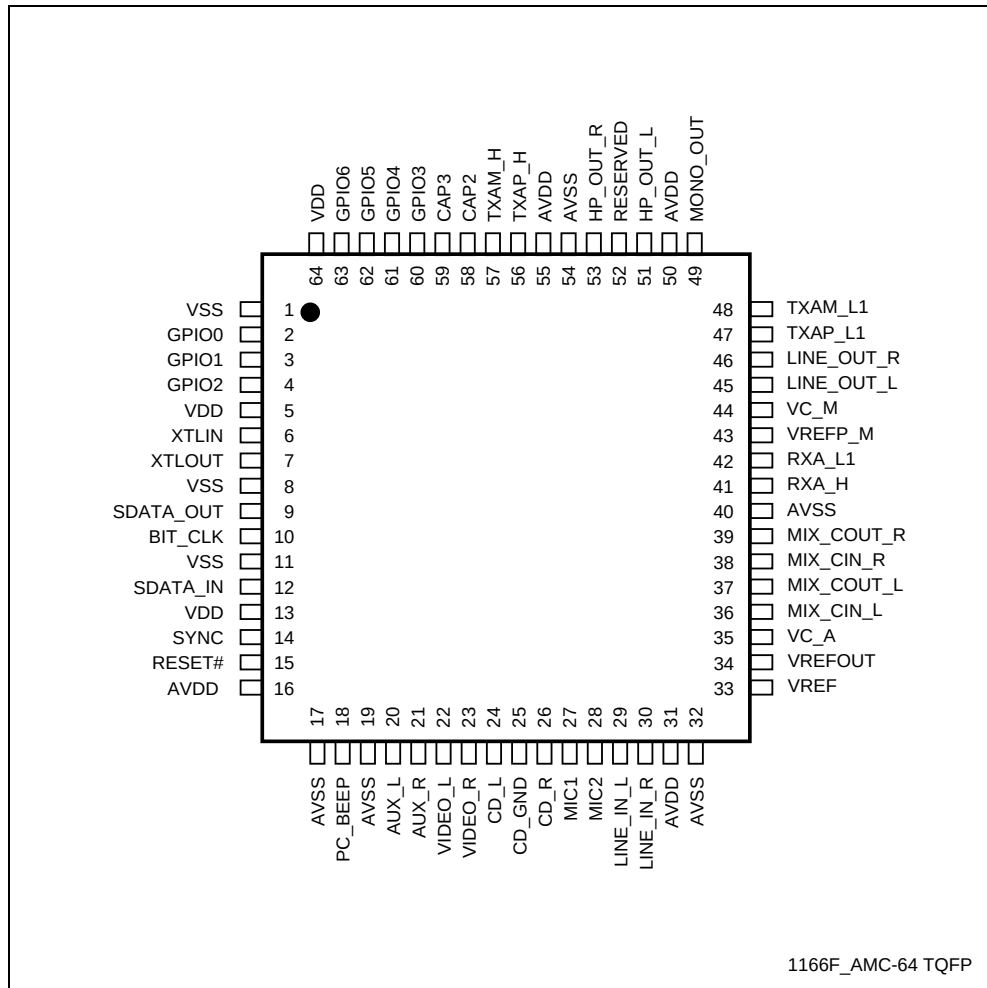


Figure 3. AMC Pin Assignments - 64-Pin TQFP

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Table 2. AMC Pin Assignments - 64-Pin TQFP

Pin	Signal Label	I/O Type ¹	Interface ²	Pin	Signal Label	I/O Type	Interface
1	VSS	GND	GND	33	VREF	REF	AGND through 10 uF and 0.1 uF
2	GPIO0	It/Ot4	Application assigned	34	VREFOUT	REF	AGND through 10 uF and 0.1 uF
3	GPIO1	It/Ot4	Application assigned	35	VC_A	REF	AGND through 10 uF and 0.1 uF
4	GPIO2	It/Ot4	Application assigned	36	MIX_CIN_L	Ia	AI: MIX_COUTL through 1 uF
5	VDD	PWR	+5V or +3.3V	37	MIX_COUT_L	Oa	AI: MIX_CIN_L through 1 uF
6	XTLIN	Ix	24.576 MHz Crystal/Clock In	38	MIX_CIN_R	Ia	AI: MIX_COUT_R through 1 uF
7	XTLOUT	Ox	24.576 MHz Crystal Out	39	MIX_COUT_R	Oa	AI: MIX_CIN_R through 1 uF
8	VSS	GND	GND	40	AVSS	AGND	AGND
9	SDATA_OUT	I	AMDC: SDATA_OUT	41	RXA_H	Ia	LTI: Handset Receive Analog
10	BIT_CLK	O	AMDC: BIT_CLK	42	RXA_L1	Ia	LTI: Line 1 Receive Analog
11	VSS	GND	GND	43	VREFP_M	REF	AGND through 10 uF and 0.1 uF
12	SDATA_IN	O	AMDC: SDATA_IN	44	VC_M	REF	AGND through 10 uF and 0.1 uF
13	VDD	PWR	+5V or +3.3V	45	LINE_OUT_L	Oa	AI: Line Out Left Channel
14	SYNC	I	AMDC: SYNC	46	LINE_OUT_R	Oa	AI: Line Out Right Channel
15	RESET#	It	AMDC: RESET#	47	TXAP_L1	Oa	LTI: Line 1 Transmit Analog Plus
16	AVDD	PWR	+5VA	48	TXAM_L1	Oa	LTI: Line 1 Transmit Analog Minus
17	AVSS	AGND	AGND	49	MONO_OUT	Oa	AI: Speaker
18	PC_BEEP	Ia	AI: PC Speaker beep pass through	50	AVDD	PWR	+5VA
19	AGND	AGND	AGND	51	HP_OUT_L	Oa	AI: Headphone Out Left Channel
20	AUX_L	Ia	AI: Aux Audio Left Channel	52	RESERVED	Ot4	NC
21	AUX_R	Ia	AI: Aux Audio Right Channel	53	HP_OUT_R	Oa	AI: Headphone Out Right Channel
22	VIDEO_L	Ia	AI: Video Audio Left Channel	54	AVSS	AGND	AGND
23	VIDEO_R	Ia	AI: Video Audio Right Channel	55	AVDD	PWR	+5VA
24	CD_L	Ia	AI: CD Audio Left Channel	56	TXAP_H	Oa	LTI: Handset Transmit Analog Plus
25	CD_GND	GND	AI: CD Audio analog ground	57	TXAM_H	Oa	LTI: Handset Transmit Analog Minus
26	CD_R	Ia	AI: CD Audio Right Channel	58	CAP2	Oa	CAP3 through 12 nF
27	MIC1	Ia	AI: Microphone 1 Input	59	CAP3	Ia	AGND through 47 nF
28	MIC2	Ia	AI: Microphone 2 Input	60	GPIO3	It/Ot4	Application assigned
29	LINE_IN_L	Ia	AI: Line In Left Channel	61	GPIO4	It/Ot4	Application assigned
30	LINE_IN_R	Ia	AI: Line In Right Channel	62	GPIO5	It/Ot4	Application assigned
31	AVDD	PWR	+5VA	63	GPIO6	It/Ot4	Application assigned
32	AVSS	AGND	AGND	64	VDD	PWR	+5V or +3.3V
¹ I/O types: Ia Input, analog It Input, TTL Ix Input, crystal/clock It/Ot4 Input, TTL/Output, TTL, 4 mA, 50 pF Oa Output, analog Ot4 Output, TTL, 4 mA, 50 pF Ox Output, crystal				² Interface: AI Audio interface LTI Line/telephone interface AMDC Audio and Modem Digital Controller			

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

4.2 AMC 80-Pin PQFP Pin Assignments

The pin assignments for the AMC in 80-pin PQFP are shown in Figure 4 and are listed in Table 3.

This package has enough GPIOs to support two phones lines.

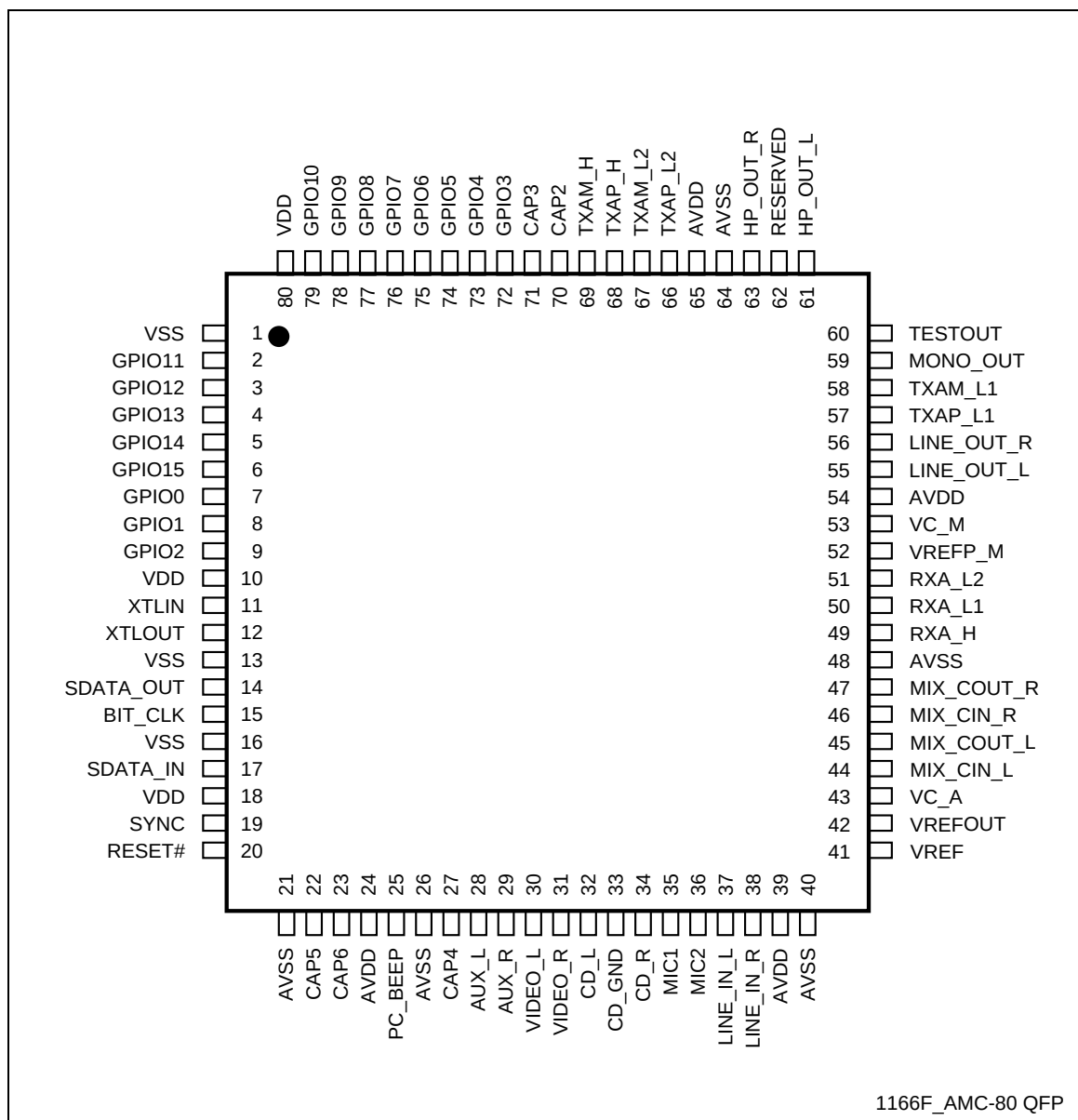


Figure 4. AMC Pin Assignments - 80-Pin PQFP

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Table 3. AMC Pin Assignments - 80-Pin PQFP

Pin	Signal Label	I/O Type ¹	Interface ²	Pin	Signal Label	I/O Type ¹	Interface ²
1	VSS	GND	GND	41	VREF	REF	AGND through 10 uF and 0.1 uF
2	GPIO11	It/Ot4	Application assigned	42	VREFOUT	REF	AGND through 10 uF and 0.1 uF
3	GPIO12	It/Ot4	Application assigned	43	VC_A	REF	AGND through 10 uF and 0.1 uF
4	GPIO13	It/Ot4	Application assigned	44	MIX_CIN_L	Ia	AI: MIX_COUTL through 1 uF
5	GPIO14	It/Ot4	Application assigned	45	MIX_COUT_L	Oa	AI: MIX_CIN_L through 1 uF
6	GPIO15	It/Ot4	Application assigned	46	MIX_CIN_R	Ia	AI: MIX_COUT_R through 1 uF
7	GPIO0	It/Ot4	Application assigned	47	MIX_COUT_R	Oa	AI: MIX_CIN_R through 1 uF
8	GPIO1	It/Ot4	Application assigned	48	AVSS	AGND	AGND
9	GPIO2	It/Ot4	Application assigned	49	RXA_H	Ia	LTI: Handset Receive Analog
10	VDD	PWR	+5V or +3.3V	50	RXA_L1	Ia	LTI: Line 1 Receive Analog
11	XTLIN	Ix	24.576 MHz Crystal/Clock In	51	RXA_L2	Ia	LTI: Line 2 Receive Analog
12	XTLOUT	Ox	24.576 MHz Crystal Out	52	VREFP_M	REF	AGND through 10 uF and 0.1 uF
13	VSS	GND	GND	53	VC_M	REF	AGND through 10 uF and 0.1 uF
14	SDATA_OUT	I	AMDC: SDATA_OUT	54	AVDD	PWR	+5VA
15	BIT_CLK	O	AMDC: BIT_CLK	55	LINE_OUT_L	Oa	AI: Line Out Left Channel
16	VSS	GND	GND	56	LINE_OUT_R	Oa	AI: Line Out Right Channel
17	SDATA_IN	O	AMDC: SDATA_IN	57	TXAP_L1	Oa	LTI: Line 1 Transmit Analog Plus
18	VDD	PWR	+5V or +3.3V	58	TXAM_L1	Oa	LTI: Line 1 Transmit Analog Minus
19	SYNC	I	AMDC: SYNC	59	MONO_OUT	Oa	AI: Speaker
20	RESET#	It	AMDC: RESET#	60	TESTOUT	O	NC
21	AVSS	AGND	AGND	61	HP_OUT_L	Oa	AI: Headphone Out Left Channel
22	CAP5	Ot4	NC	62	RESERVED		NC
23	CAP6	Ot4	NC	63	HP_OUT_R	Oa	AI: Headphone Out Right Channel
24	AVDD	PWR	+5VA	64	AVSS	AGND	AGND
25	PC_BEEP	Ia	AI: PC Speaker beep pass through	65	AVDD	PWR	+5VA
26	AVSS	AGND	AGND	66	TXAP_L2	Oa	LTI: Line 2 Transmit Analog Plus
27	CAP4	Ot4	NC	67	TXAM_L2	Oa	LTI: Line 2 Transmit Analog Minus
28	AUX_L	Ia	AI: Aux Audio Left Channel	68	TXAP_H	Oa	LTI: Handset Transmit Analog Plus
29	AUX_R	Ia	AI: Aux Audio Right Channel	69	TXAM_H	Oa	LTI: Handset Transmit Analog Minus
30	VIDEO_L	Ia	AI: Video Audio Left Channel	70	CAP2	Oa	CAP3 through 12 nF
31	VIDEO_R	Ia	AI: Video Audio Right Channel	71	CAP3	Ia	AGND through 47 nF
32	CD_L	Ia	AI: CD Audio Left Channel	72	GPIO3	It/Ot4	Application assigned
33	CD_GND	GND	AI: CD Audio analog ground	73	GPIO4	It/Ot4	Application assigned
34	CD_R	Ia	AI: CD Audio Right Channel	74	GPIO5	It/Ot4	Application assigned
35	MIC1	Ia	AI: Microphone 1 Input	75	GPIO6	It/Ot4	Application assigned
36	MIC2	Ia	AI: Microphone 2 Input	76	GPIO7	It/Ot4	Application assigned
37	LINE_IN_L	Ia	AI: Line In Left Channel	77	GPIO8	It/Ot4	Application assigned
38	LINE_IN_R	Ia	AI: Line In Right Channel	78	GPIO9	It/Ot4	Application assigned
39	AVDD	PWR	+5VA	79	GPIO10	It/Ot4	Application assigned
40	AVSS	AGND	AGND	80	VDD	PWR	+5V or +3.3V

1. I/O types:

Ia	Input, analog
It	Input, TTL
Ix	Input, crystal/clock
It/Ot4	Input, TTL/Output, TTL, 4 mA, 50 pF
Oa	Output, analog
Ot4	Output, TTL, 4 mA, 50 pF
Ox	Output, crystal

2. Interface:

AI	Audio interface
LTI	Line/telephone interface
AMDC	Audio and Modem Digital Controller

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

4.3 Pin Signal Descriptions

4.3.1 System

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
RESET#	20	15	It	AC '97 Master H/W Reset
XTLIN	11	6	Ix	24.576 MHz Crystal
XTLOUT	12	7	Ox	24.576 MHz Crystal
TESTOUT	60	NA	O	NC

4.3.2 Digital Control, Crystal, Serial I/O

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
BIT_CLK	15	10	O	Bit Clock. 12.288 MHz AC-link bit clock. Connect to Controller BIT_CLK input.
SYNC	19	14	I	Frame Sync. 48 kHz fixed rate sample AC-link sync. Connect to Controller SYNC output.
SDATA_IN	17	12	O	Serial Data Input. Serial, time division multiplexed, AC-link input data stream. Connect to Controller SDATA_IN input.
SDATA_OUT	14	9	I	Serial Data Output. Serial, time division multiplexed, AC-link output stream. Connect to Controller SDATA_OUT output.
RESET#	20	15	It	Reset. Active low reset input. Connect to Controller RESET# input.

4.3.3 General Purpose I/O

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Recommended AC '97 Application		
				Name	I/O	Description
GPIO0	7	2	It/Ot4	LINE1_OH	O	Off Hook Line 1
GPIO1	8	3	It/Ot4	LINE1_RI	I	Ring Detect Line 1
GPIO2	9	4	It/Ot4	LINE1_CID	O	Caller ID path enable Line 1
GPIO3	72	60	It/Ot4	LINE1_LCS	I	Loop Current Sense Line 1
GPIO4	73	61	It/Ot4	LINE1_PULSE	I/O	Optional GPIO / Line 1 pulse dial (out)
GPIO5	74	62	It/Ot4	LINE1_HL1R	I/O	Optional GPIO / HANDSET to Line 1 relay control (out)
GPIO6	75	63	It/Ot4	LINE1_HOHD	I/O	Optional GPIO / HANDSET off hook detect (in)
GPIO7	76	NA	It/Ot4	LINE12_AC	I/O	Optional GPIO / International Bit 1 / Line 1/2 AC (out)
GPIO8	77	NA	It/Ot4	LINE12_DC	I/O	Optional GPIO / International Bit 2 / Line 1/2 DC (out)
GPIO9	78	NA	It/Ot4	LINE12_RS	I/O	Optional GPIO / International Bit 3 / Line 1/2 RS (out)
GPIO10	79	NA	It/Ot4	LINE2_OH	O	Off Hook Line 2
GPIO11	2	NA	It/Ot4	LINE2_RI	I	Ring Detect Line 2
GPIO12	3	NA	It/Ot4	LINE2_CID	O	Caller ID path enable Line 2
GPIO13	4	NA	It/Ot4	LINE2_LCS	I	Loop Current Sense Line 2
GPIO14	5	NA	It/Ot4	LINE2_PULSE	I/O	Optional GPIO / Line 2 pulse dial (out)
GPIO15	6	NA	It/Ot4	LINE2_HL2R	O	Optional GPIO / HANDSET_TO_LINE2 relay control (out)

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

4.3.4 Audio Analog Signals

These signals connect the AC '97 component to analog sources and sinks, including microphones and speakers.

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
PC_BEEP	25	18	Ia	PC Speaker Beep Pass through.
MIC1	35	27	Ia	Microphone 1 Input.
MIC2	36	28	Ia	Microphone 2 Input.
LINE_IN_L	37	29	Ia	Line In Left Channel.
LINE_IN_R	38	30	Ia	Line In Right Channel.
CD_L	32	24	Ia	CD Audio Left Channel.
CD_GND	33	25	Ia	CD Audio Analog Ground.
CD_R	34	26	Ia	CD Audio Right Channel
VIDEO_L	30	22	Ia	Video Audio Left Channel.
VIDEO_R	31	23	Ia	Video Audio Right Channel.
AUX_L	28	20	Ia	Aux Audio Left Channel.
AUX_R	29	21	Ia	Aux Audio Right Channel.
LINE_OUT_L	55	45	Oa	Line Out Left Channel.
LINE_OUT_R	56	46	Oa	Line Out Right Channel.
HP_OUT_L	61	51	Oa	Headphone Out Left Channel.
HP_OUT_R	63	53	Oa	Headphone Out Right Channel .
MONO_OUT	59	49	Oa	Mono Sound Output.

4.3.5 Modem Analog Signals

These signals connect the Codec to telephone line and telephone handset analog signals.

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
TXAP_L1	57	47	Oa	Line 1 Transmit Analog Plus. Plus level of differential analog output signal output to telephone line 1.
TXAM_L1	58	48	Oa	Line 1 Transmit Analog Minus. Minus level of differential analog output signal output to telephone line 1.
RXA_L1	50	42	Ia	Line 1 Receive Analog. Single-ended analog receive input signal from telephone line 1.
TXAP_H	68	56	Oa	Handset Transmit Analog Plus. Plus level of differential analog output signal output to the handset speaker. For DSVD or allowing TAM functions to be independent of modem ADC/DAC.
TXAM_H	69	57	Oa	Handset Transmit Analog Minus. Minus level of differential analog output signal output to the handset speaker. For DSVD or allowing TAM functions to be independent of modem ADC/DAC.
RXA_H	49	41	Ia	Handset Receive Analog. Single-ended analog receive input signal from the handset microphone.
TXAP_L2	66	NA	Oa	Line 2 Transmit Analog Plus. Plus level of differential analog output signal output to telephone line 2.
TXAM_L2	67	NA	Oa	Line 2 Transmit Analog Minus. Minus level of differential analog output signal output to telephone line 2.
RXA_L2	51	NA	Ia	Line 2 Receive Analog. Single-ended analog receive input signal from telephone line 2.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

4.3.6 Filter and Reference Voltage Connections

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
VREF	41	33	REF	Audio Reference Voltage. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
VREFOUT	42	34	REF	Reference Voltage Out. Intended for mic bias, if needed. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
VC_A	43	35	REF	Audio Reference Voltage. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
MIX_CIN_L	44	36	Ia	Mixer Common In Left. Connect to MIX_COUT_L through 1 uF.
MIX_COUT_L	45	37	Oa	Mixer Common Out Left. Connect to MIX_CIN_L through 1 uF.
MIX_CIN_R	46	38	Ia	Mixer Common In Right. Connect to MIX_COUT_R through 1 uF.
MIX_COUTR	47	39	Oa	Mixer Common Out Right. Connect to MIX_COUT_L through 1 uF.
VREFP_M	52	43	REF	Modem Reference Voltage. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
VC_M	53	44	REF	Modem Reference Voltage. Connect to AGND through 10 uF (polarized) and 0.1 uF (ceramic) in parallel.
CAP2	70	58	Oa	Generic Cap. Connect to CAP3 through 12 nF.
CAP3	71	59	Ia	Generic Cap. Connect to AGND through 47 nF.
CAP4	27	NA	Ot4	Generic Cap. No external connection.
CAP5	22	NA	Ot4	Generic Cap. No external connection.
CAP6	23	NA	Ot4	Generic Cap. No external connection.

4.3.7 Power and Ground

Signal Name	Pin (80-PQFP)	Pin (64-TQFP)	I/O Type	Description
AVDD	24, 39, 54, 65	16, 31, 50, 55	PWR	Digital Portion of Analog Circuit Power. Connect to +5VA.
AVSS	21, 26, 40, 48, 64	17, 19, 32, 54, 40	GND	Analog Ground. Connect to AGND.
VDD	10, 18, 80	5, 13, 64	PWR	Digital Circuit Power. Connect to + 5V or +3.3V.
VSS	1, 13, 16	1, 8, 11	GND	Digital Ground. Connect to GND.

5. Specifications

5.1.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage VDD = +3.3V VDD = +5V	VDD	-0.3 to +4.6 -0.3 to +6.0	V
Digital Input Voltage	VIN	-0.3 to (VDD + 0.3)	V
Operating Temperature Range	TA	-0 to +70	°C
Storage Temperature Range	TSTG	-55 to +125	°C
Analog Input Voltage	VIN	-0.3 to (AVDD + 0.3)	V
Voltage Applied to Outputs in High Impedance (Off) State	VHZ	-0.3 to (VDD + 0.3)	V
DC Input Clamp Current	I _{IK}	±20	mA
DC Output Clamp Current	I _{OK}	±20	mA
Static Discharge Voltage (25°C)	VESD	±2500	V
Latch-up Current (25°C)	I _{TRIG}	±300	mA

5.1.2 Current and Power Requirements

Table 5. Current and Power Requirements

Mode	Typical Current (mA)	Maximum Current (mA)	Typical Power (mW)	Maximum Power (mW)	Notes
Normal Mode	63.4	-	317.0	-	VDD = +5V
Sleep Mode	-	-	-	-	VDD = +5V
Normal Mode	56.3	-	185.8	-	VDD = +3.3V
Sleep Mode	-	-	-	-	VDD = +3.3V
Notes: 1. Operating voltage: VDD = +3.3V ± 0.3V or +5V ± 5%; AVDD = 5VA ± 5%. 2. Test conditions for VDD = +3.3V; VDD = +3.3V for typical values; VDD = +3.6V for maximum values. 3. Test conditions for VDD = +5V; VDD = +5.0V for typical values; VDD = +5.25V for maximum values. 4. Test conditions for AVDD = +5V; AVDD = +5.0V for typical values; AVDD = +5.25V for maximum values. 5. Input Ripple ≤ 0.1 V _{peak-peak} . 6. f = Internal frequency. 7. Stop Mode is the same as Sleep Mode with clocks turned off.					

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

5.1.3 DC Electrical Characteristics

Table 6. DC Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Input voltage range	V_{in}	-0.30	-	3.60	V	VDD = +3.6V
Input voltage range	V_{in}	-0.30	-	5.25	V	VDD = +5.25V
Low level input voltage	V_{il}	-0.30	-	0.25*VDD	V	
High level input voltage	V_{ih}	0.65*VDD	-	VDD + 0.3	V	
High level output voltage	V_{oh}	0.85*VDD	-	VDD	V	
Low level output voltage	V_{ol}	0	-	0.1*VDD	V	
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA	
Output Leakage Current (Hi-Impedance AC-link outputs)	-	-10	-	10	uA	
GPIO Output sink current at 0.4 V maximum	-	2.4	-	-	mA	
GPIO Output source current at 2.97 V minimum	-	2.4	-	-	mA	
GPIO rise/fall time		20		100	ns	
Test conditions unless otherwise noted: 1. Temperature 25 °C 2. Digital Supply (VDD) 3.3V ± 0.3V or 5.0V ± 5% 3. Digital GND (VSS) 0 V 4. External Load 50 pF						

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5.1.4 AC Performance Characteristics

Table 7. AC Performance Characteristics

Parameter	Min	Typical	Max	Units
Full Scale Input Voltage				
LINE_IN	-	1.0	-	Vrms
MIC (+20 dB Boost on)	-	0.1	-	Vrms
MIC (+20 dB Boost off)	-	1.0	-	Vrms
Full Scale Output Voltage				
LINE_OUT	-	1.0	-	Vrms
HP_OUT	-	-	1.41	Vrms
Analog S/N				
CD to LINE_OUT, HP_OUT, or MONO_OUT	90	-	95	dB
MIC (+20 dB Boost on) to LINE_OUT, HP_OUT, or MONO_OUT	-	83	90	dB
Other to LINE_OUT, HP_OUT, or MONO_OUT	90	-	95	dB
Analog Frequency Response (± 1 dB limits)	20	-	20,000	Hz
Digital S/N ¹				
D/A	85	90	92	dB
A/D	75	80	85	dB
Total Harmonic Distortion:				
LINE_OUT (0 dB gain, 20 kHz BW, 48 kHz Sample Frequency)	-	-	0.02	%
HP_OUT (0 dB gain, 20 kHz BW, 48 kHz Sample Frequency)	-	-	1.0	%
D/A and A/D Frequency Response (± 0.25 dB limits max; ± 0.10 dB typ)	20	-	20,000	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection ²	-74	-	-	dB
Out-of-Band Rejection ³	-	-40	-	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1 kHz)	-	-40	-	dB
Crosstalk between Input channels	-	-	-85	dB
Crosstalk between headphone channels	-	-	-85	dB
Crosstalk between line ADC/DAC and any other channel	-	-	-85	dB
Isolation between audio and modem sections	100	-	-	dB
Spurious Tone Reduction	-	-100	-	dB
Attenuation, Gain Step Size (except for PC Beep)	-	1.5	-	dB
Interchannel Gain Mismatch (Difference between errors)	-0.5	-	0.5	dB
Absolute Gain Step Error at any given setting	-	-	0.75	dB
Input Impedance				
LINE_OUT	10K	-	-	ohm
MONO_OUT	10K	-	-	ohm
HP_OUT	10K	-	-	ohm
Input Capacitance	-	15	-	pF
Vrefout	-	2.5	-	V
DC Offset				
Audio ADCs	-	± 10	± 50	mV
Other ADCs	-	-	± 100	mV
Audio DACs	-	± 5	± 25	mV
Other DACs	-	-	± 100	mV

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Table 7. AC Performance Characteristics (Cont'd)

Parameter	Min	Preliminary	Max	Units
Modem Line				
DAC to Line Driver output SNR at -10 dBm, 1200Ω	77	-	80	dB
Line Input to ADC SNR at -6 dBm	77	-	80	dB
Handset				
DAC to Line Driver output SNR at -10 dBm, 1200Ω	77	-	80	dB
Line Input to ADC SNR at -6 dBm	77	-	80	dB
Mic ADC				
Line Input to ADC SNR at -6 dBm without 20 dB boost	77	-	80	dB
Line Input to ADC SNR at -6 dBm with 20 dB boost	-	65	-	dB

Notes:

1. The ratio of the rms output level with 1KHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20Hz to a 20KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
2. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
3. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 VRMS DAC output.

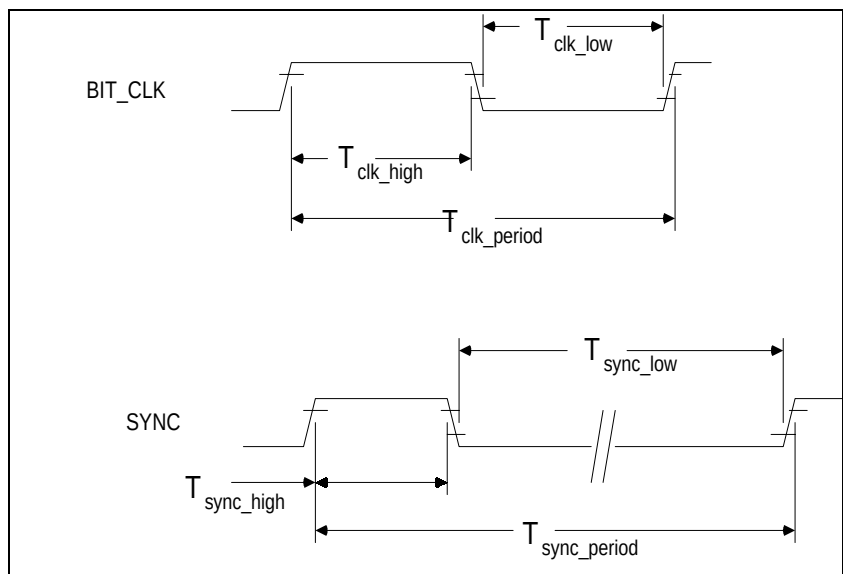
Standard test conditions unless otherwise noted:

Temperature	25 °C	
Analog Supply (AVDD)	5.0 V ±5%	
Digital Supply(VDD)	3.3 V ±0.3V	
Input Voltage Levels:	VDD = +5 V	VDD = +3.3 V
Logic Low	0.8 V	1.0 V
Logic High	2.4 V	2.97 V
Input signal	1 KHz sine wave	
Sample Frequency(FS)	48 KHz	
0 dBV = 1 Vrms		
10 kohm/50 pF load		
Testbench Characterization BW:		
Pass Band	20 Hz - 20 kHz	
Attenuation	0 dB	
Gain on inputs	0 dB	

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

5.1.5 AC Timing Characteristics

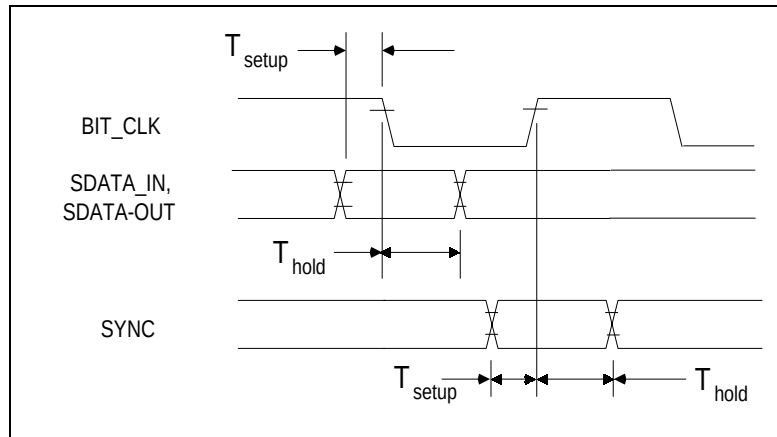
Clocks



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	T_{clk_period}	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BIT_CLK high pulse width (Note 1)	T_{clk_high}	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 1)	T_{clk_low}	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	T_{sync_period}	-	20.8	-	us
SYNC high pulse width	T_{sync_high}	-	1.3	-	us
SYNC low pulse width	T_{sync_low}	-	19.5	-	us
Notes: 1. Worst case duty cycle restricted to 40/60. 2. 50 pF external load.					

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

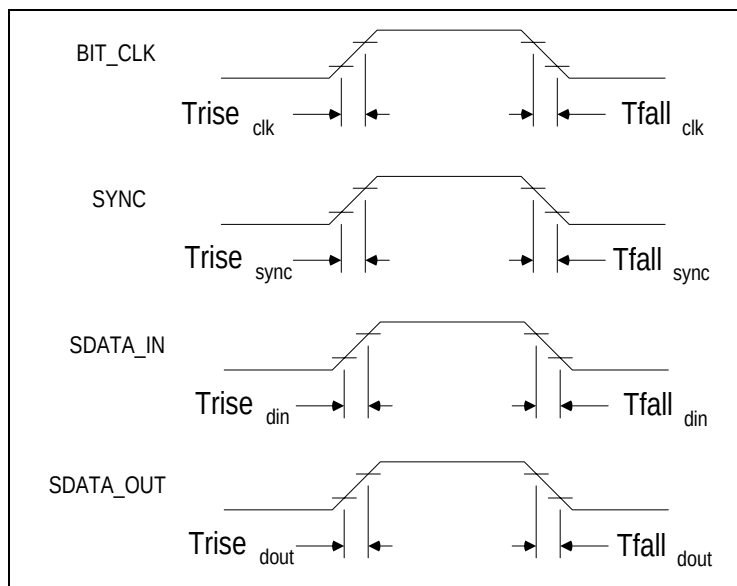
Data Setup and Hold



Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	T_{setup}	15.0	-	-	ns
Hold from falling edge of BIT_CLK	T_{hold}	5.0	-	-	ns
Note: Setup and hold time parameters for SDATA_IN are with respect to the RipTide™ Controller .					

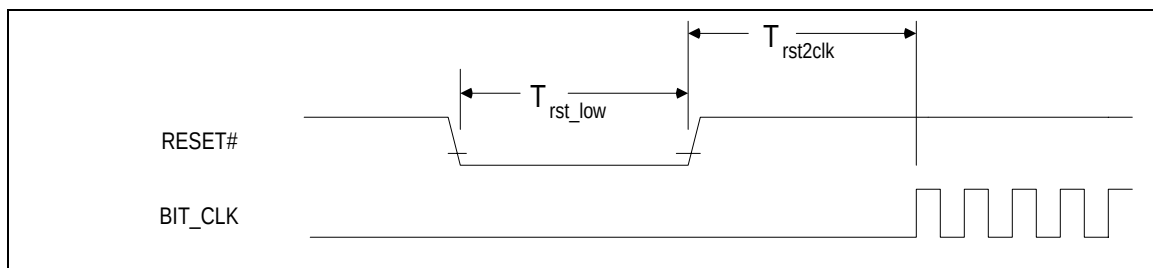
RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Signal Rise and Fall Times



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	$T_{rise_{clk}}$	2	-	6	ns
BIT_CLK fall time	$T_{fall_{clk}}$	2	-	6	ns
SYNC rise time	$T_{rise_{sync}}$	2	-	6	ns
SYNC fall time	$T_{fall_{sync}}$	2	-	6	ns
SDATA_IN rise time	$T_{rise_{din}}$	2	-	6	ns
SDATA_IN fall time	$T_{fall_{din}}$	2	-	6	ns
SDATA_OUT rise time	$T_{rise_{dout}}$	2	-	6	ns
SDATA_OUT fall time	$T_{fall_{dout}}$	2	-	6	ns
Note: 50pF external load; from 10% to 90% of VDD.					

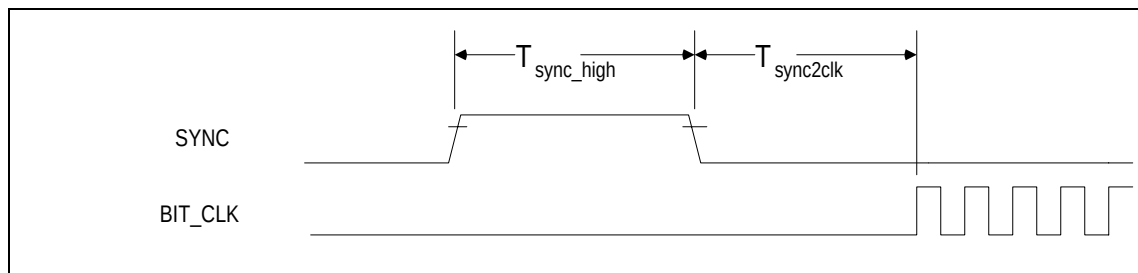
RESET# (Cold Reset)



Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	T_{rst_low}	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	$T_{rst2clk}$	162.8	-	-	ns

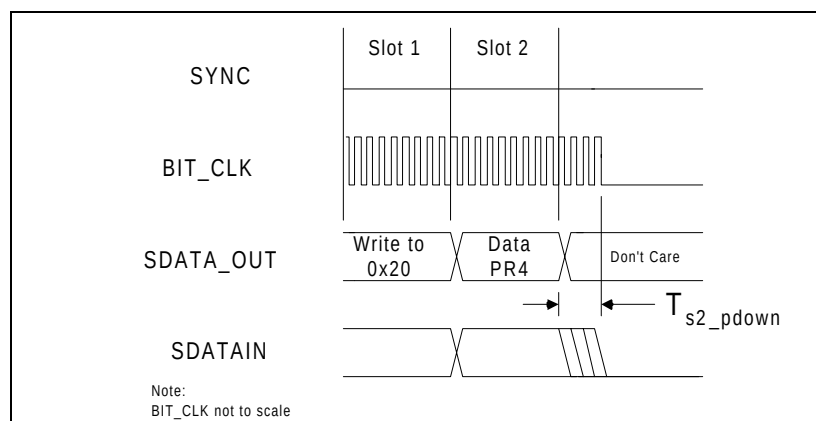
RipTide AMC '97 Audio Modem Codec (AMC) Product Description

RESET# (Warm Reset)



Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	T_{sync_high}	-	1.3	-	us
SYNC inactive to BIT_CLK startup delay	$T_{sync2clk}$	162.8	-	-	ns

AC-link Low Power Mode Timing



Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	T_{s2_pdown}	-	-	1.0	uS

Miscellaneous

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# and SYNC	T_{off}	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	T_{off}	-	-	25.0	ns

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

5.1.6 Crystal Specification

Table 8 lists the required crystal parameters. Note that the crystal circuit will be optimized for digital 3.3 V operation and thus the part is intended for this digital supply voltage.

Table 8. Crystal Specification

Parameter	Range
Frequency	24.576 MHz
Oscillation Mode	Fundamental
Resonance	Parallel
Load Capacitance	22 pF
Frequency Tolerance	± 40 ppm @ 25 °C
Temperature Stability	± 45 ppm, 0-70 °C
Operating Temperature	0 - 70 °C
Shunt Capacitance	< 7 pF
Equivalent Series Resistance	< 40 ohms @ 20 nW Drive Level
Drive Level	100 uW Correlation, 300 uW Max
Aging	± 15 ppm over 5 years
Storage Temperature Range	-40 to +85C

6. General Description

6.1 Digital Interface

The codec communicates with the controller via a digital serial link (AC-link). All digital audio streams, modem line codec stream, handset, GPIO, and command/status information is transferred between the controller and the codec over this point to point serial channel. The AC-link interface signals are shown in Figure 5 and are described in Table 9.

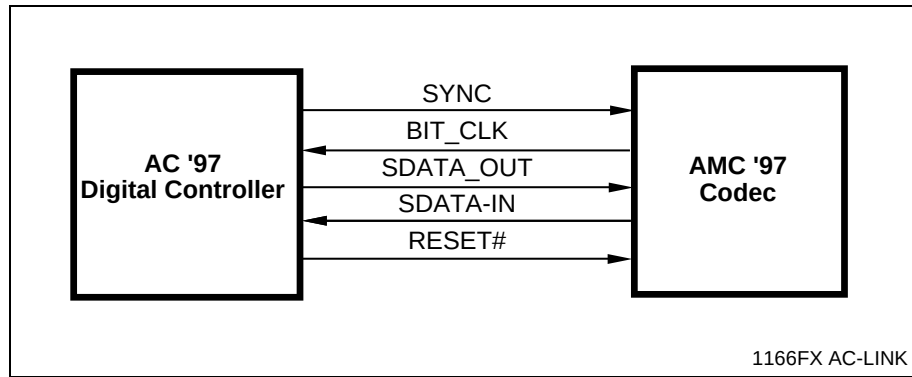


Figure 5. AMC '97 Codec Connection to AC '97 Controller

Table 9. AC-link Serial Interface Signals

Signal Name	I/O	Description
SYNC	I	48 kHz fixed rate sample synchronization from the controller.
BIT_CLK	O	12.288 MHz serial data clock from the codec.
SDATA_IN	O	Serial data stream from the codec to the controller.
SDATA_OUT	I	Serial data stream from the controller to the codec.
RESET#	I	Master hardware reset from the controller

The control and status slots allow writing and reading of registers internal to the AC '97 codec. These registers are defined as 16 bit and are addressed at word aligned byte addresses 0x00, 0x02, 0x04, ..., 0x7e. Registers 0x00 - 0x58 are predefined, 0x5a - 0x7a are reserved for the vendor, 0x7c and 0x7e are for the vendor ID.

Because provisions exist for the modem and other sample rates to be less than 48 kHz, the TAG slot contains bits which indicate the validity of each slot in the serial stream.

The AMC '97 specification also defines slot request bits that allow the codec to request samples from the controller. These bit definitions (active low) are implemented as defined in that specification.

When a slot is valid for the outgoing stream, the controller places a one in the corresponding bit position in the TAG slot. For all slots other than the PCM left and right slots, the codec ignores the data present in the slot when the slot's tag bit is a 0 for that particular data phase. This allows the controller to simply repeat the current sample if desired. However, the controller must respond properly to the SLOTREQ bits. For the PCM left and right slots, the codec assumes every slot is valid. If the slot is invalid, the controller must send 0's for the data.

When a slot is valid for the incoming stream, the codec places a one in the corresponding bit position in the TAG slot. The controller must ignore the data present in the slot when the slot's tag bit is a 0 for that particular data phase. The Codec puts zeros in the slot when the slot is invalid.

The AC-link request for status always returns in the next frame. The request is, therefore, always delayed by one frame time. A write request in the current frame will not affect the status that is returned in that particular write frame. Read-Modify-Writes across the AC-link will thus incur latency issues and must be accounted for by the controller.

For fixed 48 kHz sample rate operation, the SLOTREQ bits are always set active and a sample is transferred each frame.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

For optional multiple sample rate input, the tag bit for each input slot indicates whether valid data is present or not. The AMC '97 codec configured for fixed 48 kHz operation is backwards compatible with AC '97 controllers.

Thus, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT(controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame that should be set or reset by the controller.

Any protocol violation in the AC-link, e.g., less than 256 BIT_CLKs in a SYNC frame, will result in a warm reset of the codec. This will be indicated by TESTOUT pin (80-pin PQFP only) output toggling from 0 to 1. This output will stay high until a cold reset occurs.

6.1.1 Rockwell AMC '97 Codec

The Rockwell AMC '97 codec (AMC) is implemented only as a primary codec. The time slots supported by the AMC are listed in Table 10.

Table 10. AMC '97 Slot Assignments

Slot Number	SDATAOUT (Controller to Codec)	SDATAIN (Codec to Controller)
0	TAG	TAG
1	Command Address Port	Status Address Port
2	Command Data Port	Status Data Port
3	PCM Playback Left Channel	PCM Record Left Channel
4	PCM Playback Right Channel	PCM Record Right Channel
5	Modem Line 1 DAC Input Data	Modem Line 1 ADC Output Data
6	Not Supported	Mic ADC Output Data
7	Not Supported	Not Supported
8	Not Supported	Not Supported
9	Not Supported	Not Supported
10	Modem Line 2 DAC Input Data	Modem Line 2 ADC Output Data
11	Handset DAC Input Data	Handset ADC Output Data
12	GPIO Control	GPIO Status

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.2 SDATA_IN (Codec to Controller) Slot Definitions

6.2.1 Input Slot 1: Status Address Port / SLOTREQ Bits

Slot 1, the Status Address Port, delivers codec control register read address *and* variable sample rate slot request flags for all output slots. Bits 11 to 2 are defined as data request flags for output Slots 3-12.

Input Slot 1: Status Address Port	
Bit	Description
19	Reserved. Set to 0 by the codec.
18:12	Control Register Index. Echo of register index for which data is being returned. Set to 0s if tagged "invalid" by the controller.
11:2	"On Demand" Data Request Flags (next output frame). 0 = Send data, 1 = Do not send data.
11	Slot 3 Request. PCM Left channel.
10	Slot 4 Request. PCM Right channel.
9	Slot 5 Request. Modem Line 1.
8	Slot 6 Request. Not used. Set to 0 by the codec.
7	Slot 7 Request. Not used. Set to 0 by the codec.
6	Slot 8 Request. Not used. Set to 0 by the codec.
5	Slot 9 Request. Not used. Set to 0 by the codec.
4	Slot 10 Request. Modem Line 2.
3	Slot 11 Request. Handset.
2	Slot 12 Request. GPIO.
1:0	Reserved. Set to 0 by the codec.

The Slot 1 tag bit is independent of the bit 11:2 slot request field, and **only** indicates valid Status Address Port data (Control Register Index). The AMC sets SDATA_IN tag bits for Slot 1 (Address) and Slot 2 (Data) to "1" when returning valid data from a previous register read. They are otherwise set to 0. SLOTREQ bits have validity independent of the Slot 1 tag bit.

SLOTREQ Behavior and Power Management

SLOTREQ bits for fixed rate, powered down, and all unsupported Slots are driven with 0s for maximum compatibility with the original AC '97 Component Specification. When a DAC channel is powered down, it disappears completely from the serial frame: output tag and slot are ignored, and the SLOTREQ bit is absent (forced to zero). The SLOTREQ bit is forced to "1" in the interval between when the power-down bit for its associated channel is turned off and when its channel is ready to accept samples. The controller can take advantage of this scheme to eliminate the need to poll the AMC status registers.

To power down a channel, the controller needs only to:

1. Disable the source of DAC samples in controller.
2. Set the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.

To power up a channel, the controller needs only to:

1. Clear the PR bit for DAC channel in codec registers 26h, 2Ah, or 3Eh.
2. Enable the source of DAC samples in controller.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Variable Sample Rate Signaling Protocol

For variable sample rate output, the codec examines its sample rate control registers, the state of its FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits asserted during the current audio input frame signal which *active output slots* require data from the controller in the next audio output frame. An *active output slot* is defined as any slot supported by the codec that is not in a power-down state. For fixed 48 kHz operation, the SLOTREQ bits are always set active (low) and a sample is transferred in each frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame.

Upon reset, the audio sample rate registers default to 48 kHz.

The VRM bit controls the optional MIC ADC behavior. SLOTREQ bits for active modem DACs are always treated as valid (data on demand).

6.2.2 Input Slot 2: Status Data Port

Input Slot 2, the Status Data Port, port delivers 16-bit control register read data.

Input Slot 2: Status Data Port	
Bit	Description
19:4	Control Register Read Data. Stuffed with 0's if tagged "invalid" by the codec.
11:0	Reserved. Stuffed with 0's by the codec.

6.2.3 Input Slot 3: PCM Left Record Data

Input Slot 3 contains the 18-bit PCM left channel ADC output data.

Input Slot 3: PCM Left Channel ADC Output Data	
Bit	Description
19:2	PCM Left Channel ADC Output Data. 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	Not Used. Stuffed to 0's by the codec.

6.2.4 Input Slot 4: PCM Right Record Data

Input Slot 4 contains the 18-bit PCM right channel ADC output data.

Input Slot 4: PCM Right Channel ADC Output Data	
Bit	Description
19:2	PCM Right Channel ADC Output Data. 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	Not Used. Stuffed to 0's by the codec.

6.2.5 Input Slot 5: Modem Line 1 ADC Output Data

Input Slot 5 contains the 16-bit Modem Line 1 ADC output data.

Input Slot 5: Modem Line 1 ADC Output Data	
Bit	Description
19:4	Modem Line 1 ADC Output Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the codec.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.2.6 Input Slot 6: Microphone ADC Output Data

Input Slot 6 contains the 16-bit Microphone ADC output data.

Input Slot 6: Microphone ADC Output Data	
Bit	Description
19:4	Microphone ADC Output Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the codec.

6.2.7 Input Slots 7-9: Reserved

Input Slots 7-9 are reserved.

Input Slot 7-9: Reserved	
Bit	Description
19:0	Microphone ADC Output Data. Stuffed to 0's by the codec.

6.2.8 Input Slot 10: Modem Line 2 ADC Output Data

Input Slot 10 contains the 16-bit Modem Line 1 ADC output data.

Input Slot 10: Modem Line 2 ADC Output Data	
Bit	Description
19:4	Modem Line 2 ADC Output Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the codec.

6.2.9 Input Slot 11: Handset ADC Output Data

Input Slot 11 contains the 16-bit Handset ADC output data.

Input Slot 11: Handset ADC Output Data	
Bit	Description
19:4	Handset ADC Output Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the codec.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.2.10 Input Slot 12: GPIO Control

Input Slot 12 contains the GPIO status bits. The codec constantly updates the status slot based upon the logic level detected at each GPIO configured for input. The controller must debounce the reported states as required for the 48 kHz sample rate.

Input Slot 12: GPIO Status	
Bit	Description
19:4	GPIO[15:0] Status. 1 = High level detected at input pin; 0 = Low level detected at input pin. Bits corresponding to GPIO outputs reflect the command level.
19	GPIO15 Status. Application assigned. Not supported by the 64-pin TQFP.
18	GPIO14 Status. Application assigned. Not supported by the 64-pin TQFP.
17	GPIO13 Status. Application assigned. Not supported by the 64-pin TQFP.
16	GPIO12 Status. Application assigned. Not supported by the 64-pin TQFP.
15	GPIO11 Status. Application assigned. Not supported by the 64-pin TQFP.
14	GPIO10 Status. Application assigned. Not supported by the 64-pin TQFP.
13	GPIO9 Status. Application assigned. Not supported by the 64-pin TQFP.
12	GPIO8 Status. Application assigned. Not supported by the 64-pin TQFP.
11	GPIO7 Status. Application assigned. Not supported by the 64-pin TQFP.
10	GPIO6 Status. Application assigned.
9	GPIO5 Status. Application assigned.
8	GPIO4 Status. Application assigned.
7	GPIO3 Status. Application assigned.
6	GPIO2 Status. Application assigned.
5	GPIO1 Status. Application assigned.
4	GPIO0 Status. Application assigned.
3:0	Not Used. Stuffed to 0's by the codec.

6.3 SDATA_OUT (Controller to Codec) Slot Definitions

6.3.1 Output Slot 1: Command Address Port

Output Slot 1, the Command Address Port, is used to control features and monitor status (see Input Slots 1 and 2) for codec functions such as mixer settings and power management.

Output Slot 1: Command Address Port	
Bit	Description
19	Read/Write Command. 1 = Read; 0 = Write.
18:12	Control Register Index. 64 16-bit locations, addressed on even byte boundaries.
11:0	Not Used. Stuffed to 0's by the controller.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.3.2 Output Slot 2: Command Data Port

Output Slot 2, the Command Data Port, is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle (as indicated by Slot 1, bit 19). If the current command port operation is a read, then the entire slot time must be stuffed with 0's by the controller.

Output Slot 2: Command Data Port	
Bit	Description
19	Read/Write Command. 1 = Read; 0 = Write.
18:12	Control Register Index. 64 16-bit locations, addressed on even byte boundaries.
11:0	Not Used. Stuffed to 0's by the controller.

6.3.3 Output Slot 3: PCM Left Playback Data

Output Slot 3 contains the 18-bit PCM left channel DAC input data.

Output Slot 3: PCM Left Channel DAC Input Data	
Bit	Description
19:2	PCM Left Channel DAC Input Data. 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	Control Register Index. Stuffed to 0's by the controller.

6.3.4 Output Slot 4: PCM Right Playback Data

Output Slot 4 contains the 18-bit PCM right channel DAC input data.

Output Slot 4: PCM Right Channel DAC Input Data	
Bit	Description
19:2	PCM Right Channel DAC Input Data. 18-bit sample (bit 19 = MSB; bit 2 = LSB).
1:0	Control Register Index. Stuffed to 0's by the controller.

6.3.5 Output Slot 5: Modem Line 1 DAC Input Data

Output Slot 5 contains the 16-bit Modem Line 1 DAC input data.

Output Slot 5: Modem Line 1 DAC Input Data	
Bit	Description
19:4	Modem Line 1 DAC Input Data. 16-bit sample (bit 19 = MSD; bit 4 = LSD)
3:0	Not Used. Stuffed to 0's by the controller.

6.3.6 Output put Slots 6-9: Reserved

Output Slots 6-9 are reserved.

Output Slot 6-9: Reserved	
Bit	Description
19:0	Reserved. Stuffed to 0's by the controller.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.3.7 Output Slot 10: Modem Line 2 DAC Input Data

Output Slot 10 contains the 16-bit Modem Line 2 input data.

Output Slot 10: Modem Line 2 DAC Input Data	
Bit	Description
19:4	Modem Line 2 Input Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the controller.

6.3.8 Output Slot 11: Handset DAC Input Data

Output Slot 11 contains the 16-bit Handset DAC input data.

Output Slot 11: Handset DAC Input Data	
Bit	Description
19:4	Handset DAC Input Data. 16-bit sample (bit 19 = MSB; bit 4 = LSB).
3:0	Not Used. Stuffed to 0's by the controller.

6.3.9 Output Slot 12: GPIO Status

Output Slot 12 contains the GPIO control bits. The codec constantly sets the GPIOs that are configured for output based upon the value of the corresponding bit position of the control slot.

Output Slot 12: GPIO Control	
Bit	Description
19:4	GPIO[15:0] Control. 1 = High level at the codec output pin.; 0 = Low level at the codec output pin. Bits corresponding to GPIO inputs are set to 0 by the controller.
19	GPIO15 Control. Application assigned. Not supported by the 64-pin TQFP.
18	GPIO14 Control. Application assigned. Not supported by the 64-pin TQFP.
17	GPIO13 Control. Application assigned. Not supported by the 64-pin TQFP.
16	GPIO12 Control. Application assigned. Not supported by the 64-pin TQFP.
15	GPIO11 Control. Application assigned. Not supported by the 64-pin TQFP.
14	GPIO10 Control. Application assigned. Not supported by the 64-pin TQFP.
13	GPIO9 Control. Application assigned. Not supported by the 64-pin TQFP.
12	GPIO8 Control. Application assigned. Not supported by the 64-pin TQFP.
11	GPIO7 Control. Application assigned. Not supported by the 64-pin TQFP.
10	GPIO6 Control. Application assigned.
9	GPIO5 Control. Application assigned.
8	GPIO4 Control. Application assigned.
7	GPIO3 Control. Application assigned.
6	GPIO2 Control. Application assigned.
5	GPIO1 Control. Application assigned.
4	GPIO0 Control. Application assigned.
3:0	Not Used. Stuffed to 0's by the controller.

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

6.4 General Purpose Inputs/Outputs

The Codec contains a number of General Purpose Input/Outputs suitable for easy connection with minimal parts to a DAA circuit. The controller must configure any GPIOs as outputs on power-up.

When configured as an input, a GPIO performs as a CMOS Schmitt triggered input for a 3.3V power supply. The board designers are responsible for connecting unused pins to VDD or VSS. However, to prevent excess power loss due to floating conditions during an extended reset period, all GPIOs, when RESET# is asserted, are pulled down.

The GPIOs are tristated to a high impedance state on power-on or a cold reset. The controller must first enable the output after setting it to the desired state. To prevent overdrive of any transistors, the outputs have slow rise and fall times. Typical values should be 40 ns. In addition, the device sinks 2.4 mA at a maximum level of 0.4V and sources 2.4 mA at a minimum level of 2.97V.

Upon a warm reset, the GPIOs that are configured for outputs maintain their output values. As long as the controller does not tag the GPIO control slot as valid, the outputs will not change.

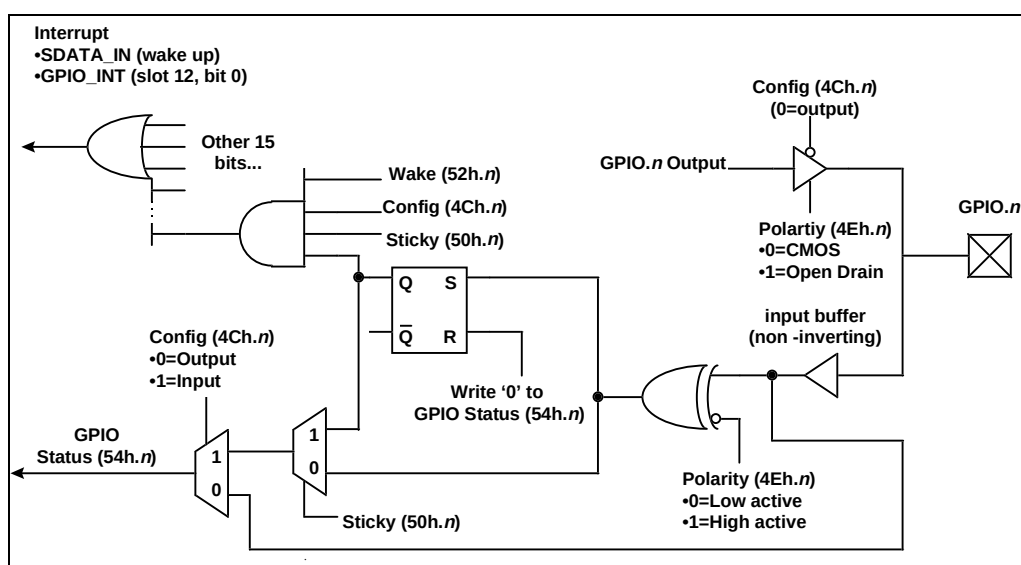


Figure 6. Conceptual GPIO Configuration

6.5 Low Power Modes

The Codec is a fully static design, i.e., when the clock is stopped to any subsection of the device, that subsection maintains its value.

The low power modes specified in Section 7 of the AC '97 Specification are supported in full, i.e., the modem ADCs/DACs, the handset ADC/DAC, and the mic ADC can be individually powered down and up. See the appropriate registers for control, which are the Power-down Control/Status and the Modem Power-down Control/Status.

The following paragraph shows an example of the procedure that would occur to wake-up the PC system using GPIOs in the controller in the D3 cold state with VAUX power. In this example, normal operation is occurring. The controller gets told to go into the D3hot state, meaning within a short period of time the RipTide system will be at the D3cold state. The controller would then

1. Using the Modem Power-down Control/Status register:
 - a) Shut down the 3D block (P3D).
 - b) Shut down the Line ADCs/DACs (PRB, PRC, PD1, PD2).
 - c) Shut down the Handset ADC/DAC (PRE, PRD).
 - d) Shut down the mic ADC (PRF).
 - e) Shut down the modem voltage reference (PREF).

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2. Using the Power-down Control/Status register:

- a) Shut down the stereo ADC/DAC (PR0, PR1).
- b) Optionally shut down the stereo and mono amplifiers (PDA, PDM), depending upon if the analog still needs to be running.
- c) Optionally shut down the analog mixer with Vref on or off, depending upon if the analog still needs to be running.

GPIOs toggling on the codec are detected by the controller across the AC-link which then forces the PCI bus PME# signal low. Operating system wake-up then occurs with the PC system giving a PCI reset to the controller and the controller then either going through the reverse of the above procedure or issuing a cold reset to restore everything to the normal state.

6.6 Loop Back Modes

Several loop back modes are defined for the ADC/DAC pairs as well as the microphone ADC. These loop back modes are for diagnostic and test purposes. The description of the modes occurs in this section; however, the positions of the controlling bits are detailed in the Mixer Register definition section.

Because the dedicated microphone ADC has no associated DAC, it must “borrow” a DAC from another source. Somewhat randomly, the source chosen is the handset DAC. Therefore, when referring to the microphone ADC loop back paths, the handset DAC is meant.

In keeping with proper AC-link terminology, AC-link Outgoing streams go INTO the AMC '97 audio modem codec, while AC-link Incoming streams go OUT of the codec.

Note that the DAC outputs are squelched automatically when the loop back modes are used.

6.6.1 Modem/Handset/Microphone Loop Back Definitions

The following definitions apply to the modem line 1, modem line 2, handset, and dedicated microphone ADC/DAC pairs. To conserve register space, implementation of the modes are done by combinations of bits, rather than by individual bits, with the exception of the one-bit output bit.

ADC Loop Back

The ADC Loop Back travels from the Line input signal through the continuous time anti-aliasing filter, the delta-sigma ADC, the lowpass switched capacitor filter, the lowpass continuous time filter, and then to the Line output.

Line In -> AAF -> ADC -> SCF -> CTF -> Line Out.

Local Analog Loop Back

Otherwise known as Loop3, the digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the comb filter, the delta-sigma DAC, the lowpass switched capacitor filter, the lowpass continuous time filter, routed back through the delta-sigma ADC, the sinc decimation filter, and then out onto the appropriate incoming stream slot of the AC-link.

AC-link Out Stream -> DAC -> SCF -> CTF -> ADC -> Decimation -> AC-link In Stream

DAC Digital Loop Back

The DAC Digital Loop Back is a purely digital loop back. The digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the comb filter, the delta-sigma DAC, back to the sinc decimation filter, and then out onto the appropriate incoming stream slot of the AC-link.

AC-link Out Stream -> DAC -> Decimation -> AC-link In Stream

Remote Analog Loop Back

Otherwise known as Loop4, the Line input signal is passed through the line anti-aliasing filter and routed directly back to the Line output.

Line In -> AAF -> Line Out

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ADC and DAC Loop Back Combined

This mode provides the option to perform both of the ADC and DAC loop backs at the same time since they use separate blocks of the codec.

SCF One-bit In

This mode enables the one-bit input of the SCF. The input to the SCF comes from one of the device pads. This pad is one of the GPIOs and only occurs when in test mode. This is for debugging purposes only.

DAC One-bit out

This mode enables the one-bit output of the DAC modulator to be accessible by an output pad. This pad is one of the GPIOs and only occurs when in test mode. This is for debugging purposes only.

6.6.2 Audio ADC/DAC Loop Back Definitions

The following definitions apply to the audio ADC/DAC pairs. To conserve register space and to provide backward compatibility to AC '97, implementation of the modes are done by both a combination of bits and individual bits. Some have been defined previously by the AC '97 spec.

ADC to DAC Loop Back

The LPBK bit enables loop back of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. This will provide both left and right loop backs to occur simultaneously for backward compatibility. Individual bits are required to allow for left ADC to left DAC and right ADC to right DAC independently of each other.

DAC to ADC Loop Back

The DAC to ADC Loop Back is a purely digital loop back. The digital bit stream from the appropriate outgoing stream slot of the AC-link is passed through the interpolation filter, the delta-sigma DAC, back to the sinc and decimation filters, and then out onto the appropriate incoming stream slot of the AC-link.

AC-link Out Stream -> DAC -> Decimation -> AC-link In Stream

SCF One-bit In

This mode enables the one-bit input of the SCF. The input to the SCF comes from one of the device pads. This pad is one of the GPIOs and only occurs when in test mode. This is for debugging purposes only.

DAC One-bit out

This mode enables the one-bit output of the DAC modulator to be accessible by an output pad. This pad is one of the GPIOs and only occurs when in test mode. This is for debugging purposes only.

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7. Interface Registers

Table 11 identifies the AMC'97 Codec registers and bits.

Table 11. Audio Modem Codec (AMC) Registers

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	5573h
02h	Play Master Volume	Mute	x	ML5	ML4	ML3	ML2	ML1	ML0	x	x	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Headphone Volume	Mute	x	ML5	ML4	ML3	ML2	ML1	ML0	x	x	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Mono Master Volume	Mute	x	x	x	x	x	x	x	x	x	MM5	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV2	PV0	x	0000h
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	GN5	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h
1Eh	Record Gain Mic	Mute	x	x	x	x	x	x	x	x	x	x	x	GM3	GM2	GM1	GM0	8000h
20h	General Purpose	POP	x	3D	LD	x	x	MIX	MS	LPBK	x	PCMS	x	x	x	x	x	0000h
22h	3D Control	X	x	x	x	CR3	CR2	CR1	CR0	x	x	x	x	DP3	DP2	DP1	DP0	0300h
26h	Power-down Control/Status	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	PDM	PDA	x	REF	ANL	DAC	ADC	000xh
28h	Extended Audio ID	ID1 0	ID0 0	x	x	x	x	x	LDAC 0	SDAC 0	CDAC 0	x	x	VRM 1	x	DRA 0	VRA 0	0008h
2Ah	Extended Audio Status/Control	x	PRL	x	x	x	x	MADC	LDAC	SDAC	CDA	x	x	VRM	x	DRA	VRA	4x00h
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	x	x	HSET	LIN 2	LIN1	0007h~ 0005h#
3Eh	Extended Modem Status/Control	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	FFxxh
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line 2 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
4Ah	Handset DAC/ADC level	Mute	x	x	DAC4	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h
4Ch	GPIO Pin Configuration	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh~ 007Fh#
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h
52h	GPIO Pin Wake up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh
56h	Misc Modem AFE Status/Control	X	x	x	x	X	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	0000h
5Ah	Mixer Volume	X	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h
5Ch	Miscellaneous Audio	P3D	USEM	USEL	USER	CALM	CALL	CALR	DM	x	x	FAIM	FAIL	FAIR	DONM	DONL	DONR	00xxh
5Eh	Modem Control Register 1	LM21	LM20	SCM2	VM21	VM20	AM2	GM21	GM20	LM11	LM10	SCM1	VM11	VM10	AM1	GM11	GM10	0000h
60h	Modem Control Register 2	x	x	x	x	x	x	SQ2	SQ1	DH	DM2	DM1	LH1	LH0 6	SCH	VH1	VH0	0000h
78h	Rockwell Test Register	x	x	x	x	x	x	x	x	x	x	x	x	x	LMI2	LMI1	LIM0	0000h
7Ah	Rockwell Reserved	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	X
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5253h
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5312h~ 5306h#
bold: status inputs to AC-link ~: 80-pin package #: 64-pin package																		

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7.1 Register Definitions

7.1.1 Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code identifying supported functions and a code identifying the 3D Stereo Enhancement supplier.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	5573h

Bit	Label	R/W	Description
15			Reserved. Set to 0.
14:10	SE[4:0]	RO	3D Stereo Enhancement Vendor ID. Identifies the Rockwell 3D Stereo Enhancement (01001b).
9	ID9	RO	20-Bit ADC Supported Status. 0 = Not Supported.
8	ID8	RO	18-Bit ADC Supported Status. 1 = Supported.
7	ID7	RO	20-Bit DAC Supported Status. 0 = Not Supported.
6	ID6	RO	18-Bit DAC Supported Status. 1 = Supported.
5	ID5	RO	Loudness (Bass Boost) Supported Status. 1 = Supported.
4	ID4	RO	Headphone Out Supported Status. 1 = Supported.
3	ID3	RO	Simulated Stereo (Mono to Stereo) Supported Status. 0 = Not Supported.
2	ID2	RO	Bass and Treble Control Supported Status. 0 = Not Supported.
1	ID1	RO	Modem Line Codec Supported Status. 1 = Supported.
0	ID0	RO	Dedicated Mic PCM in Channel Supported Status. 1 = Supported.

7.1.2 Play Master Volume Registers (Index 02h)

This register controls the Play Master output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
02h	Play Master Volume	Mute	x	ML5	ML4	ML3	ML2	ML1	ML0	x	x	MR5	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description															
15	Mute	R/W	Master Volume Mute. 1 = The channel is muted (default). 0 = Channel volume is controlled by the ML[5:0] and MR[5:0] bits).															
14			Reserved.															
13	ML5	R/W	Left Master Volume Maximum Attenuation. 1 = Force ML[4:0] to all 1s. 0 = Do not force ML[4:0] to all 1s (channel volume controlled by ML[4:0] bits) .															
12:8	ML[4:0]	R/W	Left Master Volume Control Attenuation. This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. <table><tr><th>Mute</th><th>ML[5:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>00 0000</td><td>0 dB</td></tr><tr><td>0</td><td>01 1111</td><td>46.5 dB</td></tr><tr><td>0</td><td>1x xxxx</td><td>46.5 dB</td></tr><tr><td>1</td><td>xx xxxx</td><td>∞ dB</td></tr></table>	Mute	ML[5:0]	Attenuation	0	00 0000	0 dB	0	01 1111	46.5 dB	0	1x xxxx	46.5 dB	1	xx xxxx	∞ dB
Mute	ML[5:0]	Attenuation																
0	00 0000	0 dB																
0	01 1111	46.5 dB																
0	1x xxxx	46.5 dB																
1	xx xxxx	∞ dB																
7:6			Reserved.															
5	MR5	R/W	Right Master Volume Maximum Attenuation. 1 = Force MR[4:0] to all 1s. 0 = Do not force MR[4:0] to all 1s (channel volume controlled by MR[4:0] bits).															
4:0	MR[4:0]	R/W	Right Master Volume Control Attenuation. This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. <table><tr><th>Mute</th><th>MR[5:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>00 0000</td><td>0 dB</td></tr><tr><td>0</td><td>01 1111</td><td>46.5 dB</td></tr><tr><td>0</td><td>1x xxxx</td><td>46.5 dB</td></tr><tr><td>1</td><td>xx xxxx</td><td>∞ dB</td></tr></table>	Mute	MR[5:0]	Attenuation	0	00 0000	0 dB	0	01 1111	46.5 dB	0	1x xxxx	46.5 dB	1	xx xxxx	∞ dB
Mute	MR[5:0]	Attenuation																
0	00 0000	0 dB																
0	01 1111	46.5 dB																
0	1x xxxx	46.5 dB																
1	xx xxxx	∞ dB																

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7.1.3 Headphone Volume Register (Index 04h)

This register controls the Headphone output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
04h	Headphone Volume	Mute	x	ML5	ML4	ML3	ML2	ML1	ML0	x	x	MR5	MR4	MR3	MR2	MR1	MR0	8000h

Bit	Label	R/W	Description															
15	Mute	R/W	Headphone Master Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the ML[5:0] and MR[5:0] bits.															
14			Reserved.															
13	ML5	R/W	Headphone Left Master Volume Maximum Attenuation. 1 = Force ML[4:0] to all 1s. 0 = Do not force ML[4:0] to all 1s (channel volume controlled by ML[4:0] bits (default).															
12:8	ML[4:0]	R/W	Headphone Left Master Volume Control. This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. <table><tr><th>Mute</th><th>ML[5:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>00 0000</td><td>0 dB</td></tr><tr><td>0</td><td>01 1111</td><td>46.5 dB</td></tr><tr><td>0</td><td>1x xxxx</td><td>46.5 dB</td></tr><tr><td>1</td><td>xx xxxx</td><td>∞ dB (default).</td></tr></table>	Mute	ML[5:0]	Attenuation	0	00 0000	0 dB	0	01 1111	46.5 dB	0	1x xxxx	46.5 dB	1	xx xxxx	∞ dB (default).
Mute	ML[5:0]	Attenuation																
0	00 0000	0 dB																
0	01 1111	46.5 dB																
0	1x xxxx	46.5 dB																
1	xx xxxx	∞ dB (default).																
7:6			Reserved.															
5	MR5	R/W	Headphone Right Master Volume Maximum Attenuation. 1 = Force MR[4:0] to all 1s. 0 = Do not force MR[4:0] to all 1s (channel volume controlled by MR[4:0] bits (default).															
4:0	MR[4:0]	R/W	Headphone Right Master Volume Control. This field controls the channel attenuation from 0 dB to 46.5 dB in 1.5 dB steps. <table><tr><th>Mute</th><th>MR[5:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>00 0000</td><td>0 dB</td></tr><tr><td>0</td><td>01 1111</td><td>46.5 dB</td></tr><tr><td>0</td><td>1x xxxx</td><td>46.5 dB</td></tr><tr><td>1</td><td>xx xxxx</td><td>∞ dB (default).</td></tr></table>	Mute	MR[5:0]	Attenuation	0	00 0000	0 dB	0	01 1111	46.5 dB	0	1x xxxx	46.5 dB	1	xx xxxx	∞ dB (default).
Mute	MR[5:0]	Attenuation																
0	00 0000	0 dB																
0	01 1111	46.5 dB																
0	1x xxxx	46.5 dB																
1	xx xxxx	∞ dB (default).																

7.1.4 Mono Master Volume Register (Index 06h)

This register controls the Mono Master output Volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
06h	Mono Master Volume	Mute	x	x	x	x	x	x	x	x	x	MM5	MM4	MM3	MM2	MM1	MM0	8000h

Bit	Label	R/W	Description															
15	Mute	R/W	Mono Master Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the MM[5:0] bits.															
14:6			Reserved.															
5	MM5	R/W	Mono Master Volume Maximum Attenuation. 1 = Force MM[4:0] to all 1s. 0 = Do not force MM[4:0] to all 1s (channel volume controlled by MM[4:0] bits (default).															
4:0	MM[4:0]	R/W	Mono Master Volume Control. This field controls the Mono Master Volume Control output attenuation from 0 dB to -46.5 dB in 1.5 dB steps. <table><thead><tr><th>Mute</th><th>MMR[5:0]</th><th>Attenuation</th></tr></thead><tbody><tr><td>0</td><td>00 0000</td><td>0 dB</td></tr><tr><td>0</td><td>01 1111</td><td>46.5 dB</td></tr><tr><td>0</td><td>1x xxxx</td><td>46.5 dB</td></tr><tr><td>1</td><td>xx xxxx</td><td>∞ dB (default).</td></tr></tbody></table>	Mute	MMR[5:0]	Attenuation	0	00 0000	0 dB	0	01 1111	46.5 dB	0	1x xxxx	46.5 dB	1	xx xxxx	∞ dB (default).
Mute	MMR[5:0]	Attenuation																
0	00 0000	0 dB																
0	01 1111	46.5 dB																
0	1x xxxx	46.5 dB																
1	xx xxxx	∞ dB (default).																

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7.1.5 PC Beep Register (Index 0Ah)

This register controls the PC Beep input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Ah	PC Beep Volume	Mute	x	x	x	x	x	x	x	x	x	x	PV3	PV2	PV2	PV0	x	0000h

Bit	Label	R/W	Description												
15	Mute	R/W	PC Beep Volume Mute. 1 = The channel is muted. 0 = The channel volume is controlled by the PV[3:0] bits (default). Because the PC Beep signal input to the audio mixer is used primarily for system diagnostic purposes, the default value for the PC Beep Volume is unmuted.												
14:5			Reserved.												
4:1	PV[3:0]	R/W	PC Beep Volume Control. This field controls the PC Beep output attenuation from 0 dB to 46.5 dB in approximately 3 dB steps. <table><thead><tr><th>Mute</th><th>PV[3:0]</th><th>Attenuation</th></tr></thead><tbody><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>1111</td><td>45 dB</td></tr><tr><td>1</td><td>xxxx</td><td>∞ dB</td></tr></tbody></table>	Mute	PV[3:0]	Attenuation	0	0000	0 dB (default)	0	1111	45 dB	1	xxxx	∞ dB
Mute	PV[3:0]	Attenuation													
0	0000	0 dB (default)													
0	1111	45 dB													
1	xxxx	∞ dB													
0			Reserved.												

7.1.6 Mic Volume Register (Index 0Eh)

This register controls the Mic input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0Eh	Mic Volume	Mute	x	x	x	x	x	x	x	x	20dB	GN5	GN4	GN3	GN2	GN1	GN0	8008h

Bit	Label	R/W	Description															
15	Mute	R/W	Mic Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GN[5:0] bits.															
14:7			Reserved.															
6	20dB	R/W	Mic 20 dB Gain Enable. 1 = Enable the Mic 20 dB boost. 0 = Disable the Mic 20 dB boost (default).															
5	GN5	R/W	Mic Volume Maximum Gain. 1 = Force GL[4:0] to all 1s. 0 = Do not force GL[4:0] to all 1s (channel volume controlled by GL[4:0] bits (default).															
4:0	GN[4:0]	R/W	Mic Volume. This field controls the Mic volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><thead><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr></thead><tbody><tr><td>0</td><td>00000</td><td>+12 dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></tbody></table>	Mute	GL[4:0]	Gain	0	00000	+12 dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12 dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

7.1.7 Line In Volume Register (Index 10h)

This register controls the Line In input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
10h	Line In Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description															
15	Mute	R/W	Line In Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.															
14:13			Reserved.															
12:8	GL[4:0]	R/W	Left Line In Volume. This field controls the Left Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><thead><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr></thead><tbody><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></tbody></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																
7:5			Reserved.															
4:0	GR[4:0]	R/W	Right Line In Volume. This field controls the Right Line In volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><thead><tr><th>Mute</th><th>GR[4:0]</th><th>Gain</th></tr></thead><tbody><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></tbody></table>	Mute	GR[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GR[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

7.1.8 CD Volume Register (Index 12h)

This register controls the CD input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
12h	CD Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description															
15	Mute	R/W	CD Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.															
14:13			Reserved.															
12:8	GL[4:0]	R/W	Left CD Volume. This field controls the Left CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><thead><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr></thead><tbody><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></tbody></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																
7:5			Reserved.															
4:0	GR[4:0]	R/W	Right CD Volume. This field controls the Right CD Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><thead><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr></thead><tbody><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></tbody></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

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7.1.9 Video Volume Register (Index 14h)

This register controls the CD input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
14h	Video Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description															
15	Mute	R/W	Video Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.															
14:13			Reserved.															
12:8	GL[4:0]	R/W	Left Video Volume. This field controls the Left Video Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																
7:5			Reserved.															
4:0	GR[4:0]	R/W	Right Video Volume. This field controls the Right Video Volume from +12 dB to -34.5 dB in approximately 1.5 dB steps. The default value is 0 dB. <table><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

7.1.10 Aux Volume Register (Index 16h)

This register controls the Aux input volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
16h	Aux Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description															
15	Mute	R/W	Aux Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.															
14:13			Reserved.															
12:8	GL[4:0]	R/W	Left Aux Volume. This field controls the Left Aux Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																
7:5			Reserved.															
4:0	GR[4:0]	R/W	Right Aux Volume. This field controls the Right Aux Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GR[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GR[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GR[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

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7.1.11 PCM Out Volume Register (Index 18h)

This register controls the PCM Out output volume.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
18h	PCM Output Volume	Mute	x	x	GL4	GL3	GL2	GL1	GL0	x	x	x	GR4	GR3	GR2	GR1	GR0	8808h

Bit	Label	R/W	Description															
15	Mute	R/W	PCM Out Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the GL[4:0] and GR[4:0] bits.															
14:13			Reserved.															
12:8	GL[4:0]	R/W	Left PCM Out Volume. This field controls the Left PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GL[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GL[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																
7:5			Reserved.															
4:0	GR[4:0]	R/W	Right PCM Out Volume. This field controls the Right PCM Out Volume gain from +12 dB to -34.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GR[4:0]</th><th>Gain</th></tr><tr><td>0</td><td>00000</td><td>+12dB</td></tr><tr><td>0</td><td>01000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>11111</td><td>-34.5 dB</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GR[4:0]	Gain	0	00000	+12dB	0	01000	0 dB (default)	0	11111	-34.5 dB	1	xxxxx	−∞ dB
Mute	GR[4:0]	Gain																
0	00000	+12dB																
0	01000	0 dB (default)																
0	11111	-34.5 dB																
1	xxxxx	−∞ dB																

7.1.12 Record Select Register (Index 1Ah)

This register selects the record source.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ah	Record Select	X	x	x	x	x	SL2	SL1	SL0	x	x	x	x	x	SR2	SR1	SR0	0000h

Bit	Label	R/W	Description
15:11			Reserved.
10:8	SL[2:0]	R/W	Left Record Select. This field selects the record source for the left channel. SL[2] Left Record Source 0 Left Mic (default) 1 Left CD In 2 Left Video In 3 Left Aux In 4 Left Line In 5 Left Stereo Mix 6 Mono Mix 7 Reserved
7:3			Reserved.
2:0	SR[2:0]	R/W	Right Record Select. This field selects the record source for the right channel. SL[2] Right Record Source 0 Right Mic (default) 1 Right CD In 2 Right Video In 3 Right Aux In 4 Right Line In 5 Right Stereo Mix 6 Mono Mix 7 Reserved

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7.1.13 Record Gain Register (Index 1Ch)

This register controls the input record gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Ch	Record Gain	Mute	x	x	x	GL3	GL2	GL1	GL0	x	x	x	x	GR3	GR2	GR1	GR0	8000h

Bit	Label	R/W	Description												
15	Mute	R/W	Input Record Gain Mute. 1 = The channel is muted (default). 0 = Record gain is controlled by the GL[3:0] and GR[3:0] bits.												
14:12			Reserved.												
11:8	GL[3:0]	R/W	Left Input Record Gain. This field controls the Left Input Record gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GL[3:0]</th><th>Function</th></tr><tr><td>0</td><td>1111</td><td>+22.5 dB</td></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[3:0]	Function	0	1111	+22.5 dB	0	0000	0 dB (default)	1	xxxxx	−∞ dB
Mute	GL[3:0]	Function													
0	1111	+22.5 dB													
0	0000	0 dB (default)													
1	xxxxx	−∞ dB													
7:4			Reserved.												
3:0	GR[3:0]	R/W	Right Input Record Gain. This field controls the Right Input Record gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GR[3:0]</th><th>Gain</th></tr><tr><td>0</td><td>1111</td><td>+22.5 dB</td></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GR[3:0]	Gain	0	1111	+22.5 dB	0	0000	0 dB (default)	1	xxxxx	−∞ dB
Mute	GR[3:0]	Gain													
0	1111	+22.5 dB													
0	0000	0 dB (default)													
1	xxxxx	−∞ dB													

7.1.14 Record Gain Mic Register (Index 1Eh)

This register controls the input record gain mic.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
1Eh	Record Gain Mic	Mute	x	x	x	x	x	x	x	x	x	x	x	GM3	GM2	GM1	GM0	8000h

Bit	Label	R/W	Description												
15	Mute	R/W	Input Record Gain Mic Mute. 1 = The channel is muted (default). 0 = Record gain is controlled by the GL[3:0] and GR[3:0] bits.												
14:12			Reserved.												
11:8	GL[3:0]	R/W	Left Input Record Gain Mic. This field controls the Left Input Record Gain Mic from 0 dB to +22.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GL[3:0]</th><th>Function</th></tr><tr><td>0</td><td>1111</td><td>+22.5 dB</td></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GL[3:0]	Function	0	1111	+22.5 dB	0	0000	0 dB (default)	1	xxxxx	−∞ dB
Mute	GL[3:0]	Function													
0	1111	+22.5 dB													
0	0000	0 dB (default)													
1	xxxxx	−∞ dB													
7:4			Reserved.												
3:0	GR[3:0]	R/W	Right Input Record Gain Mic. This field controls the Right Input Record Gain Mic from 0 dB to +22.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>GR[3:0]</th><th>Gain</th></tr><tr><td>0</td><td>1111</td><td>+22.5 dB</td></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>1</td><td>xxxxx</td><td>−∞ dB</td></tr></table>	Mute	GR[3:0]	Gain	0	1111	+22.5 dB	0	0000	0 dB (default)	1	xxxxx	−∞ dB
Mute	GR[3:0]	Gain													
0	1111	+22.5 dB													
0	0000	0 dB (default)													
1	xxxxx	−∞ dB													

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7.1.15 General Purpose Register (Index 20h)

This register controls several miscellaneous functions of the AC '97 component. This register should be read before writing, to generate a mask for only the bit(s) that need to be changed. The function default value is 0000h which is all off.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
20h	General Purpose	POP	x	3D	LD	x	x	MIX	MS	LPBK	x	PCMS	x	x	x	x	x	0000h

Bit	Label	R/W	Description															
15	POP	R/W	PCM Output Path Select. This bit controls the optional PCM out 3D bypass path and Mute (the pre and post 3D PCM out paths are mutually exclusive). 1 = Post 3D. 0 = Pre 3D (default)															
14		R/W	Must be 0. Defaults to 0.															
13	3D	R/W	3D Stereo Enhancement On/Off Control. 1 = 3D Stereo Enhancement on. 0 = 3D Stereo Enhancement off (default).															
12	LD	R/W	Loudness (Bass Boost) On/Off Control. 1 = Bass boost on. 0 = Bass boost off (default).															
11:10			Reserved.															
9	MIX	R/W	Mono Output Select. 1 = Mic input 0 = Input Mixer output (default).															
8	MS	R/W	Microphone Input Select. 1 = Mic 2. 0 = Mic 1															
7	LPBK	R/W	ADC/DAC Loopback Mode Enable. 1 = Enable loopback of the stereo ADC output to the stereo DAC input (left-to-left, right-to-right) without involving the AC-link, allowing for full system performance measurements. 0 = Disable loopback (default).															
6			Reserved.															
5	PCMS	R/W	PCM Output Selection. 0 = result of bit 15; 1 = PCM DAC Out to no Mix, Main Analog Out = PCM Stereo. See Figure 7. <table><thead><tr><th>POP (Bit 15)</th><th>PCMS (Bit 5)</th><th>Description</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>Normal operation occurs, with the PCM stereo DAC output going into the audio mixer, going through the 3D/bass boost block (if enabled), and then out the speaker. This output can then be recorded if the record mux is selected properly.</td></tr><tr><td>1</td><td>0</td><td>The PCM stereo DAC output is summed after the 3D block. Again, the output can be record if the record mux is selected properly.</td></tr><tr><td>1</td><td>1</td><td>The PCM stereo DAC goes directly out to the speaker. What can be recorded is post 3D without the PCM stereo DAC.</td></tr><tr><td>0</td><td>1</td><td>The speaker, headphone, and mono output (if mic as input is not selected) are muted.</td></tr></tbody></table>	POP (Bit 15)	PCMS (Bit 5)	Description	0	0	Normal operation occurs, with the PCM stereo DAC output going into the audio mixer, going through the 3D/bass boost block (if enabled), and then out the speaker. This output can then be recorded if the record mux is selected properly.	1	0	The PCM stereo DAC output is summed after the 3D block. Again, the output can be record if the record mux is selected properly.	1	1	The PCM stereo DAC goes directly out to the speaker. What can be recorded is post 3D without the PCM stereo DAC.	0	1	The speaker, headphone, and mono output (if mic as input is not selected) are muted.
POP (Bit 15)	PCMS (Bit 5)	Description																
0	0	Normal operation occurs, with the PCM stereo DAC output going into the audio mixer, going through the 3D/bass boost block (if enabled), and then out the speaker. This output can then be recorded if the record mux is selected properly.																
1	0	The PCM stereo DAC output is summed after the 3D block. Again, the output can be record if the record mux is selected properly.																
1	1	The PCM stereo DAC goes directly out to the speaker. What can be recorded is post 3D without the PCM stereo DAC.																
0	1	The speaker, headphone, and mono output (if mic as input is not selected) are muted.																
4:0			Reserved.															

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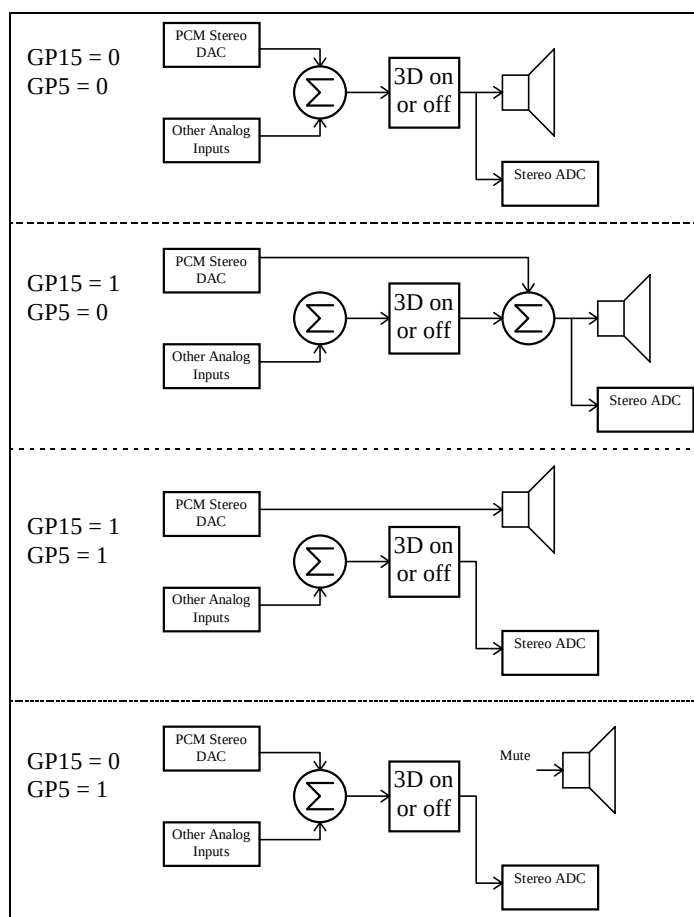


Figure 7. PCM Output Select: 3-Way Mux Options

7.1.16 3D Control Register (Index 22h)

This register controls the 3D Stereo Enhancement Gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
22h	3D Control	X	x	x	x	CR3	CR2	CR1	CR0	x	x	x	x	DP3	DP2	DP1	DP0	0300h

Bit	Label	R/W	Description										
15:12			Reserved.										
11:8	CR[3:0]	R/W	3D Stereo Enhancement Gain A. This field controls the 3D Stereo Enhancement Gain A from -32 dB, -12 dB to 9 dB in 1.5 dB steps. <table><tr><th>CR[3:0]</th><th>Gain</th></tr><tr><td>0000</td><td>-32 dB (default)</td></tr><tr><td>0001</td><td>-12 dB</td></tr><tr><td>....</td><td>....</td></tr><tr><td>1111</td><td>9 dB</td></tr></table>	CR[3:0]	Gain	0000	-32 dB (default)	0001	-12 dB			1111	9 dB
CR[3:0]	Gain												
0000	-32 dB (default)												
0001	-12 dB												
....													
1111	9 dB												
7:4			Reserved.										
3:0	DP[3:0]	R/W	3D Stereo Enhancement Gain B. This field controls the 3D Stereo Enhancement Gain B from -32 dB, -12 dB to 9 dB in 1.5 dB steps. <table><tr><th>DP[3:0]</th><th>Gain</th></tr><tr><td>0000</td><td>-32 dB (default)</td></tr><tr><td>0001</td><td>-12 dB</td></tr><tr><td>....</td><td>....</td></tr><tr><td>1111</td><td>9 dB</td></tr></table>	DP[3:0]	Gain	0000	-32 dB (default)	0001	-12 dB			1111	9 dB
DP[3:0]	Gain												
0000	-32 dB (default)												
0001	-12 dB												
....													
1111	9 dB												

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7.1.17 Power-Down Control/Status Register (Index 26h)

This register controls power-down states and monitors subsystem readiness. The lower four bits are read-only status with a “1” indicating that the subsection is “ready”. Ready indicates the subsection is able to perform in its nominal state. When this register is written, the bit values that come in on AC-link have no effect on read only bits 4-0.

When the AC-link “Codec Ready” indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AMC'97 control and status registers are in a fully operational state. The AMC '97 controller must further probe this Power-down Control/Status Register to determine exactly which subsections, if any, are ready.

PR0, PR1, and PR2 can be used individually rather than in combination with each other.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
26h	Power-down Control/Status	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	PRZ	PDM	PDA	x	REF	ANL	DAC	ADC	000xh

Bit	Label	R/W	Description
15	PR7	R/W	Power-down Modem DAC/ADC. Not supported. NOTE: Modem power-down control handled by Extended Modem Status and Control register (Index 3Eh).
14	PR6	R/W	Power-down Headphone Amplifier. 1 = Power-down Headphone Amplifier. 0 = Do not power-down Headphone Amplifier (default).
13	PR5	R/W	Power-down Internal Clock Circuit. 1 = Power-down internal clock circuit (crystal oscillator and all codec clocks). 0 = Do not power-down internal clock circuit (default).
12	PR4	R/W	Power-down Digital Interface. 1 = Power-down digital AC-link interface (external clock is off but oscillator circuit is on). 0 = Do not power-down digital AC-link interface (default).
11	PR3	R/W	Power-down Analog Mixer with Vref Off. PR3 can be used in combination with PR2 or by itself. 1 = Power-down Analog Mixer and turn Vref off. 0 = Do not power-down Analog Mixer (default).
10	PR2	R/W	Power-down Analog Mixer with Vref On. 1 = Power-down Analog Mixer but leave Vref on. 0 = Do not power-down Analog Mixer (default).
9	PR1	R/W	Power-down PCM Output DACs. 1 = Power-down PCM Output DACs. 0 = Do not power-down PCM Output DACs. (default).
8	PR0	R/W	Power-down PCM Input ADCs and Input Mux. 1 = Power-down PCM Input ADCs and Input Mux. 0 = Do not power-down PCM Input ADCs and Input Mux (default).
7	PRZ	R/W	Power-down Clock Interface Except BIT_CLK. 1 = Power-down Clock Interface except BIT_CLK output. This turns off all digital power to clock interface except BIT_CLK so the ASIC controller can monitor GPIOs. 0 = Do not power-down Clock Interface (default).
6	PDM	R/W	Power-down Mono Amplifier. 1 = Power-down Mono output amplifier. 0 = Do not power-down Mono output amplifier (default).
5	PDA	R/W	Power-down Line Out Amplifiers. 1 = Power-down stereo Line Out output amplifiers (left and right). 0 = Do not power-down stereo Line Out output amplifiers (default).
4	MDM	R	Modem Ready Status. Not supported, always 0 (default). NOTE: Modem status reported in Extended Modem Status and Control register (Index 3Eh).
3	REF	R	Audio Reference Voltages Ready Status. 1 = Audio reference voltages (Vrefs) ready (at nominal level). 0 = Audio reference voltages (Vrefs) not ready.
2	ANL	R	Analog Mixers Ready Status. 1 = Analog mixers, etc., ready. 0 = Analog mixers, etc., not ready.
1	DAC	R	DAC Ready Status. 1 = Stereo playback DAC ready to accept data. 0 = Stereo playback DAC not ready to accept data.
0	ADC	R	ADC Ready Status. 1 = Stereo record ADC ready to transmit data. 0 = Stereo record ADC not ready to transmit data.

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7.1.18 Extended Audio ID Register (Index 28h)

The read-only Extended Audio ID register identifies which extended audio features are supported (in addition to the original AC '97 features identified by reading the Reset register at Index 0h). A 1 indicates the extended audio feature is supported.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
28h	Extended Audio ID	ID1 0	ID0 0	x	x	x	x	x	LDAC 0	SDAC 0	CDAC 0	x	x	VRM 1	x	DRA 0	VRA 0	0008h

Bit	Label	R/W	Description
15:14	ID[1:0]	RO	Codec Configuration Identifier. This 2-bit field identifies the codec configuration. 00 = Primary configuration supported.
13:9			Reserved.
8	LDAC	RO	PCM LFE DAC Supported. 0 = Not supported.
7	SDAC	RO	PCM Surround DAC Supported. 0 = Not supported.
6	CDAC	RO	PCM Center DAC Supported. 0 = Not supported.
5:4			Reserved.
3	VRM	RO	Variable Rate Mic Supported. 1 = Supported.
2			Reserved.
1	DRA	RO	Double-Rate PCM Audio Supported. 0 = Not supported.
0	VRA	RO	Variable Rate PCM Audio Supported. 0 = Not supported.

7.1.19 Extended Audio Status and Control Register (Index 2Ah)

The Extended Audio Status and Control Register provides status and control of the extended audio features.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
2Ah	Extended Audio Status/Control	x	PRL	x	x	x	x	MADC	LDAC	SDAC	CDAC	x	x	VRM	x	DRA	VRA	4x00h

Bit	Label	R/W	Description
15			Reserved.
14	PRL	R/W	Power-down Mic ADC. 1 = Power-down the MIC ADC (MIC ADC operation is independent of PR0 in address 26h) 0 = Do not power-down the MIC ADC (default).
13:10			Reserved.
9	MADC	RO	Mic ADC Ready Status. 1 = Mic ADC is ready. 0 = Mic ADC is not ready.
8:4			Reserved.
8	LDAC	RO	PCM LFE DAC Supported. 0 = Not supported.
7	SDAC	RO	PCM Surround DAC Supported. 0 = Not supported.
6	CDAC	RO	PCM Center DAC Supported. 0 = Not supported.
5:4			Reserved.
3	VRM	R/W	Variable Rate Audio for Dedicated Mic Enable. 1 = Enables Variable Rate Audio mode for the dedicated Mic ADC. 0 = Disables Variable Rate Audio mode for the dedicated Mic ADC (default).
2			Reserved.
1	DRA	R/W	Double-Rate Audio Mode Enable. 0 = Not supported (default).
0	VRA	R/W	Variable Rate Audio Mode Enable. 0 = Not supported (default).

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7.1.20 MIC ADC Rate Control Registers (Index 34h)

This register controls the Mic ADC Sample rate.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
34h	MIC ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description																
15:0	SR[15:0]	R/W	Mic ADC Sample Rate. 16-bit unsigned value between 0 and 65535 as follows, representing the rate of operation in Hz: <table><tr><th>D[15-0] (hex)</th><th>Sample Rate (Hz)</th></tr><tr><td>1F40</td><td>8000</td></tr><tr><td>2580</td><td>9600</td></tr><tr><td>3592</td><td>13,714.28 (96000/7)</td></tr><tr><td>3E80</td><td>16000</td></tr><tr><td>4B00</td><td>19200</td></tr><tr><td>5DC0</td><td>24000</td></tr><tr><td>BB80</td><td>48000</td></tr></table>	D[15-0] (hex)	Sample Rate (Hz)	1F40	8000	2580	9600	3592	13,714.28 (96000/7)	3E80	16000	4B00	19200	5DC0	24000	BB80	48000
D[15-0] (hex)	Sample Rate (Hz)																		
1F40	8000																		
2580	9600																		
3592	13,714.28 (96000/7)																		
3E80	16000																		
4B00	19200																		
5DC0	24000																		
BB80	48000																		

7.1.21 Extended Modem ID Register (Index 3Ch)

The extended modem ID is a read/write register that primarily identifies the enhanced codec's modem AFE capabilities. The default value will depend on features and hardware configuration. Writing any value to this register performs a warm modem AFE reset (register range 3C-56h), including GPIO (register range 4C-54h). The warm reset causes all affected registers to revert to their default values. Note: for AMC '97 parts the audio and modem AFE should be logically independent (writes to register 0h resets audio only).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Ch	Extended Modem ID	ID1	ID0	x	x	x	x	x	x	x	x	x	x	x	HSET	LIN 2	LIN1	0007h~0005h#

Bit	Label	R/W	Description
15:14	ID[1:0]	R/W	Codec Configuration Identifier. This 2-bit field identifies the codec configuration: 00 = Primary 01 = Secondary 10 = Secondary 11 = Secondary
13:3			Reserved.
2	HSET	RO	Handset DAC Supported. 1 = Supported.
1	LIN2	RO	Line 2 Supported. 1 = Supported.
0	LIN1	RO	Line 1 Supported. 1 = Supported. NOTE: All modem functionality is controlled via the Extended AC '97 registers, i.e., the Modem Status and Control Register (Index 3Eh).

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7.1.22 Extended Modem Status and Control Register (Index 3Eh)

This register controls modem and handset power-down and reports modem and handset ready status. This register functions similarly to the Power-down Control/Status Register (Index 26h), however, bits MDM and PR7 in register 26h are not supported and replaced by extended functions in this register. Read/write bits 15-8 control modem subsystem power-down. Read-only bits 7-0 indicate modem subsystem readiness.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
3Eh	Extended Modem Status/Control	PRH	PRG	PRF	PRE	PRD	PRC	PRB	PRA	HDAC	HADC	DAC2	ADC2	DAC1	ADC1	MREF	GPIO	FFxh

Bit	Label	R/W	Description
15	PRH	R/W	Powerdown Handset DAC. 1 = Powerdown DAC (default). 0 = Do not powerdown DAC.
14	PRG	R/W	Powerdown Handset ADC. 1 = Powerdown ADC (default). 0 = Do not powerdown ADC.
13	PRF	R/W	Powerdown Modem Line 2 DAC. 1 = Powerdown DAC (default). 0 = Do not powerdown DAC.
12	PRE	R/W	Powerdown Modem Line 2 ADC. 1 = Powerdown ADC (default). 0 = Do not powerdown ADC.
11	PRD	R/W	Powerdown Modem Line 2 DAC. 1 = Powerdown DAC (default). 0 = Do not powerdown DAC.
10	PRC	R/W	Powerdown Modem Line 1 ADC. 1 = Powerdown ADC (default). 0 = Do not powerdown ADC.
9	PRB	R/W	Powerdown Modem Vref. 1 = Powerdown Modem Vref (default). 0 = Do not powerdown Modem Vref.
8	PRA	R/W	Powerdown GPIO. 1 = Powerdown GPIO (default). NOTE: When the GPIO section is powered down, all outputs are tri-stated and input slot 12 is marked invalid when the AC-link is active. 0 = Do not powerdown GPIO.
7	HDAC	R	Handset DAC Ready Status. 1 = Ready. 0 = Not ready (default).
6	HADC	R	Handset ADC Ready Status. 1 = Ready. 0 = Not ready (default).
5	DAC2	R	Modem Line 2 DAC Ready Status. 1 = Ready. 0 = Not ready (default).
4	ADC2	R	Modem Line 2 ADC Ready Status. 1 = Ready. 0 = Not ready (default).
3	DAC1	R	Modem Line 1 DAC Ready Status. 1 = Ready. 0 = Not ready (default).
2	ADC1	R	Modem Line 1 ADC Ready Status. 1 = Ready. 0 = Not ready (default).
1	MREF	R	Modem Reference Voltage (Vrefs) Ready Status. 1 = Ready. 0 = Not ready (default).
0	GPIO	R	GPIO Ready Status. 1 = Ready. 0 = Not ready (default).

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7.1.23 Modem Line 1 DAC/ADC Rate Control Register (Index 40h)

7.1.24 Modem Line 1 DAC/ADC Rate Control Register (Index 42h)

These registers control the sample rate the modem ADCs/DACs are using for sending/receiving samples to/from the controller.

A sample rate change will result in an unknown transient at both the analog output and the receive ADC input. The controller should mute the appropriate output, configure the codec as desired, wait for approximately TBD sample times, unmute the output, and then resume normal operation.

For modem AFE, each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. Any number written over BB80h will cause the sample rate to be 48 kHz. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) rate supported is returned.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
40h	Line 1 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
42h	Line 2 DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description																
15:0	SR[15:0]	R/W	Modem Line 1 or Line 2 DAC/ADC Sample Rate. 16-bit unsigned value between 0 and 65535 as follows representing the rate of operation in Hz: <table><tr><th>D[15-0] (hex)</th><th>Sample Rate (Hz)</th></tr><tr><td>1F40</td><td>8000</td></tr><tr><td>2580</td><td>9600</td></tr><tr><td>3592</td><td>13,714.28 (96000/7)</td></tr><tr><td>3E80</td><td>16000</td></tr><tr><td>4B00</td><td>19200</td></tr><tr><td>5DC0</td><td>24000</td></tr><tr><td>BB80</td><td>48000</td></tr></table>	D[15-0] (hex)	Sample Rate (Hz)	1F40	8000	2580	9600	3592	13,714.28 (96000/7)	3E80	16000	4B00	19200	5DC0	24000	BB80	48000
D[15-0] (hex)	Sample Rate (Hz)																		
1F40	8000																		
2580	9600																		
3592	13,714.28 (96000/7)																		
3E80	16000																		
4B00	19200																		
5DC0	24000																		
BB80	48000																		

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7.1.25 Modem Handset DAC/ADC Rate Control Register (Index 44h)

This register controls the sample rate the handset ADCs/DACs are using for sending/receiving samples to/from the controller.

A sample rate change will result in an unknown transient at both the analog output and the receive ADC input. The controller should mute the appropriate output, configure the codec as desired, wait for approximately TBD sample times, unmute the output, and then resume normal operation.

For modem AFE, each DAC/ADC pair is governed by a read/write modem sample rate control register that contains a 16-bit unsigned value between 0 and 65535, representing the rate of operation in Hz. Any number written over BB80h will cause the sample rate to be 48 kHz. For all rates, if the value written to the register is supported that value will be echoed back when read, otherwise the closest (higher in case of a tie) rate supported is returned.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
44h	Handset DAC/ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h

Bit	Label	R/W	Description																
15:0	SR[15:0]	R/W	Modem Handset DAC/ADC Sample Rate. 16-bit unsigned value between 0 and 65535 as follows representing the rate of operation in Hz: <table><tr><th>D[15-0] (hex)</th><th>Sample Rate (Hz)</th></tr><tr><td>1F40</td><td>8000</td></tr><tr><td>2580</td><td>9600</td></tr><tr><td>3592</td><td>13,714.28 (96000/7)</td></tr><tr><td>3E80</td><td>16000</td></tr><tr><td>4B00</td><td>19200</td></tr><tr><td>5DC0</td><td>24000</td></tr><tr><td>BB80</td><td>48000</td></tr></table>	D[15-0] (hex)	Sample Rate (Hz)	1F40	8000	2580	9600	3592	13,714.28 (96000/7)	3E80	16000	4B00	19200	5DC0	24000	BB80	48000
D[15-0] (hex)	Sample Rate (Hz)																		
1F40	8000																		
2580	9600																		
3592	13,714.28 (96000/7)																		
3E80	16000																		
4B00	19200																		
5DC0	24000																		
BB80	48000																		

7.1.26 Handset DAC/ADC Level Control Registers (Index 4Ah)

This register controls the handset output volume and mute when the handset is connected to TXA_H via relay control as well as the handset input volume and mute.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ah	Handset DAC/ADC level	Mute	x	x	DAC4	DAC3	DAC2	DAC1	DAC0	Mute	20dB	x	x	ADC3	ADC2	ADC1	ADC0	8080h

Bit	Label	R/W	Description												
15	Mute	R/W	Handset Output Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the DAC[4:0] bits.												
14:13			Reserved.												
12-8	DAC[4:0]	R/W	Handset Output Volume. This field controls the handset output attenuation from 0 dB to -46. dB. <table><tr><th>DAC[4:0]</th><th>Attenuation</th></tr><tr><td>00000</td><td>0 dB (default)</td></tr><tr><td>11111</td><td>46.5 dB</td></tr></table>	DAC[4:0]	Attenuation	00000	0 dB (default)	11111	46.5 dB						
DAC[4:0]	Attenuation														
00000	0 dB (default)														
11111	46.5 dB														
7	Mute	R/W	Handset Input Volume Mute. 1 = The channel is muted (default). 0 = The channel volume is controlled by the ADC[3:0] bits.												
6			Handset 20 dB Attenuation Enable. 1 = Enable 20 dB attenuation. 0 = Disable 20 dB attenuation (default).												
5:4			Reserved.												
3:0	ADC[3:0]	R/W	Handset Input Volume. This field controls the handset input gain from 0 dB to +22.5 dB in approximately 1.5 dB steps. <table><tr><th>Mute</th><th>ADC[3:0]</th><th>Gain</th></tr><tr><td>0</td><td>1111</td><td>+22.5 dB</td></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>1</td><td>xxxx</td><td>-∞ dB</td></tr></table>	Mute	ADC[3:0]	Gain	0	1111	+22.5 dB	0	0000	0 dB (default)	1	xxxx	-∞ dB
Mute	ADC[3:0]	Gain													
0	1111	+22.5 dB													
0	0000	0 dB (default)													
1	xxxx	-∞ dB													

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7.1.27 GPIO Pin Configuration Register (Index 4Ch)

The GPIO Pin Configuration is a read/write register that specifies whether a GPIO pin is configured for input (1) or for output (0), and is accessed via the standard slot 1 and 2 command address/data protocols.

On reset (Cold or Warm), all pins are configured as inputs. The status of all implemented GPIO pins will initially read back "1" (via Slot 12 or reg 54h), any unimplemented GPIO pins will always read back "0". This scheme informs software as to how many GPIO pins have been implemented. It is up to the AMC '97 digital controller to send the desired GPIO pin value over output slot 12 in the outgoing stream of the AC-link before configuring any of these bits for output.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Ch	GPIO Pin Configuration	GC15	GC14	GC13	GC12	GC11	GC10	GC9	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	FFFFh~007Fh#

7.1.28 GPIO Pin Polarity/Type Register (Index 4Eh)

The GPIO Pin Polarity/Type is a read/write register that defines GPIO Input Polarity (0=Low, 1=High active) when a GPIO pin is configured as an Input. It defines GPIO Output Type (0=CMOS, 1=OPEN-DRAIN) when a GPIO pin is configured as an Output.

On reset (Cold or Warm) this register defaults to all 1s. Unimplemented GPIO pins always return "1s".

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
4Eh	GPIO Pin Polarity/Type	GP15	GP14	GP13	GP12	GP11	GP10	GP9	GP8	GP7	GP6	GP5	GP4	GP3	GP2	GP1	GP0	FFFFh

7.1.29 GPIO Pin Sticky Register (Index 50h)

The GPIO Pin Sticky is a read/write register that defines GPIO Input Type (0=Not Sticky, 1=Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a "0" to the corresponding bit of the GPIO Pin Status register 54h (see below), and by reset.

On reset (Cold or Warm) this register defaults to all "0's" specifying Non-Sticky. Unimplemented

GPIO pins always return "0's". Sticky is defined as Edge sensitive, Non-Sticky as Level-sensitive.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
50h	GPIO Pin Sticky	GS15	GS14	GS13	GS12	GS11	GS10	GS9	GS8	GS7	GS6	GS5	GS4	GS3	GS2	GS1	GS0	0000h

7.1.30 GPIO Pin Wake up Mask Register (Index 52h)

The GPIO Pin Wake up is a read/write register that provides a mask for determining if an input GPIO change will generate a wake up or GPIO_INT (0=No, 1=Yes). When the AC-Link is powered down (Register 26h PR4 = 1 for Primary Codecs), a wake up event will trigger the assertion of SDATA_IN (the AC-Link wake up protocol is defined in Appendix C). When AC-link is powered up, a wake up event will appear as GPIO_INT=1 on bit 0 of input slot 12.

On reset (Cold or Warm) this register defaults to all "0's" specifying no wake up event. Unimplemented GPIO pins always returns "0's". An AC-Link wake up Interrupt is defined as a "0" to "1" transition on SDATA_IN when the AC-Link is Powered down (Register 26h PR4="1"). GPIO bits that have been programmed as Inputs, Sticky and Pin Wake up, upon transition either (high-to-low) or (low-to-high) depending on pin polarity, will cause an AC-Link wake up event (transition of SDATA_IN from "0" to "1"), if and only if the AC-Link was powered down.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
52h	GPIO Pin Wake up	GW15	GW14	GW13	GW12	GW11	GW10	GW9	GW8	GW7	GW6	GW5	GW4	GW3	GW2	GW1	GW0	0000h

7.1.31 GPIO Pin Status Register (Index 54h)

The GPIO Status is a read/write register that reflects the state of all GPIO pins (inputs and outputs) on slot 12. The value of all GPIO pin inputs and outputs comes in from the codec every frame on slot 12, but is also available for reading as GPIO Pin Status via the standard slot 1 and 2 command address/data protocols. GPIO inputs.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
54h	GPIO Pin Status	GI15	GI14	GI13	GI12	GI11	GI10	GI9	GI8	GI7	GI6	GI5	GI4	GI3	GI2	GI1	GI0	xxxxh

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7.1.32 Miscellaneous Modem Register (Index 56h)

This register defines the loop back modes available for the modem line ADCs/DACs, the handset ADCs/DACs, and the mic ADC. See section 6.6 for more information and a description of the modes. Note that the DAC outputs are squelched automatically when the loop back modes are used.

Also included are bits allowing squelch of the modem line outputs. The handset output has a volume control register already that includes a mute level selection.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
56h	Misc Modem AFE Status/Control	X	x	x	x	X	HSB2	HSB1	HSB0	x	L2B2	L2B1	L2B0	x	L1B2	L1B1	L1B0	0000h

Bit	Label	R/W	Description
15:11			Reserved.
10:8	HSB[2:0]	R/W	Handset loop back Enable. HSB[2:0] Function 000 = Disabled (default) 001 = ADC loop back 010 = Local Analog loop back 011 = DAC loop back 100 = Remote Analog loop back 101 = ADC and DAC loop back combined 110 = DAC one bit out 111 = SCF one bit in
7			Reserved.
6:4	L2B[2:0]	R/W	Modem Line 2 loop back Enable. L2B[2:0] Function 000 = Disabled (default) 001 = ADC loop back 010 = Local analog loop back 011 = DAC loop back 100 = Remote analog loop back 101 = ADC and DAC loop back combined 110 = DAC one bit out 111 = SCF one bit in
3			Reserved.
2:0	L1B[2:0]	R/W	Modem Line 1 Loop back Enable. L2B[2:0] Function 000 = Disabled (default) 001 = ADC Loop back 010 = Local analog loop back 011 = DAC Loop back 100 = Remote analog loop back 101 = ADC and DAC loopback combined 110 = DAC one bit out 111 = SCF one bit in

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7.1.33 Mixer Volume Register (Index 5Ah)

This register controls the attenuation on each of the signals coming into the main mixer so as to prevent clipping of the final signal. The step size is 1.5 dB and the range is 0 to -21.0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ah	Mixer Volume	X	x	x	x	MXL3	MXL2	MXL1	MXL0	x	x	x	x	MXR3	MXR2	MXR1	MXR0	0000h

Bit	Label	R/W	Description															
15:12			Reserved.															
11:8	MXL[3:0]	R/W	Left Mixer Volume Attenuation. This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. <table><tr><th>Mute</th><th>MXL[3:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>0001</td><td>1.5 dB</td></tr><tr><td>0</td><td>....</td><td>....</td></tr><tr><td>0</td><td>1110</td><td>21.0 dB</td></tr></table>	Mute	MXL[3:0]	Attenuation	0	0000	0 dB (default)	0	0001	1.5 dB	0			0	1110	21.0 dB
Mute	MXL[3:0]	Attenuation																
0	0000	0 dB (default)																
0	0001	1.5 dB																
0																		
0	1110	21.0 dB																
7:4			Reserved.															
3:0	MXR[3:0]	R/W	Right Mixer Volume Attenuation. This field controls the attenuation on each of the signals coming into the main mixer in 1.5 dB steps. <table><tr><th>Mute</th><th>MXR[3:0]</th><th>Attenuation</th></tr><tr><td>0</td><td>0000</td><td>0 dB (default)</td></tr><tr><td>0</td><td>0001</td><td>1.5 dB</td></tr><tr><td>0</td><td>....</td><td>....</td></tr><tr><td>0</td><td>1110</td><td>21.0 dB</td></tr></table>	Mute	MXR[3:0]	Attenuation	0	0000	0 dB (default)	0	0001	1.5 dB	0			0	1110	21.0 dB
Mute	MXR[3:0]	Attenuation																
0	0000	0 dB (default)																
0	0001	1.5 dB																
0																		
0	1110	21.0 dB																

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

7.1.34 Miscellaneous Audio Register (Index 5Ch)

This register allocates bits to control and provide status of the ADC DC offset calibration. It also has bits to enable dithering of the ADC output. All bits are defaulted 0.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Ch	Miscellaneous Audio	P3D	USEM	USEL	USER	CALM	CALL	CALR	DM	x	x	FAIM	FAIL	FAIR	DONM	DONL	DONR	00xxh

Bit	Label	R/W	Description
15	P3D	R/W	3D Block Power Down Control. 1 = Power-down 3D block. 0 = Do not power-down 3D block (default).
14	USEM	R/W	DC offset calibration use, dedicated mic ADC. 1 = Calibrate. 0 = Do not calibrate (default).
13	USEL	R/W	DC offset calibration use, left channel of audio ADC. 1 = Calibrate. 0 = Do not calibrate (default).
12	USER	R/W	DC offset calibration use, right channel of audio ADC. 1 = Calibrate. 0 = Do not calibrate (default).
11	CALM	R/W	DC offset calibration start, dedicated mic ADC. 1 = Calibrate. 0 = Do not calibrate (default).
10	CALL	R/W	DC offset calibration start, left channel of audio ADC. 1 = Calibrate. 0 = Do not calibrate.
9	CALR	R/W	DC offset calibration start, right channel of audio ADC. 1 = Calibrate. 0 = Do not calibrate.
8	DM	R/W	Dither enable for dedicated mic ADC. 1 = Enable dither 0 = Disable dither
5	FAIM	R	DC offset calibration fail, dedicated mic ADC. 1 = Calibration failed. 0 = Calibration did not failed (default).
4	FAIL	R	DC offset calibration fail, left channel of audio ADC. 1 = Calibration failed. 0 = Calibration did not failed (default).
3	FAIR	R	DC offset calibration fail, right channel of audio ADC. 1 = Calibration failed. 0 = Calibration did not failed (default).
2	DONM	R	DC offset calibration done, dedicated mic ADC. 1 = Calibration complete. 0 = Calibration not complete (default).
1	DONL	R	DC offset calibration done, left channel of audio ADC. 1 = Calibration complete. 0 = Calibration not complete (default).
7-6			Reserved.
0	DONR	R	DC offset calibration done, right channel of audio ADC. 1 = Calibration complete. 0 = Calibration not complete (default).

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

7.1.35 Modem Control Register 1 (Index 5Eh)

This register has several bits that perform required control functions for the modem line ADCs. The gain boosts provide performance improvements that are required for the K56 type modems.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
5Eh	Modem Control Register 1	LM21	LM20	SCM2	VM21	VM20	AM2	GM21	GM20	LM11	LM10	SCM1	VM11	VM10	AM1	GM11	GM10	0000h

Bit	Label	R/W	Description
15:14	LM[21:20]	R/W	Modem Line 2 TX Lowpass Filter Pole Location. LM[21:20] Location 00 = 8 kHz (default) 01 = 12 kHz 10 = 25 kHz 11 = 25 kHz
13	SCM2	R/W	Modem Line 2 TX SCF gain control 0 = 0 dB gain (default) 1 = 6 dB gain
12:11	VM[21:20]	R/W	Modem Line 2 DAC interpolator gain VM[21:20] Gain 00 = 0 dB (default) 01 = 6 dB 10 = 12 dB 11 = -6 dB
10	AM2	R/W	Modem Line 2 ADC LPF dB gain 0 = 0 dB (default) 1 = -4 dB
9:8	GM[21:20]	R/W	Modem Line 2 ADC gain boost GM[21:20] Gain 00 = 0 dB (default) 01 = 10 dB 10 = 15 dB 11 = 20 dB
7:6	LM[11:10]	R/W	Modem Line 1 TX Lowpass Filter Pole Location LM[11:10] Location 00 = 8 kHz (default) 01 = 12 kHz 10 = 25 kHz 11 = 25 kHz
5	SCM1	R/W	Modem Line 1 TX SCF gain control 0 = 0 dB gain (default) 1 = 6 dB gain
4:3	VM[11:10]	R/W	Modem Line 1 DAC interpolator gain VM[11:10] Gain 00 = 0 dB (default) 01 = 6 dB 10 = 12 dB 11 = -6 dB
2	AM1	R/W	Modem Line 1 ADC LPF dB gain 0 = 0 dB (default) 1 = -4 dB
1:0	GM[11:10]	R/W	Modem Line 1 ADC gain boost GM[11:10] Gain 00 = 0 dB (default) 01 = 10 dB 10 = 15 dB 11 = 20 dB

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

7.1.36 Modem Control Register 2 (Index 60h)

This register controls modem transmit squelch, handset and modem dither enable, handset transmit SCF gain, Handset lowpass filter pole location, and handset DAC interpolator gain.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
60h	Modem Control Register 2	x	x	x	x	x	x	SQ2	SQ1	DH	DM2	DM1	LH1	LH0	SCH	VH1	VH0	0000h

Bit	Label	R/W	Description
15:10			Reserved.
9	SQ2	R/W	Modem Line 2 TX Squelch. 1 = Squelch 0 = Do not squelch (default).
8	SQ1	R/W	Modem Line 1 TX Squelch. 1 = Squelch 0 = Do not squelch(default).
7	DH	R/W	Handset ADC Dither Enable. 1 = Enable dither 0 = Disable dither(default).
6	DM2	R/W	Modem Line 2 ADC Dither Enable. 1 = Enable dither 0 = Disable dither(default).
5	DM1	R/W	Modem Line 1 ADC Dither Enable. 1 = Enable dither 0 = Disable dither(default).
4:3	LH[1:0]	R/W	Handset TX Lowpass Filter Pole Location. LH[1:0] Location 00 = 8 kHz (default) 01 = 12 kHz 10 = 25 kHz 11 = 25 kHz
2	SCH	R/W	Handset TX SCF Gain Control 1 = 6 dB gain. 0 = 0 dB gain (default)
1:0	VH[1:0]	R/W	Handset DAC Interpolator Gain. VH[1:0] Gain 00 = 0 dB (default) 01 = 10 dB 10 = 15 dB 11 = 20 dB

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

7.1.37 Rockwell Test Register (Index 78h)

Register 78h is a Rockwell Test Register.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
78h	Rockwell Test Register	x	x	x	x	x	x	x	x	x	x	x	x	x	LMI2	LMI1	LIM0	0000h

Bit	Label	R/W	Description
15:3			Reserved.
2:0	LMI[2:0]	R/W	Dedicated Mic Loop Back Enable. LMI[2:0] Function 000 = Normal Operation (default) 001 = NA 010 = Local analog loop back with handset DAC 011 = DAC Loop back 100 = Remote analog loop back with handset DAC 101 = ADC and handset DAC loopback combined 110 = NA 111 = NA

7.1.38 Rockwell Reserved Register (Index 7Ah)

Register 7Ah is reserved for Rockwell.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ah	Rockwell Reserved	X	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	X

7.1.39 Vendor ID Registers 1 and 2 (Indexes 7Ch, 7Eh)

This register contains the vendor identification code and revision numbers.

The vendor identification code is reported in the F[7:0], S[7:0], and T[7:0] fields. The ID method is Microsoft's Plug and Play Vendor ID code.

The vendor revision number is reported in the REV[7:0] field.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	5253h

Bit	Label	R/W	Description
15:8	F[7:0]	R	Vendor ID Code Character 1. RSS ID code character 1: ASCII "R" (52h).
7:0	S[7:0]	R	Vendor ID Code Character 2. RSS ID code character 2: ASCII "S" (53h).

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	REV7	REV6	REV5	REV4	REV3	REV2	REV1	REV0	5312h~5306h#

Bit	Label	R/W	Description
15:8	T[7:0]	R	Vendor ID Code Character 3. RSS ID code character 3: ASCII "S" (53h).
7:0	REV[7:0]	R	Vendor Revision Number. RSS revision number (example): ASCII "6" (06h). The values in-between the large step sizes can be used for revision codes for device changes relative to the base family. REV[7:0] 0000 01XX 0001 00XX Description 64-pin codec 80-pin codec with full support for two modem lines.

8. Package Dimensions

The package dimensions are shown in Figure 2 (64 TQFP) and Figure 3 (80 PQFP).

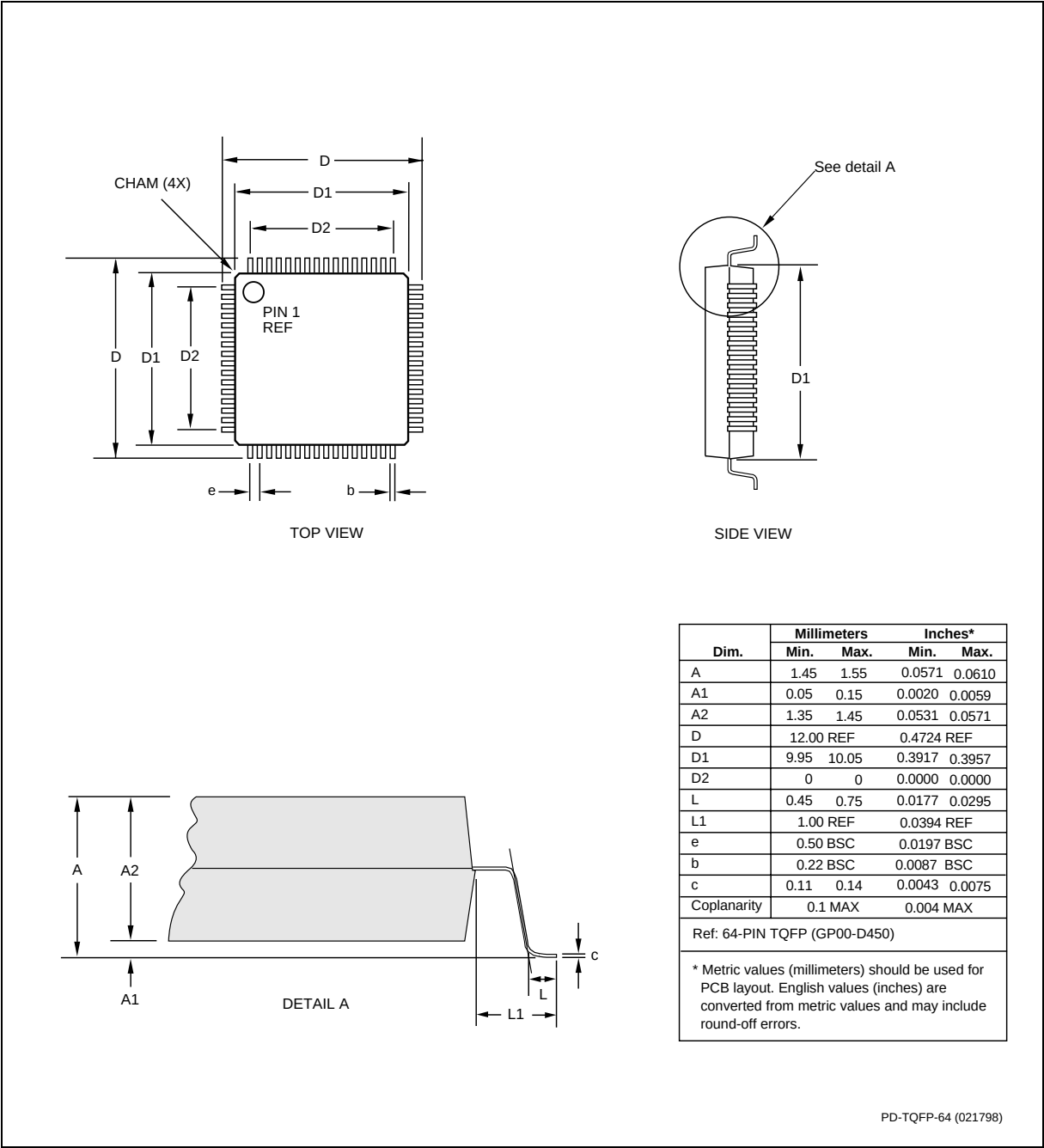


Figure 8. 64-Pin TQFP package dimensions

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

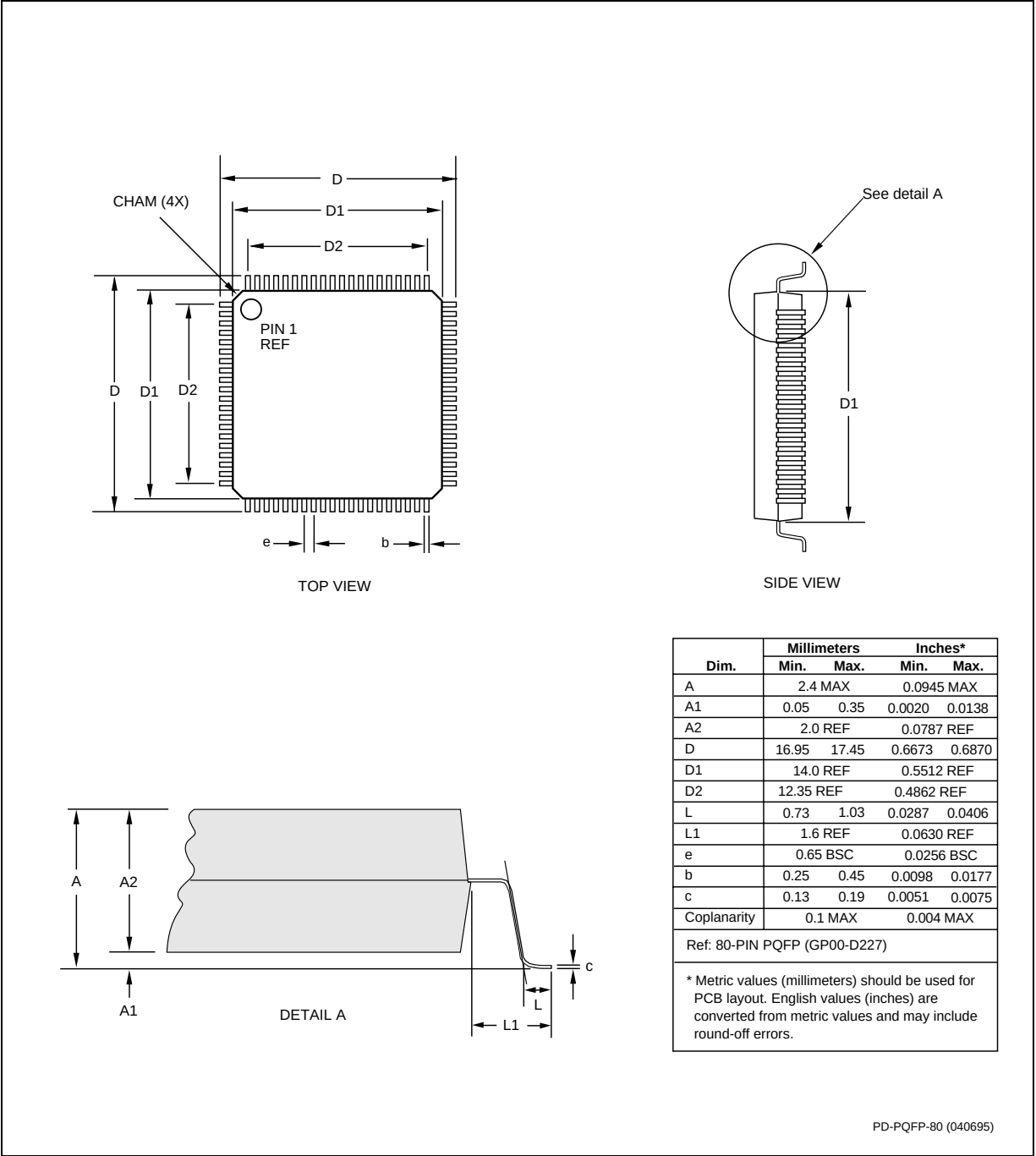


Figure 9. 80-Pin PQFP Package Dimensions

9. Application Connection Circuits

9.1 Typical Interface Connections and Supporting Components

Figure 10 shows typical codec interface connections in an application circuit with required supporting components. Recommended supporting components are described in Table 12.

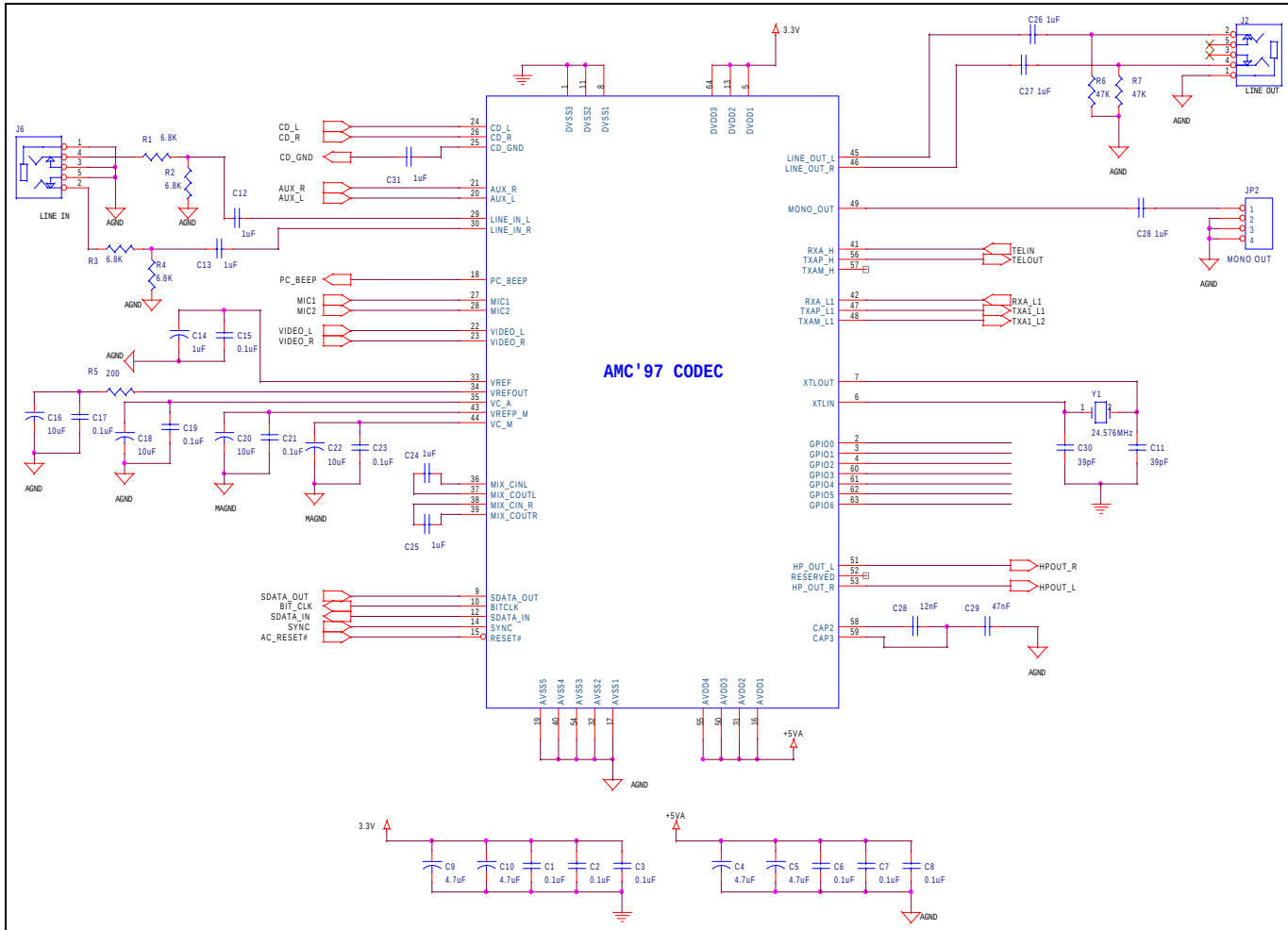


Figure 10. AMC Interface Recommended Supporting Components

RipTide AMC '97 Audio Modem Codec (AMC) Product Description

Table 12. R AMC Interface Recommended Supporting Components

Pin Name	Connection Description
VDD	Connect to VSS through 0.1 uF ceramic capacitors
AVDD	Connect to AVSS through 0.1 uF ceramic and 10 uF capacitors in parallel with each other. One pair for each AVDD.
XTALIN	39 pF to VSS
XTALOUT	39 pF to VSS
PC_BEEP	1 uF AC-coupling capacitor
AUX_L	1 uF AC-coupling capacitor
AUX_R	1 uF AC-coupling capacitor
VIDEO_L	1 uF AC-coupling capacitor
VIDEO_R	1 uF AC-coupling capacitor
CD_L	1 uF AC-coupling capacitor
CD_R	1 uF AC-coupling capacitor
MIC1	1 uF AC-coupling capacitor
MIC2	1 uF AC-coupling capacitor
LINE_IN_L	1 uF AC-coupling capacitor
LINE_IN_R	1 uF AC-coupling capacitor
VREF	10 uF Tantalum in parallel with 0.1 uF ceramic to AVSS
VREFOUT	200 ohm in series with 10 uF Tantalum in parallel with 0.1 uF ceramic to AVSS
VC_A	10 uF Tantalum in parallel with 0.1 uF ceramic to AVSS
MIX_CIN_L	1 uF ceramic to MIX_COUT_L
MIX_CIN_R	1 uF ceramic to MIX_COUT_R
VREFP_M	10 uF Tantalum in parallel with 0.1 uF ceramic to AVSS
VC_M	10 uF Tantalum in parallel with 0.1 uF ceramic to AVSS
LINE_OUT_L	1 uF AC-coupling capacitor. Also attach a 47 kohm resistor if the DC level is desired to be 0V
LINE_OUT_R	1 uF AC-coupling capacitor. Also attach a 47 kohm resistor if the DC level is desired to be 0V
MONO_OUT	1 uF AC-coupling capacitor. Also attach a 47 kohm resistor if the DC level is desired to be 0V
CAP2	12 nF between CAP2 and CAP3.
CAP3	47 nF to AVSS
CAP4	NC (80-pin PQFP only)
CAP5	NC (80-pin PQFP only)
CAP6	NC (80-pin PQFP only)

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