RC4011-IP

CMOS IEEE 1394 400 Mbps Analog Physical Layer Transceiver

Product Summary

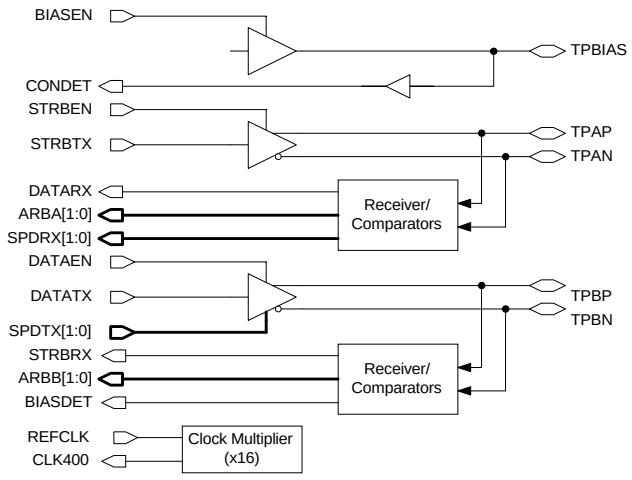
Description

The RC4011-IP is a fully verified CMOS core ready for integration into advanced communications products. It fully supports the IEEE 1394-1995 standard, including 1394a additions. The core interfaces directly to the cable's two twisted pairs (TPA/TPB) and includes TPBIAS generation, speed signaling generation and detection, arbitration, bias detection, cable power status, and connect detection. Also included is a fully monolithic clock multiplier, which generates a 400 MHz clock from a 25 MHz reference clock.

I/O Definition

Name	Type	Description
TPBIAS	Analog	Twisted Pair Bias Generator Output
TPAP, TPAN	Analog	Differential Twisted Pair A Interface
TPBP, TPBN	Analog	Differential Twisted Pair B Interface
STRBEN	Input	Enable TPA Driver
STRBTX	Input	Strobe to TPA Driver
DATARX	Output	Data from TPA Receiver
DATAEN	Input	Enable TPB Driver
DATATX	Input	Data to TPB Driver
STRBRX	Output	Strobe from TPB Receiver
ARBA[1:0]	Output	TPA Arbitration Comparator Output
ARBB[1:0]	Output	TPB Arbitration Comparator Output
SPDTX[1:0]	Input	Speed Signaling Control
SPDRX[1:0]	Output	Speed Signaling Comparator Output
BIASDET	Output	Cable Bias Voltage Comparator Output
CONDET	Output	Connect Detect Comparator Output
REFCLK	Input	25 MHz Reference Clock
CLK400	Input	400 MHz Clock Output
VDD/VSS	Power	Digital Supply/Ground
AVDD/AVSS	Power	Analog Supply/Ground

Block Diagram



Patent pending

Features

IEEE 1394 & 1394a Compatible
400 Mbps Data Rate
Integrated Bias Generator
Speed Signaling Generation and Detection
Bias and Connect Detection
Arbitration Comparators
Fully Monolithic Clock Multiplier
Power-Down Mode
+3.3V or +2.5V Operation
Low Power (<300mW Typical)
Fully Verified, Hard Core

Process Compatibility

0.35µ, 1P5M (3.3V)
0.25µ, 1P5M (2.5V)

Deliverables

Layout (GDS)
Abstract View
Netlist
Timing Model
Integration Support

Availability

3Q00

For More Information

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