RC2110-IP

CMOS Fibre Channel Transceiver With 10-Bit Interface

Product Summary

Applications

- Fibre Channel Host Adapters
- Switches, Hubs, and Routers
- High-Performance Serial Backplanes
- Proprietary Communication Links

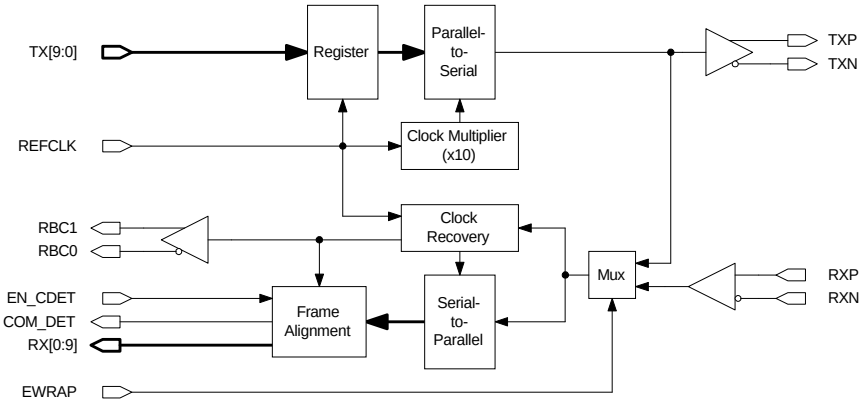
Description

The RC2110-IP is a fully verified, CMOS core ready for integration into advanced communications products. It supports high-speed, point-to-point, serial communications at over 1.0625 Gbps. The core is compatible with the ANSI X3T11 Fibre Channel physical layer specification. It accepts 10-bit parallel data referenced to the rising edge of the reference clock, and outputs the data serially at 10 times the reference clock frequency. The RC2110-IP recovers clock and data from differential serial input and outputs the data in parallel at 1/10th the input data rate. Word alignment is supported via Comma pattern (RD[0:9] = 0011111XXX) detection. The clock recovery is fully monolithic, requiring no external components.

I/O Definition

Name	Description
TD[0:9]	Parallel Transmit Data
TXP, TXN	Differential Serial Transmit Data Outputs
RXP, RXN	Differential Serial Receive Data Inputs
RD[0:9]	Parallel Receive Data Outputs
RBC	Recovered Byte Clock
EN_CDET	Comma Detection Enable
COM_DET	Comma Pattern (RD[0:9] = 0011111XXX) Detected
REFCLK	1.0625 MHz Reference Clock
VDD/VSS	Digital Supply/Ground
AVDD/AVSS	Analog Supply/Ground

Block Diagram



Patent pending

Features

Gigabit Ethernet Compatible
1.0625 Gbps Data Rate
Fully Monolithic Clock Multiplier and Recovery PLL's
10-Bit Parallel Interfaces
106.25 MHz Reference Clock
Loopback Mode
+3.3V or 2.5V Operation
Low Power (<300mW Typical)
Fully Verified, Hard Core

Process Compatibility

0.35µ, 1P5M (+3.3V)
0.25µ, 1P5M (+2.5V)

Deliverables

Layout (GDS)
Abstract View
Netlist
Timing Model
Integration Support

Availability

3Q00

For More Information

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