ROCKWELL SCIENTIFIC

RAD020

10 Bit 1 GS/s Analog-to-Digital Converter

Features

- 10-Bit Resolution
- Up to 1 GS/s Sampling Rate
- 1 Vpp Differential Full Scale Range
- 9 GHz Small-Signal Bandwidth
- 6 GHz Large-Signal Bandwidth
- < 100 fs Aperture Jitter
- DNL < 0.5 LSB
- INL < 1 LSB
- ENOB > 8 (DC to 1 GHz)
- SFDR > 60 dB (DC to 1 GHz)
- SNR > 55 dB
- LVDS-Compatible CML Output
- Binary/Offset Binary Code
- Over-Range Indicator
- 3 Clock Cycle Latency
- Track Mode Select for Static Test
- Decimation Clock Select

Applications

- Test Instrumentation Equipment
- Satellite Receivers
- Software Radio
- Radar
- Digital Receiver Systems
- Digital Sampling Oscilloscopes
- RF Demodulation Systems

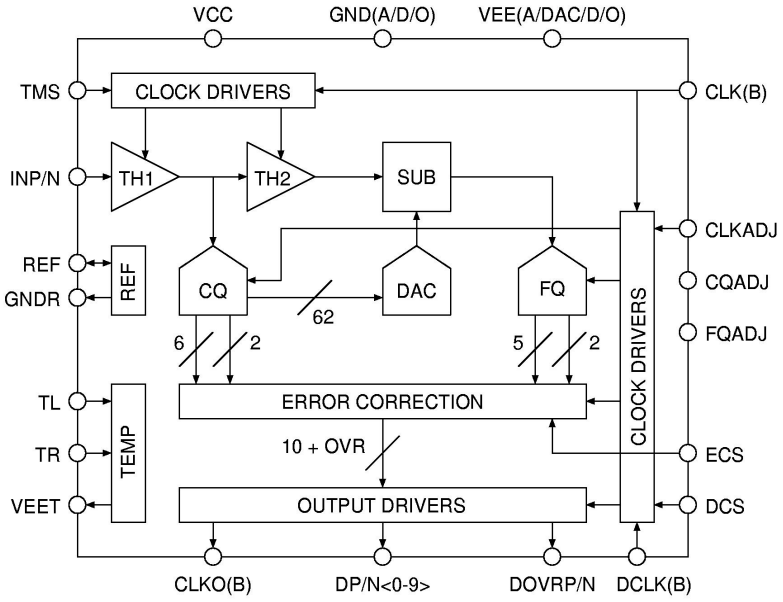

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Product Description

The RAD020 is a 10-bit analog-to-digital converter with an integrated track-and-hold amplifier sampling up to 1 GS/s. The monolithic circuit is fabricated in an 80-GHz f_T GaAs HBT process. Unprecedented bandwidth and aperture jitter performance allow direct conversion of signals with DC to multi-GHz carrier frequencies. Test modes include decimation of the output data to facilitate high-speed testing.

Absolute Maximum Ratings

Supply Voltages

Between GNDs ..... -0.3 to +0.3 V
Between VEEs ..... -0.3 to +0.3 V
VCC to GNDA ..... -1 V to +6 V
VCC to VEEA, VCC to VEEDAC ..... -1 V to +11 V
VEEA to GNDA, VEEDAC to GNDA ..... -6 V to +1 V
VEED to GNDD ..... -6 V to +1 V
VEEO to GNDO ..... -6 V to +1 V

RF Input Voltages

INP, INN to GNDA ..... -1 to +1 V
CLK, CLKB, DCLK, DCLKB to GNDD ..... -1 to +1 V

DC Analog Input Voltages

CLKADJ to GNDA ..... -4 to +2 V
OFFADJ, CQADJ, FQADJ to GNDA ..... -4 to +1 V
GNDR connects internally to GNDA and should not be connected externally except for biasing REF relative to GNDR
REF to GNDR .....-1.2 to 0 V
VEET connects internally to VEEDAC and should not be connected externally except for biasing TL and/or TR relative to VEET
TL to VEET, TR to VEET ..... –1.5 to +1.5 V

DC Digital Input Voltages

TMS to GNDA ..... -1.5 to +1 V
DCS, ECS to GNDD ..... -5 to +1 V

Digital Outputs

DP<0-9>, DN<0-9>, DOVRP, DOVRN, CLKO, CLKOB to GNDO ..... -2.5 to +3 V

Temperature

Operating Temperature ..... -30 to +70 °C
Case Temperature ..... -15 to +85 °C
Junction Temperature ..... +125 °C
Lead, Soldering (10 Seconds) ..... +220 °C
Storage ..... -40 to 125 °C

Electrical Specification (Static)

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
DC TRANSFER FUNCTION[1]							
Full Scale Range/|Vref|[2]	FSR		1		1.15	1.2	
Offset Voltage	VOS	OFFADJ Control Input Open	1			±7	mV
Resolution		Binary / Offset Binary	3	10		10	bits
Missing Codes			1			0	
Differential Nonlinearity	DNL	Maximum of Absolute Value	1		TBD		LSB
Integral Nonlinearity	INL	Maximum of Absolute Value	1		TBD		LSB
TEMPERATURE DRIFT							
Warm-up Time		After Power-up	2		30		s
Reference Drift	dVref/dT	After Warm-up	2		TBD		µV/°C
Full Scale Drift	dFSR/dT	After Warm-up	2		TBD		ppm/°C
Offset Voltage Drift	dVoff/dT	After Warm-up	2		TBD		µV/°C
ANALOG SIGNAL INPUTS, INP/N[3]							
Common Mode Voltage	V_{CM}		2	-100	0	100	mV
Common Mode Rejection Ratio	CMRR	Defined as $\partial VOS/\partial V_{CM}$	2		TBD		
Input Resistance		Each Lead to GNDA	2	46	50	54	Ω
Input Capacitance		Each Lead to GNDA	2	200	250	300	fF
CLOCK INPUTS, CLK(B), DCLK(B)[3]							
Amplitude[4]			2	200	600	1000	mVpp
Common Mode Voltage			2	-250	0	250	mV
Input Resistance		Each Lead to GNDD	2	46	50	54	Ω
Input Capacitance		Each Lead to GNDD	2	200	250	300	fF
REFERENCE, REF[5]							
Reference Voltage	Vref	REF Open	2		-1		V
Input Resistance			4		800		Ω
ANALOG DC INPUT, CLKADJ[5]							
CLKADJ High		No CQ Clock Advance	3	-0.5		1	V
CLKADJ Low		CQ Clock Advance, Open ≈ –3 V	3	-5.2	Open	-2.5	V
ANALOG DC INPUT, OFFADJ[5]							
Offset Adjust Ratio			4				mV/V
Input Resistance			4		3		kΩ
ANALOG DC INPUTS, CQADJ, FQADJ[5]							
Quantizer Scale Adjust Ratio	$(dFSR_Q/dV_{ADJ})/FSR_Q$	Q is CQ or FQ. Open Control ≈ -2.8 V	4		2.5		%/V
Input Resistance CQADJ			4		20.5		kΩ
Input Resistance			4		5.1		kΩ

[1] See Figure 2.
[2] Difference from unity is due to loss in the input T/H for 0.5 ns hold time. The loss increases for longer hold times, see Electrical Specification (Switching).
[3] See Figure 6.
[4] For > 500 MHz sinusoidal CLK(B), 500 to 700 mVpp (–2 to 1 dBm,pp) amplitude is recommended for combined aperture jitter and clock feed-through performance. At lower clock frequencies, use high amplitude for minimum jitter. See Theory of Operation.
[5] See Figure 7.

Electrical Specification (Static, Continued)

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
DIGITAL INPUT, TMS[6]							
High			3	-0.5	0	1	V
Low		Open ≈ –1.4 V	3	-1.5	Open	-1.2	V
Current Draw		Into Lead, High	3		0.75		mA
DIGITAL INPUTS, ECS, DCS							
High			3	-0.5	0	1	V
Low		Open ≈ –1.4 V	3	-5.2	Open	-1.2	V
Current Draw		Into Lead, High	3		0.25		mA
DIGITAL OUTPUTS, DP<0-9>, DN<0-9>, DOVR, DOVRB, CLKO, CLKOB							
Ext. Termination Ground	GNDOT	Relative to GNDO	3	-1	0	2	V
Ext. Termination Resistor[7]	Rterm	Required From Outputs To GNDOT	3		50	75	Ω
High		With Rterm To GNDOT	2		0		Vpp
Low		With 50 Ω Rterm To GNDOT	3		-0.4		V
Maximum Current		Into Lead	3		8		mA
POWER SUPPLY REQUIREMENTS							
GNDA Current	IGNDA	Into Device	2		244		mA
Positive Analog Supply Voltage	VCC	Relative to GNDA	1	4.75	5.0	5.25	V
VCC Current	ICC	Into Device	1		143		mA
Negative Analog Supply Voltage	VEEA	Relative to GNDA	1	-5.45	-5.2	-4.95	V
VEEA Current	IEEA	Out of Device	1		307		mA
DAC Supply Voltage	VEEDAC	Relative to GNDA	1	-5.45	-5.2	-4.95	V
VEEDAC Current	IEEDAC	Out of Device	1		71		mA
GNDD Current	IGNDD	Into Device	2		538		mA
Digital Supply Voltage	VEED	Relative to GNDD	1	-5.45	-5.2	TBD	V
VEED Current	IEED	Out of Device	1		549		mA
GNDO Current	IGNDO	Into Device	2		65		mA
GNDOT Current	IGNDOT	From GNDOT Into Device	2		90		mA
Output Supply Voltage	VEEO	Relative to GNDO	1	-5.45	-5.2	TBD	V
VEEO Current	IEEO	Out of Device	1		155		mA
Chip Power Dissipation	Pchip		1	TBD	6.0		W
Chip and Terminations Power Dissipation	Ptotal		1	TBD	6.35		W
Positive Analog Power Supply Rejection Ratio	$PSRR_{VCC}$	Defined as ∂VOS/∂VCC	2				dB
Negative Analog Power Supply Rejection Ratio	$PSRR_{VEEA}$	Defined as ∂VOS/∂VEEA	2				dB
DAC Power Supply Rejection Ratio	$PSRR_{VEEDAC}$	Defined as ∂VOS/∂VEEDAC	2				dB

[6] See Figure 8.
[7] Termination resistors should match the characteristic impedance of the data lines. The 50 Ω best matches to on-chip back-termination circuitry. Higher impedances may increase rise and fall times and diminish high-speed signal integrity.

Electrical Specification (Dynamic)

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT							
Bandwidth, Small Signal	bw	-3dB Gain, < -16 dBfs (< 0.1 Vpp)	2	8.5	9	9.5	GHz
Bandwidth, Half Signal		-3dB Gain, -6 dBfs	2	7.5	8	8.5	GHz
Bandwidth, Large Signal	BW	-3dB Gain, -0.5 dBfs	2	5.5	6	6.5	GHz
Gain Flatness Deviation		Maximum of Absolute Value, Before Final Gain Roll-Off	2			1	dB
Integrated Noise		Input Referred	4		550		μV
Noise Floor		Input Referred	4		5.3		nV/√ns
Signal-to-Noise Ratio	SNR		1				dB
-THD/SFDR 20 MHz		-0.5 dBfs	1				dB
-THD/SFDR 520 MHz		-0.5 dBfs	1				dB
-THD/SFDR 1020 MHz		-0.5 dBfs	1				dB
-THD/SFDR 1520 MHz		-0.5 dBfs	1				dB
-THD/SFDR 3020 MHz		-0.5 dBfs	1				dB
-THD/SFDR 5020 MHz		-0.5 dBfs	1				dB
-THD/SFDR 20 MHz		-6 dBfs	1				dB
-THD/SFDR 520 MHz		-6 dBfs	1				dB
-THD/SFDR 1020 MHz		-6 dBfs	1				dB
-THD/SFDR 1520 MHz		-6 dBfs	1				dB
-THD/SFDR 3020 MHz		-6 dBfs	1				dB
-THD/SFDR 5020 MHz		-6 dBfs	1				dB
-THD/SFDR 5020 MHz		-12 dBfs	2				dB
DYNAMIC TRACK MODE PERFORMANCE, SINEWAVE INPUT							
Track Bandwidth		-3dB Gain, TH1 & TH2 In Track Mode (TMS High)	2	800	1000	1200	MHz
Gain Flatness Deviation		Maximum of Absolute Value, Before Final Gain Roll-Off	2			0.5	dB
Integrated Noise		Input Referred	4		400		μV
Noise Floor		Input Referred	4		3.9		nV/√ns

Electrical Specification (Switching)

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
TRACK-TO-HOLD SWITCHING AND HOLD STATE, TH1							
Aperture Delay	ta	After V(CLK) - V(CLKB) Goes Neg.	4		+0.5		ns
Aperture Jitter	Δt	Jitter Free 1-GHz 0.5-Vpp CLK(B)[8,9]	3	70	100	130	fs
HOLD-TO-TRACK SWITCHING AND TRACK STATE, TH1							
Acquisition Time to 1 mV[10]	tacq	At Hold Caps, FSR Step At Input	4		250		ps
Maximum Acquisition Slew Rate[10]	dvdt,max	At Hold Caps, FSR Step At Input	4		15		V/ns
Rise Time[10]	tr	20 – 80%	3			50	ps
TRACK STATE AND HOLD STATE, TH1							
CLK Pulse Width High	tt	Track Time	3	TBD		TBD	MHz
CLK Pulse Width Low	th	Hold Time	3	TBD		TBD	MHz
Minimum CLK Freq.	fclk,min	50% Duty Cycle Clock	2	TBD		TBD	MHz
Maximum CLK Freq.	fclk,max	50% Duty Cycle Clock	2	TBD		TBD	MHz
Relative FSR Change per Time in Hold Mode	$(\partial FSR/\partial th)/FSR$	Gain Loss in TH1	4		0.56		%/ns
Recovery Time		Required Accumulated Track Time After fclk,min Violation	3			4	ns
DIGITAL OUTPUTS, DP<0-9>, DN<0-9>, DOVR, DOVRB, CLKO, CLKOB[11]							
Output Rise Time	tR	10 – 90%, Single-ended Into 50 Ω	2		120		ps
Output Fall Time	tF	10 – 90%, Single-ended Into 50 Ω	2		120		ps
Propagation Delay	tPD	CLK Neg. Edge to CLKO Neg. Edge	2				ps
Data Invalid Window	tinvalid	± tinvalid/2 Around CLKO Neg. Edge	2				ps
Latency			3		3		cycles

[8] The clock source jitter and the aperture jitter combine in an rms manner to yield the total sampling jitter. See Definition of Terms.
[9] Device aperture jitter increases as the V(CLK) – V(CLKB) slew rate at the zero crossing decreases. See Theory of Operation.
[10] TH1 tacq, dvdt,max, and tr also apply to the reconstructed ADC output if sub-sampling a fast-edge repetitive wave form.
[11] See Figure 3.

Test Levels

TEST LEVEL	TEST PROCEDURE
1	100% production tested at Ta = 25 C[1]
2	Sample tested at Ta = 25 C unless other temperature is specified[1]
3	Quaranteed by design and/or characterization testing
4	Typical value only

[1] All tests are continuous, not pulsed. Therefore, Tj (junction temperature) > Tc (case temperature) > Ta (ambient temperature). This is the normal operating condition and is more stressful than a pulsed test condition.

Pin Description

P/I/O	PIN	QTY	NAME	FUNCTION
P	1,6,7,89-96,110,119,122-126	18	GNDA	Analog Ground
P	2-4,12,13,117,118	7	VCC	Analog Positive Supply (+5 V)
P	8-10,97-102,111-116	15	VEEA	Analog Negative Supply (-5.2 V)
P	11,80,81	3	VEEDAC	DAC Negative Supply (-5.2 V)
P	16,19-21,24,67,70,82-88	14	GNDD	Digital Ground
P	14,15,25,65,66,73-79	12	VEED	Digital Supply (-5.2 V)
P	26-30,62-64	8	GNDO	Digital Output Ground
P	31,32,45,46,59-61	7	VEEO	Digital Supply (-5.2 V)
O	18	1	GNDR	Reference Ground
I/O	17	1	REF	Reference
O	103	1	VEET	Diode Reference Supply (-5.2 V)
I	105	1	TL	Diode Current Sense Pins. Measure and I-V point relative to VEET to monitor diode temperature. Diodes are transistor base-emitter junctions, and require about 1.4 V relative to VEET to conduct mA current levels. TL diode is located left of internal DAC, TR diode is located right of internal DAC.
I	104	1	TR	
I	106	1	CLKADJ	Coarse Quantizer Clock Phase Adjust
I	107	1	OFFADJ	ADC Offset Adjust
I	108	1	CQADJ	Coarse Quantizer Full Scale Adjust
I	109	1	FQADJ	Fine Quantizer Full Scale Adjust
I	5	1	TMS	Track Mode Select
I	72	1	ECS	Error Correction Select
I	71	1	DCS	Decimation Clock Select
I	121	1	INP	V(INP) – V(INN) Is Analog Input
I	120	1	INN	
I	69	1	CLK	V(CLK) – V(CLKB) Is Clock Input
I	68	1	CLKB	
I	57	1	DCLK	V(DCLK) – V(DCLKB) Is Decimation Clock Input
I	58	1	DCLKB	
O	35,37,39,41,43,47,49,51,53,55	10	DP<0-9>	Digital Bit i Output. Bit 9 is MSB, bit 0 is LSB.
O	36,38,40,42,44,48,50,52,54,56	10	DN<0-9>	Digital Bit i Complementary Output. Bit 9 is MSB, bit 0 is LSB.
O	33	1	DOVRP	Digital Overrange Output
O	34	1	DOVRN	Digital Overrange Complementary Output
O	22	1	CLKO	Output Clock
O	23	1	CLKOB	Output Clock Complement
P/I/O	All	126		

Definitions of Terms

Acquisition Time (tacq). The delay between the time that a track-and-hold circuit (TH) enters track mode and the time that the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from track to hold state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

If the underlying voltage noise mechanism of the sampling jitter has a white spectrum, the sampled signal will display a white noise floor as well. In this case, the required aperture jitter, Δt, to achieve a certain SNR, for a full-scale sinewave at frequency, f, is given by (B. Razavi, Principles of Data Conversion, IEEE Press, 1995, Appendix 2.1):

$$SNR\,(dB) = -20\log(2\pi f \Delta t)\ . \tag{1}$$

Using Eqs. (6, 7), allowable aperture jitter can be related to ENOB:

$$\Delta t \le \frac{1}{\sqrt{6}\pi 2^{ENOB} f}\ . \tag{2}$$

Note that this is independent of the sampling rate, so undersampling does not improve jitter tolerance. The averaging that is often combined with undersampling in test equipment, does improve jitter tolerance (and tolerance to other white noise effects).

The criterion above is sharper than the standard (incorrect) time-domain slope estimate by a factor $\sqrt{6}$. The reason is that n-bit quantization requires an rms error of (quantization step)/$\sqrt{12}$, which is considerably smaller than the quantization step error implicitly allowed in the usual time-domain estimates (another $\sqrt{2}$ comes from the energy of a sinewave relative to its amplitude squared).

The time-domain maximum slope argument can be appropiate for non-sinusoidal inputs, such as those encountered in instrumentation. If the rms error, ΔV, in the maximum slope region, slope FSR/(rise time), is used to define an effective number of bits, n, then the jitter simpy needs to fulfill:

$$\Delta t \le \frac{rise\ time}{2^n}\ . \tag{4}$$

Bin. See frequency bin.

Bit. Minimal unit of information, assuming one of two values commonly denoted as 0 (for low) and 1 (for high).

Clock Jitter. The standard deviation of the instants of the mid-point of the relevant (rising or falling) edge of the clock source relative to the ideal instants (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Code Width. The ADC input voltage interval that is mapped onto a given output code by the ADC transfer curve. In case of noise, the borders of the ith code width are those points at which it is equally likely that the output code is i or the bordering code, i – 1 or i + 1, assuming that the transfer curve is monotonic. The code width is not defined for the lowest and highest code.

Dynamic Nonlinearity (DNL). The deviation of any code width from one LSB. May also denote the maximum deviation for all codes.

Effective Number of Bits (ENOB). Resolution of an ideal ADC that would lead to the same SNDR as the measured SNDR of a non-ideal converter (includes distortion, quantization error, and noise). Equation (7) leads to the following relationship between SNDR and ENOB:

$$SNDR(dB) = 1.76 + 6.02\,ENOB\,. \tag{5}$$

Fast Fourier Transform (FFT). *NS*-point discrete fourier transform with *NS* an integer power of 2.

Frequency Bin. Index, 0, 1, 2, …, *NS* – 1, of *NS* frequency components in the FFT of a signal sampled at *NS* equidistant instants.

Full-Power Bandwidth. Input frequency at which the SNDR is reduced by 3 dB relative to its value at low frequencies (where the SNDR is approximately constant). This corresponds to an ENOB drop of 0.5 relative to its value at low frequencies.

Full Scale Range (FSR). Product of the number of ADC output codes and the LSB.

Gain, DC. Ratio of the digital full scale, or number of ADC output codes, and the FSR. This is equal to 1/LSB.

Gain. Ratio of the amplitude of the sine wave fit to the ADC output with frequency equal to the input frequency and the amplitude of the input sine wave. The first amplitude is easiest to determine from the magnitude of the first (main) harmonic (HD1) in the FFT spectrum of the digital output to the amplitude of the input.

Input Bandwidth (BW, bw). The input frequency at which the gain for sinewave inputs is reduced by 3 dB (factor $1/\sqrt{2}$) relative to its average value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs (small signal bandwidth, bw) and smallest for FSR inputs (large signal bandwidth, BW).

Integral Nonlinearity (INL). The deviation of any threshold from its ideal value given by the line fit used to determine the LSB.

Least Significant Bit (LSB). The average code width, which is the inverse slope of the linear fit to the *N* – 1 points, (ADC threshold *i*, *i* – 1/2), *i* = 1, …, *N* – 1, where *N* is the number of ADC codes. This assumes a monotonic ADC.

Offset, Offset Voltage (VOS). The input voltage, VOS, for which the point (VOS, *y*) lies on the linear fit to the *N* – 1 points, (ADC threshold *i*, *i* – 1/2), *i* = 1, …, *N* – 1, where *N* is the number of ADC codes, and *y* is equal to half the maximum code, i.e. ($2^{resolution}$ – 1) / 2.

Resolution. Number of ADC output bits.

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Signal-to-Noise Ratio (SNR). Ratio of the signal amplitude and the square root of the sum of the squares of all other FFT spectral components, excluding dc and harmonics 2, 3, …, *H*, the stop harmonic. SNR in dB is given by 20 $\log_{10}$ (SNR as amplitude ratio), and is generally positive. For amplitude ratios, we have:

$$\frac{1}{SNR^2} + THD^2 = \frac{1}{SNDR^2} \; . \tag{6}$$

Signal-to-Noise-and-Distortion Ratio (SNDR, SINAD). Ratio of the signal amplitude to the square root of the sum of all other FFT spectral components, excluding dc. SNDR in dB is given by 20 $\log_{10}$ (SNR as amplitude ratio), and is generally positive. For amplitude ratios, Eq. (6) holds.

Signal-to-Quantization Error Ratio (SQR). The SNDR of an ideal *n*-bit ADC, limited only by quantization error:

$$SNDR(ideal\ ADC, dB) = SQR(dB) = 10\log(3/2) + 20\log(2)\,n = 1.76 + 6.02\,n \; . \tag{7}$$

since the sine wave energy is $FSR^2/8$ and the quantization error energy is $LSB^2/12$.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or nonharmonic other tone, if present), as observed in the FFT spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20 $\log_{10}$ (SFDR as amplitude ratio), and is generally positive. For amplitude ratios, we have:

$$THD^2 \geq \frac{1}{SFDR^2} \; . \tag{8}$$

Stop Harmonic (*H*). Highest harmonic explicitly included in THD calculation and excluded from SNR calculation (relative to SNDR). Values of *H* between 5 and several percent of the total number of FFT frequency bins (normally larger than 1000) tend to very similar values. We use *H* = 24.

Threshold. Threshold *i* is the ADC input value for which code *i* - 1 and code *i* have equal probabilities of occurrence and these probabilities are larger than the probability of any other code. This covers the case of noise in the output code (it changes over time, even if the ADC input is constant), but assumes that the ADC (average) output is monotonically increasing versus input and that there are no missing codes. If code *i* is missing (zero code width), define both threshold *i* and threshold *i*+1 to be equal to the ADC input value at which the codes *i* – 1 and *i* + 1 are equally likely, etc. If an end code is missing, the effective output range of the ADC is reduced; we will not consider this case here. For a non-monotonic ADC, the this threshold definition extends in a natural manner.

Total Harmonic Distortion (THD). Ratio of the square root of the sum of the harmonics 2, 3, …, *H*, the stop harmonic, to the signal amplitude in the FFT spectrum. THD in dB is given by 20 $\log_{10}$ (THD as amplitude ratio), and is generally negative. For amplitude ratios, Eqs. (6, 8) hold.

Transfer Curve. The straight segment curve connecting the points (threshold 1, start code of threshold 1), (threshold 1, end code of threshold 1), (threshold 2, start code of threshold 2), (threshold 2, end code of threshold 2), … . If the ADC is monotonic and has no missing end codes, $N - 1$ thresholds are defined and the transfer curve connects the points (threshold 1, code 0), (threshold 1, code 1), (threshold 2, code 1), (threshold 2, code 2), …, (threshold $N - 1$, code $N - 2$), (threshold $N - 1$, code $N - 1$).

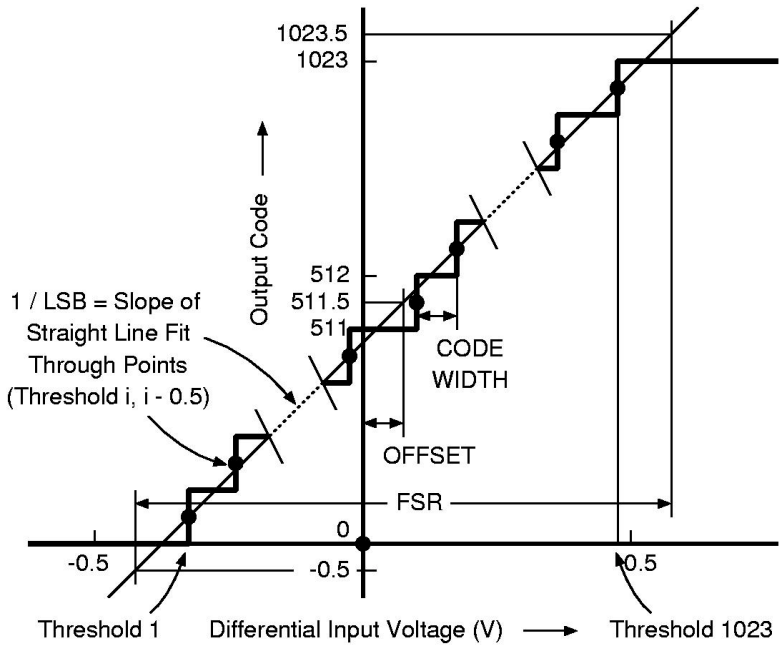

Figure 2. Transfer curve and related concepts for a 10-bit ADC with approximately 1 Vpp full scale range (FSR). Vertical axis is offset two's complement decimal code. Non-integer codes are not output by the ADC but define the offset and FSR.

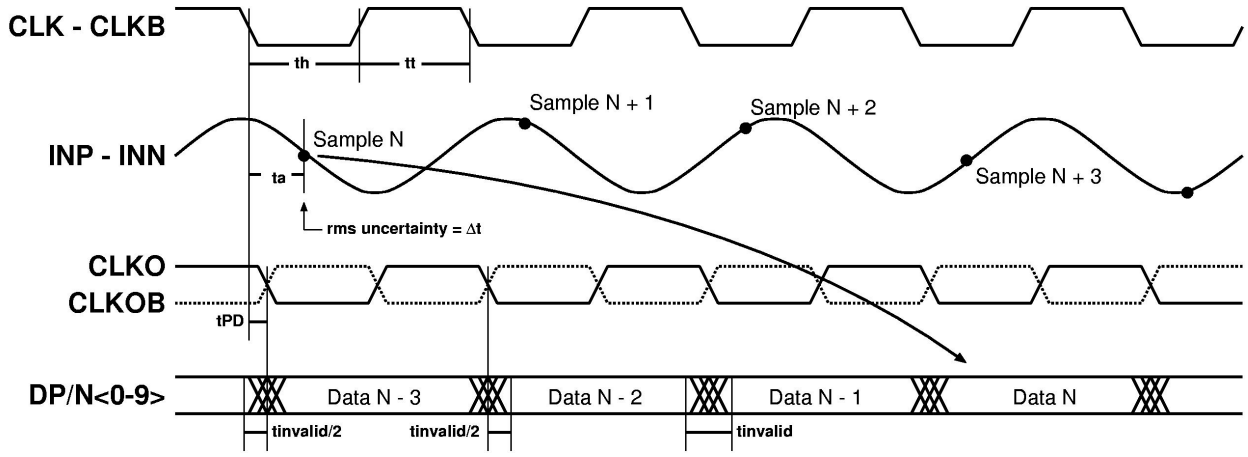

Figure 3. Timing diagram for RAD020.

Theory of Operation

The ADC chip is a monolithic circuit fabricated in an 80-GHz fT GaAs HBT process. It uses a high performance input track-and-hold circuit (TH1) followed by a two-step pipeline with a 6-bit coarse quantizer (CQ) and a 5-bit fine quantizer (FQ), see Figure 1. The CQ provides a 6-bit estimate of the input signal. This estimate is converted back to an analog signal, or reconstructed, by a digital-to-analog converter, DAC. A second track-and-hold, TH2 delays the TH1 output by half a clock cycle so it aligns in time with the DAC output. A subtract circuit, SUB, subtracts the coarse signal estimate from the held output of TH2 (a copy of the input signal). The resulting residue signal is converted by the 5-bit FQ. An error correction circuit takes CQ and FQ digital outputs, aligns them in time, and produces a 10-bit data word and an overrange bit. These signals are re-timed again and output in 50-Ω CML style. The re-timing clock is also output as a data strobe. To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential.

Input Track-and-Hold and Clock Driver

The input track-and-hold, TH1 (Figure 1), determines the dynamic performance of the ADC. Its sampling bridges exploit the ultrahigh speed Schottky diodes available in the GaAs HBT process. The TH1 clock is derived from the differential ADC clock inputs, CLK and CLKB, which should be driven by a low-jitter clock source.

The ADC receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of the differential clock voltage V(CLK) – V(CLKB), after an aperture delay, ta, see Figure 3. TH1's aperture delay is positive, nominally 0.5 ns.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise). TH1 and its clock driver are designed for low jitter by using extra large low noise devices in the clock signal path. From the Definition of Terms, the required total sampling jitter for sampling a 1-GHz 1-Vpp sine wave with 10-bit accuracy is 127 fs. The aperture jitter of the RAD020 is less than 100 fs for a 1-GHz 0.5-Vpp ADC clock, CLK(B). Using rms addition of jitter, the clock source jitter must be less than 80 fs (over the measurement record time) for direct 10-bit sampling of GHz range signals. Given a noise variance, ΔV, of the on-chip clock buffer, its aperture jitter, Δt, is inversely proportional to the clock buffer gain and the slew rate of the incoming clock at the zero-crossing point:

$$\Delta t = \frac{\Delta V}{gain \times slew\,rate}\ . \tag{9}$$

For low slew rates or frequencies, the clock buffer gain is constant and its aperture jitter is inversely proportional to the input clock slew rate, improving with increasing slew rate. For high slew rates or high frequencies, the jitter increases again, because the buffer gain drops steeply. For the RAD020, the clock buffer gain is still roughly constant up to 1 GHz, so that the aperture jitter is inversely proportional with the slew rate of the incoming clock. In the above equation, we have $\Delta V/gain \approx 0.15$ mV. The RAD020 aperture jitter at various slew rates can then be estimated. For example, a 1-GHz 0.5-Vpp sinusoidal CLK(B) signal corresponds to a slew rate ~ 1.6 V/ns, correctly yielding an aperture jitter < 100 fs.

TH1 hold mode feedthrough, or in-to-out hold-mode gain in dB, is critical, since any distortion on the held TH1 signal by a rapidly varying TH1 input will be sampled by subsequent ADC circuitry, and can not be removed. RAD020's TH1 hold mode feedthrough performance is more than sufficient for 10-bit sampling of GHz range signals.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold and track times (th and tt). For longer hold times, the ADC must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode.

Interstage Track-and-Hold and Clock Driver

The interstage track-and-hold, TH2 (Figure 1), is designed to have unity gain to facilitate gain matching of the two pipeline quantizer stages. It uses low distortion Schottky diode bridges. Its output buffer drives the subtract circuit, SUB. Since TH2 samples a held signal, its clock jitter is irrelevant and the TH2 clock driver is optimized for low power and proper drive.

Quantizers

The coarse and fine quantizers are flash style ADCs. They employ interpolation, resistive averaging, and layout techniques that optimize bandwidth and linearity. Special circuitry for high-speed encoding and low comparator hysteresis is included.

Digital-to-Analog Converter and Subtract Circuit

A high-speed current-mode unary DAC reconstructs the CQ output. Special attention is paid to matching of the DAC current sources and the DAC output settling time. The DAC and TH2 outputs interface with a unique high-bandwidth subtract circuit that forms a residue signal driving the FQ.

Error Correction

The ADC uses extra range of the FQ to correct the estimate of the CQ up to ±1/2 a CQ LSB. The ADC architecture is such that the error correction circuit simply adds the FQ MSB (0 or 1) as an LSB to the CQ binary code with a minimum number of gate delays. The four FQ LSBs are unaffected by the circuit. This block also constructs the ADC over-range bit, DOVR(B), from CQ and FQ under- and over-flow signals. The digital circuitry uses differential CML and ECL gates to minimize coupling to analog sections of the ADC.

Output Drivers

The output drivers are differential CML style drivers (Figure 8) preceded by master-slave latches. The output clock signal path delay is designed to be similar to the data path delay, and tracks over temperature. All outputs are differential and use two pads to minimize single-ended coupling to analog sections of the ADC.

Signal Descriptions

Analog Input

The RAD020 analog signal inputs are terminated on-chip with 50 Ω to GNDA, see Figure 6. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is ±1 V, at 20 mA current. The RAD020 is designed for 1-Vpp differential analog input signals (±0.25 V signals at each input), and can accept common-mode offsets up to ±100 mV. If operated in single-ended mode, terminate the complementary input off-chip with 50 Ω to the same common mode as the driven input. The single-ended FSR is half that of the differential FSR. Distortion in the single-ended mode can be up to 6 dB higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on the ADC output.

Clock Signals

All four clock input signals are terminated on-chip with 50 Ω to GNDD, see Figure 6. For lowest clock source jitter, use a sinusoidal clock source for CLK(B). Use differential clock signals for optimal performance. Large CLK(B) amplitude benefits aperture jitter performance, small CLK(B) amplitude minimizes distortion due to clock feed-through in the higher clock frequency range (500 to 1000 MHz). Independent of the clock waveform, clock slew rates < 2 V/ns are recommended to minimize clock feed-through related distortion. In case of single-ended clocking the complementary input(s) can be terminated directly to GNDD (lowest noise, clock waveform distortion is not critical). Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

Reference Circuit

The ADC FSR is controlled by the REF pin voltage, which is nominally close to –1 V. The ADC quantizing section after TH1 has a FSR equal to –VREF. Due to TH1 gain loss, the ADC FSR is typically larger than this value by a factor 1.15. Since TH1 gain loss increases with TH1 hold time, the ADC FSR increases proportionally.

An internal circuit sets REF to approximately –1 V (Figure 4). An external reference can be used to override this value for more accurate ADC FSR control. This reference is to be connected between GNDR and REF. The GNDR is internally connected to the analog ground, GNDA, but conducts no current, except the reference circuit current (Kelvin probe).

Figure TBD

Figure 4. Equivalent reference circuit.

Coarse Quantizer Clock Phase Adjustment

The CLKADJ input is an analog control that is left open by default. Its value affects the clock phase of the CQ and can be adjusted to trade off CQ comparator amplify time versus regeneration time. This trade-off affects ADC accuracy and metastability at high speeds.

Offset Adjustment

The OFFADJ input may be used to correct ADC offset error, VOS. See Figure 10.

Gain Matching

The ADC is designed to operate without foreground calibration and does not require external operational amplifiers. The coarse and fine quantizer scale fine adjust controls, CQADJ and FQADJ, may be used to optimize ADC linearity.

Low Frequency Test Mode

One digital input, Track Mode Select (TMS), is provided to put both TH1 and TH2 in track mode, independent of the clock signal. The ADC bandwidth is substantially lower in this mode than in the sampled mode. The TMS is useful for low sample-rate operation, including DC testing. It allows testing at clock frequencies below the minimum clock frequency of the ADC in sampled mode. TMS can simply be left open for the (default) sampled-mode operation of the RAD020. Grounding the TMS puts the track-and-holds in track-mode. In this state, the TMS draws up to 0.75 mA of current.

Decimation Mode

The RAD020 offers a decimated output mode, which is selected through the DCS input. In this mode, the data output rate is equal to the frequency of the decimation clock, to be provided by the user at inputs DCLK and DCLKB. An external variable delay may be required to properly align this clock signal with the ADC master clock. The decimation clock frequency must be equal to the master clock frequency divided by an integer, say *ND*, so only every *ND*-th internal ADC data word is output.

Testing in decimation mode affects details of FFT processing of the ADC output. Let the record length used for subsequent FFT processing of the decimated data be *NS* (number of samples). The number of ADC master clock periods that elapse during this record is *ND* x *NS*. The number of nonequivalent sampling points is *NS* / GCD(*ND*,*NS*), since GCD(*ND*,*NS*) (greatest common divisor) is the number of times that an equivalent point (same phase) of the input wave will be sampled. To sample only nonequivalent points (as in non-decimated testing), choose GCD(*ND*,*NS*) = 1, i.e. *ND* and *NS* are relatively prime. Since *NS* is a power of 2 for the FFT algorithm, this is equivalent to choosing *ND* odd. Proper input frequencies to avoid windowing effects and ensure that harmonics do not “fall on top of each other” (until the *NS*-th harmonic) are then given by (*n* x fclk) / (*ND* x *NS*), with *n* relatively prime to *ND* x *NS*.

The effect of sampling equivalent input sine wave points is not very obvious in the FFT spectrum if the ADC is random noise limited. If one discards some LSB’s, the ADC acts as a deterministic (lower resolution) ADC and the effects of equivalent point sampling become apparent: the FFT spectrum contains nonzero amplitudes only in every *NE*-th bin, where *NE* is the number of equivalent points sampled. To optimally test the ADC, whether noise limited or not, one should ensure that *NE* =1.

Figure TBD

Figure 5. Timing diagram for RAD020 in decimation mode.

Error Correction Off Mode

An error correction select, ECS, is provided to enable/disable the error correction circuit. The default open mode of the ECS pin enables error correction, which is critical to normal ADC operation. Grounding the ECS disables the error correction circuit. In this mode, the 6 coarse quantizer (CQ) bits are not changed by the fine quantizer (FQ) MSB (as if the FQ MSB is 0, see Theory of Operation). This mode is useful to test CQ operation.

Digital Outputs

The digital outputs are 12 differential current-mode logic (CML) signals: output clock for data strobing, CLKO(B), data word, DP/N<0-9> (MSB is DP/N<9>), and overrange bit, DOVRP/N. CML is a power efficient and highly noise-immune interface for high-speed differential signaling. The equivalent circuit of one differential CML output driver is shown in Figure 8. Two external 50-Ω termination resistors to the termination voltage, GNDOT (which is referenced to GNDO and is normally simply connected to GNDO) result in low and high levels of –0.4 V and 0 V (relative to GNDOT). Therefore, the differential output voltage is ±0.4 V.

One may also use 75-Ω lines and 75-Ω termination resistors to GNDOT. In this case the differential swing increases to ±0.6 V, but the rise and fall times, tR and tF, will increase slightly.

Differential CML interfaces easily to LVDS. The 50-Ω transmission lines from the chip to an LVDS input buffer are already AC terminated correctly by the 100-Ω differential LVDS termination resistor. To provide a DC termination, from which the approximately 8 mA of the chip output buffer will flow to VEEO (Figure 8), use two relatively large resistors to a positive supply. For instance, 1-kΩ resistors from each line to 5 V set the common mode of the outputs at 1 V. These resistors are best placed close to the chip pads, so the transmission lines still terminate differentially into 100 Ω. The large resistors actually affect the back termination of the line in a positive manner. If the large resistors are placed close to the LVDS input buffer, then the effective differential input impedance is 100 Ω in parallel with 2 kΩ, which is still close to 100 Ω. In either case, the signal swing is reduced by 1/21th, or 5%, due to resistive voltage division.

Output Data Formats and Overrange Bit

The transfer curve shown in Figure 2 approximates a perfectly linear transfer curve that defines the relationship between input voltage and offset two's complement decimal code. In this offset code, 0 represents the lowest (negative) input range and $2^{resolution} - 1$ represents the highest (positive) input range. The RAD020 output word formed by DP/N<0-9> represents this offset code in binary format:

$$offset\ code = \sum_{i=0}^{9} D<i>\, 2^{i} \ , \tag{10}$$

where:

$$D<i> = \frac{1 + \mathrm{sgn}(DP<i> - DN<i>)}{2} \ . \tag{11}$$

A two's complement binary code can easily be obtained from the offset two's complement code by inversion of the MSB. Since the RAD020 outputs are differential, this code results by simply twisting the DP/N<9> connections.

An overrange bit, DOVRP/N, is output with every data word and indicates the condition that the lowest or the highest code of the ADC is assumed. It is low, except if the ADC output is one of the extreme codes,

corresponding to an input at or beyond the limits of the linear ADC input range. The timing is the same as that of the digital data outputs, see Figure 3.

Ideal-ADC Input Range (LSB)	ADC Output Code				ADC Over Range Bit
	Offset Two's Complement		Two's Complement		
	BINARY	DECIMAL	BINARY	DECIMAL	
< -511	0000000000	0	1000000000	-512	1
-511 to -510	0000000001	1	1000000001	-511	0
…	…	…	…	…	0
-1 to 0	0111111111	511	1111111111	-1	0
0 to 1	1000000000	512	0000000001	0	0
…	…	…	…	…	0
510 to 511	1111111110	1022	0111111110	510	0
> 511	1111111111	1023	0111111111	511	1

Temperature Measurement

TBD.

Power Supplies

Due to its highly differential design, the RAD020 requires relatively modest power supply decoupling. The 0.01 μF capacitors VEEX-to-GNDX and VEEA-to-VCC (Figure 10) should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEEX-to-GNDX and VCCA-to-GNDA, should be placed within 1 inch of the RTH010. Depending on the expected noise on the supplies more capacitors in parallel may need to be used.

Equivalent Input and Output Schematics

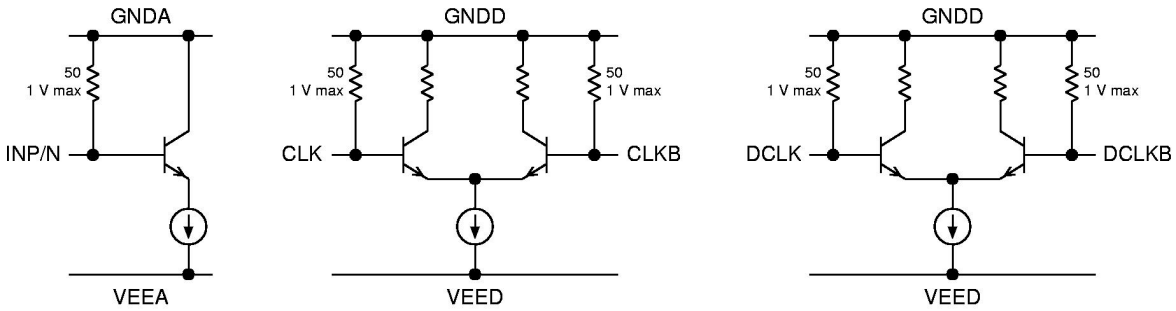

Figure 6. Equivalent circuits for analog and clock inputs.

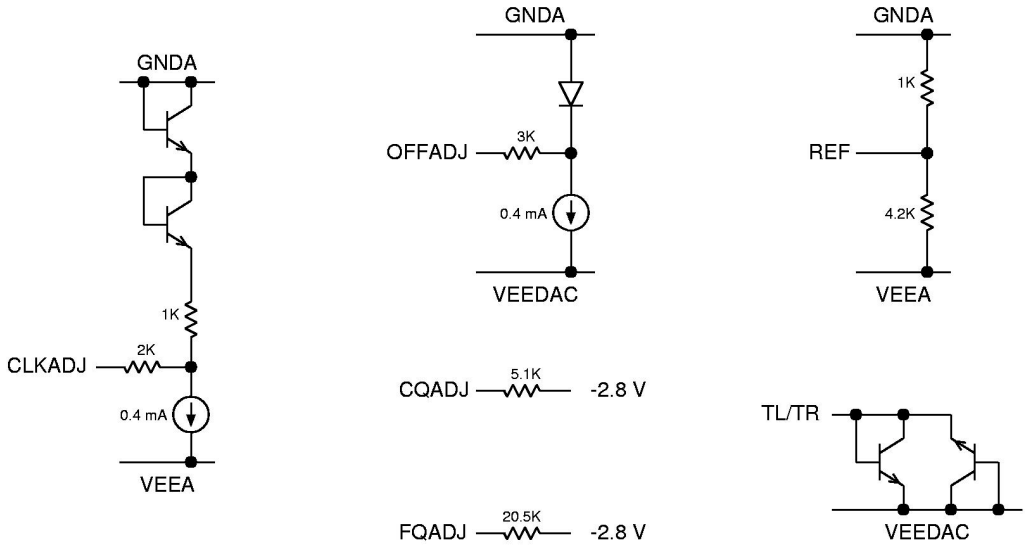

Figure 7. Equivalent circuits for adjusts, reference, and temperature sense.

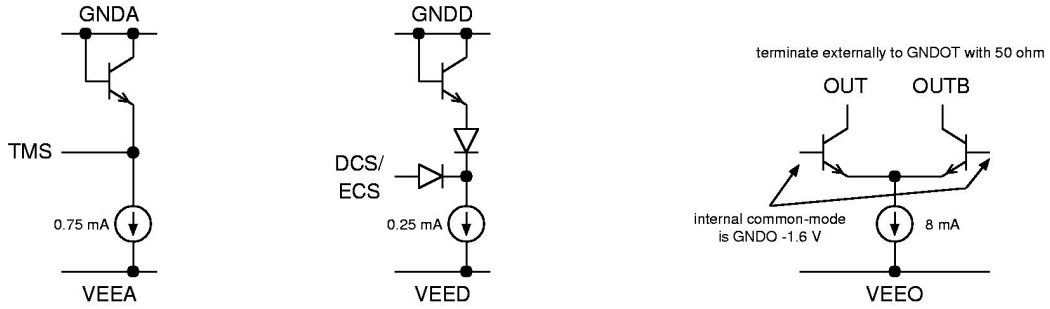

Figure 8. Equivalent circuits for digital inputs and outputs [DP/N<0-9>,DOVRP/N,CLKO(B)]

Pin Configuration

Figure TBD

Figure 9. Pin configuration (top view, not to scale)

Typical Operating Circuit

Figure TBD

Figure 10. Typical interface circuit.

Die Plot and Pad Arrangement

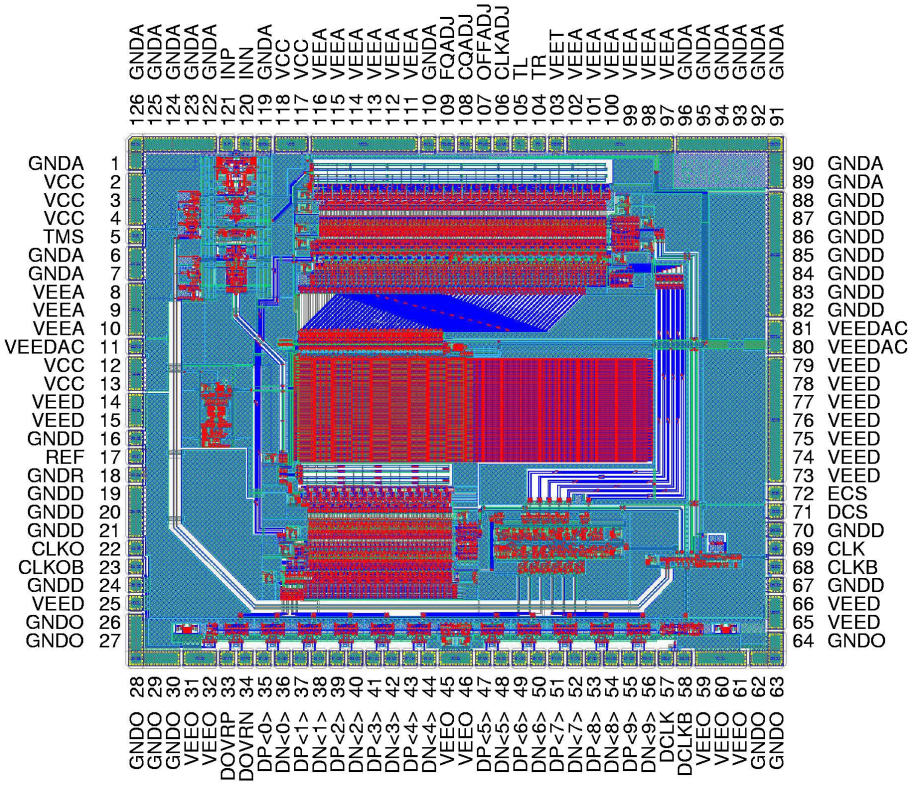

Figure 11. RTH020 die plot and pad arrangement
Die size: 217 x 175 x 7 mils (5.499 x 4.449 x 0.178 mm)
Pad pitch: 5.91 mil (0.150 mm)

Ordering Information

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
RAD020DIE	Die	0 to +100 °C