Intel®Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process (intended for sub-45W TDP designs) at 1.60 GHz, 1.80 GHz, and 2 GHz

Datasheet

Product Features

- Available at 1.60, 1.80, and 2 GHz
- Binary compatible with applications running on previous members of the Intel microprocessor line
- Intel® NetBurst™ micro-architecture
- System bus frequency at 400 MHz
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper Pipelined Technology
- Advance Dynamic Execution
  - —Very deep out-of-order execution
  - —Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12K micro-ops and removes decoder latency from main execution loops
- Limited to 45W Thermal Design Point and intended for the small form factor desktop market
- 8 KB Level 1 data cache
- 512 KB Advanced Transfer Cache (on-die, full speed Level 2 (L2) cache) with 8-way associativity and Error Correcting Code (ECC)
- 144 new Streaming SIMD Extensions 2 (SSE2) instructions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - —System Management mode
  - —Multiple low-power states
- Optimized for 32-bit applications running on advanced 32-bit operating systems
- 8-way cache associativity provides improved cache hit rate on load/store operations

The Intel® Pentium® 4 processor with 512KB L2 cache on .13 micron process (intended for sub-45W TDP designs) is designed for small form factor desktops. It is binary compatible with previous Intel Architecture processors. The Pentium 4 processor provides great performance for applications running on advanced operating systems such as Windows* 98, Windows* ME, Windows* 2000, Windows* XP, and UNIX*. This is achieved by the Intel® NetBurst™ micro-architecture which brings a new level of performance for system buyers. The Pentium 4 processor extends the power of the Pentium III processor with performance headroom for advanced audio and video internet capabilities. Systems based on Pentium 4 processors also include the latest features to simplify system management and lower the total cost of ownership for large and small business environments. The Pentium 4 processor offers great performance for today's and tomorrow's applications.

Order Number: 298639-001
January 2002

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1.0 Introduction

The Intel® Pentium® 4 processor with 512KB L2 cache (intended for sub-45W TDP designs) is a lower power version of the Pentium 4 processor. The thermal design point for the Intel® Pentium® 4 processor with 512KB L2 cache (intended for sub-45W TDP designs) will be at most 45 watts. The Pentium 4 processor with 512KB cache utilizes Flip-Chip Pin Grid Array package technology, and plugs into a 478-pin surface mount, Zero Insertion Force (ZIF) socket, referred to as the mPGA478B socket. The Pentium 4 processor with 512KB cache is based on the Intel NetBurst™ micro-architecture and maintains the tradition of compatibility with IA-32 software. In this document the Pentium 4 processor with 512KB cache will be referred to as the “Pentium 4 processor”, or simply “the processor”.

The Intel NetBurst micro-architecture features include hyper-pipelined technology, a rapid execution engine, a 400 MHz system bus, and an execution trace cache. The rapid execution engine allows the two integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400 MHz system bus is a quad-pumped bus running off a 100 MHz system clock making 3.2 GBytes/sec data transfer rates possible. The execution trace cache is a first level cache that stores approximately 12k decoded micro-operations, which removes the instruction decoding logic from the main execution path, thereby increasing performance.

Additional features within the Intel NetBurst micro-architecture include advanced dynamic execution, advanced transfer cache, an enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 512KB, on-die level 2 (L2) cache. A new floating point and multimedia unit has been implemented which provides superior performance for multi-media and mathematically intensive applications. Finally, SSE2 adds 144 new instructions for double-precision floating point, SIMD integer, and memory management. Power management capabilities such as AutoHALT, Stop-Grant, Sleep, and Deep Sleep have been retained.

The Streaming SIMD Extensions 2 (SSE2) enable break-through levels of performance in multimedia applications including 3-D graphics, video decoding/encoding, and speech recognition. The new packed double-precision floating-point instructions enhance performance for applications that require greater range and precision, including scientific and engineering applications and advanced 3-D geometry techniques, such as ray tracing.

The Pentium 4 processor’s 400 MHz Intel NetBurst micro-architecture system bus uses a variant of GTL+ signalling technology called Assisted Gunning Transceiver Logic (AGTL+) signal technology and utilizes a split-transaction, deferred reply protocol. This system bus is not compatible with the P6 processor family bus. The 400 MHz Intel NetBurst micro-architecture system bus uses Source-Synchronous Transfer (SST) of address and data to improve performance by transferring data four times per bus clock (4X data transfer rate, as in AGP 4X). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a “double-clocked” or 2X address bus. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 3.2 Gbytes/second.

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

"System Bus" refers to the interface between the processor and system core logic (a.k.a. the chipset components). The system bus is a multiprocessing interface to processors, memory, and I/O.

1.1.1 Processor Packaging Terminology

Commonly used terms are explained here for clarification:

- **Intel Pentium 4 processor in the 478-pin package** — 0.18 micron Intel Pentium 4 processor core in the 478 pin uPGA package.
- **Intel Pentium 4 processor in the 423-pin package** — 0.18 micron Intel Pentium 4 processor core in the PGA package.
- **Intel® Pentium® 4 processor with 512KB L2 cache** — 0.13 micron version of Intel Pentium 4 processor in the 478-pin package with a 512 KB L2 cache.
- **Intel® Pentium® 4 processor with 512KB L2 cache (intended for sub-45W TDP designs)** — 0.13 micron version of Intel Pentium 4 processor in the 478-pin package with a 512 KB L2 cache and limited to 45W thermal design power.
- **Processor** — For this document, the term processor shall mean Intel® Pentium® 4 processor with 512KB L2 cache limited to 45W TDP.
- **Keep out zone** — The area on or near the processor that system design can not utilize. This area must be kept free of all components to make room for the processor package, retention mechanism, heat sink, and heat sink clips.
- **Intel® 850 chipset**— chipset which supports RDRAM* memory technology.
- **Intel® 845 chipset** — chipset which supports SDRAM and DDR SDRAM memory technologies.
- **Processor core** — Intel® Pentium® 4 processor with 512KB L2 cache core die with integrated L2 cache.
- **mPGA478B socket** — surface mount, 478 pin, Zero Insertion Force (ZIF) socket with 50 mil pin pitch. Mates the processor to the system board.
- **Integrated heat spreader** — The surface used to make contact between a heatsink or other thermal solution and the processor. Abbreviated IHS.
- **Retention mechanism** — The structure mounted on the system board which provides support and retention of the processor heatsink.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document:

Table 1. References

Document	Order Number
Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide	Note 1
Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform for DDR Design Guide	Note 1
Intel® Pentium® 4 Processor in the 478-Pin Package datasheet	Note 1
VRM 9.0 DC-DC Converter Design Guidelines	Note 1
Intel® Pentium® 4 Processor VR-Down Design Guidelines	Note 1
CK00 Clock Synthesizer/Driver Design Guidelines	Note 1
CK408 Clock Design Guidelines	Note 1
Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478B) Socket Design Guidelines	Note 1
Intel® Architecture Software Developer's Manual	Note 1
Volume I: Basic Architecture	245470
Volume II: Instruction Set Reference	245471
Volume III: System Programming Guide	245472
Intel® Pentium® 4 Processor in the 478-pin Package Processor I/O Buffer models	
Intel® Pentium® 4 Processor Overshoot Checker Tool	
Intel® Pentium® 4 Processor with 512KB L2 Cache in the .13 Micron Process/Pentium® 4 in the 478 Pin Package Debug Port Design Guide	Note 1
ITP700 Debug Port Design Guide	Note 1
Intel® Pentium® 4 Processor in the 478-pin Package ProcessorFloTherm Models	
Intel® Pentium® 4 Processor in the 478-pin Package Processor Icepak Models	
Pentium® 4 in the 478 Pin Package/Intel® Pentium® 4 Processor with 512KB Cache in the .13 Micron Process Enabled Components drawings	

Note:

1. Contact your Intel representative for the latest revision and order number of this document.

2.0 Electrical Specifications

2.1 System Bus and GTLREF

Most Pentium 4 processor system bus signals use Assisted Gunning Transceiver Logic (AGTL+) signalling technology. As with the P6 family of microprocessors, this signalling technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. The termination voltage level for the Pentium 4 processor AGTL+ signals is V_{CC}, which is the operating voltage of the processor core. The use of a termination voltage that is determined by the processor core allows better voltage scaling on the system bus for Pentium 4 processors. Because of the speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families. Design guidelines for the Pentium 4 processor system bus are detailed in the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board.

Termination resistors are provided on the processor silicon and are terminated to its core voltage (V_{CC}). The Intel 850 and the Intel 845 chipsets will also provide on-die termination, thus eliminating the need to terminate the bus on the system board for most AGTL+ signals. However, some AGTL+ signals do not include on-die termination and must be terminated on the system board. For more information, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

The AGTL+ bus depends on incident wave switching. Therefore timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the system bus, including trace lengths, is highly recommended when designing a system.

2.2 Power and Ground Pins

For clean on-chip power distribution, the Pentium 4 processor has 85 V_{CC} (power) and 181 V_{SS} (ground) inputs. All power pins must be connected to V_{CC}, while all V_{SS} pins must be connected to a system ground plane.The processor V_{CC} pins must be supplied with the voltage defined by the VID (Voltage ID) pins and the loadline specifications (see Figure 4).

2.3 Decoupling Guidelines

Due to the large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Care must be taken in the board design to ensure that the

voltage provided to the processor remains within the specifications listed in Table 6. Failure to do so can result in timing violations and/or affect the long term reliability of the processor. For further information and design guidelines, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

2.3.1 V_{CC} Decoupling

Regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/ exiting low power states, must be provided by the voltage regulator solution (VR). For more details on this topic, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

2.3.2 System Bus AGTL+ Decoupling

Pentium 4 processors integrate signal termination on the die as well as incorporate high frequency decoupling capacitance on the processor package. Decoupling must also be provided by the system system board for proper AGTL+ bus operation. For more information, refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

2.4 Voltage Identification

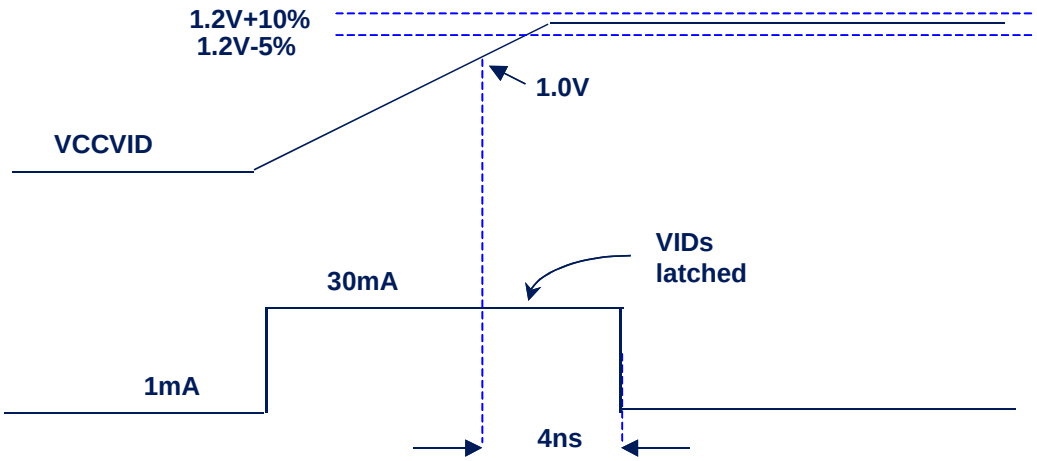
The VID specification for Pentium 4 processors is supported by the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*. The voltage set by the VID pins is the maximum voltage allowed by the processor. A minimum voltage is provided in Table 6 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Pentium 4 processors use five voltage identification pins, VID[4:0], to support automatic selection of power supply voltages. The VID pins for Pentium 4 processor are open drain outputs driven by the processor VID circuitry. The VID signals rely on pull-up resistors tied to a 3.3V (max) supply to set the signal to a logic high level. These pull-up resistors may be either external logic on the system board or internal to the Voltage Regulator. Table 2 specifies the voltage level corresponding to the state of VID[4:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to low voltage level. The definition provided in Table 2 is not related in any way to previous P6 processors or VRs, but is compatible with the Intel Pentium 4 Processor in the 478-pin package. If the processor socket is empty (VID[4:0] = 11111), or the voltage regulation circuit cannot supply the voltage that is requested, it must disable itself. See the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for more details.

Power source characteristics must be stable whenever the supply to the voltage regulator is stable. Refer to the Figure 11 for timing details of the power up sequence.

Pentium 4 processor's Voltage Identification circuit requires an independent 1.2V supply. This voltage must be routed to the processor VCCVID pin. Figure 1 shows the voltage and current requirements of the VCCVID pin. See Table 6 for VCCVID specifications.

Figure 1. VCCVID Pin Voltage and Current Requirements



NOTE: The rising edge of VCCVID must be monotonic from 0 to 1.1V.

Table 2. Voltage Identification Definition (Page 1 of 2)

Processor Pins					
VID4	VID3	VID2	VID1	VID0	V_{CC_MAX}
1	1	1	1	1	VRM output off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525

Table 2. Voltage Identification Definition (Page 2 of 2)

0	1	1	0	0	1.550

2.4.1 Phase Lock Loop (PLL) Power and Filter

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system; it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from V_{CC}. A typical filter topology is shown in Figure 2.

The AC low-pass requirements, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 2), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 3. For recommendations on implementing the filter refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

Figure 2. Typical $V_{CCIOPLL}$, V_{CCA} and V_{SSA} Power Distribution

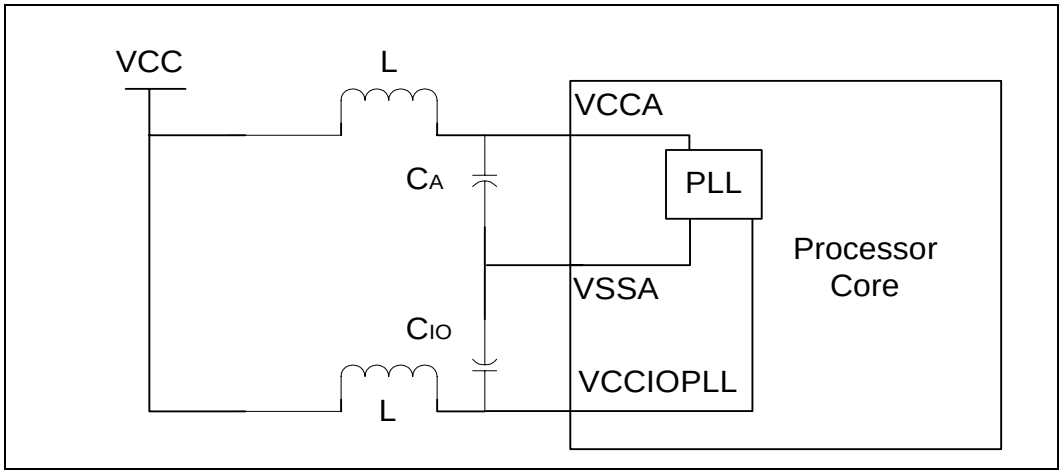
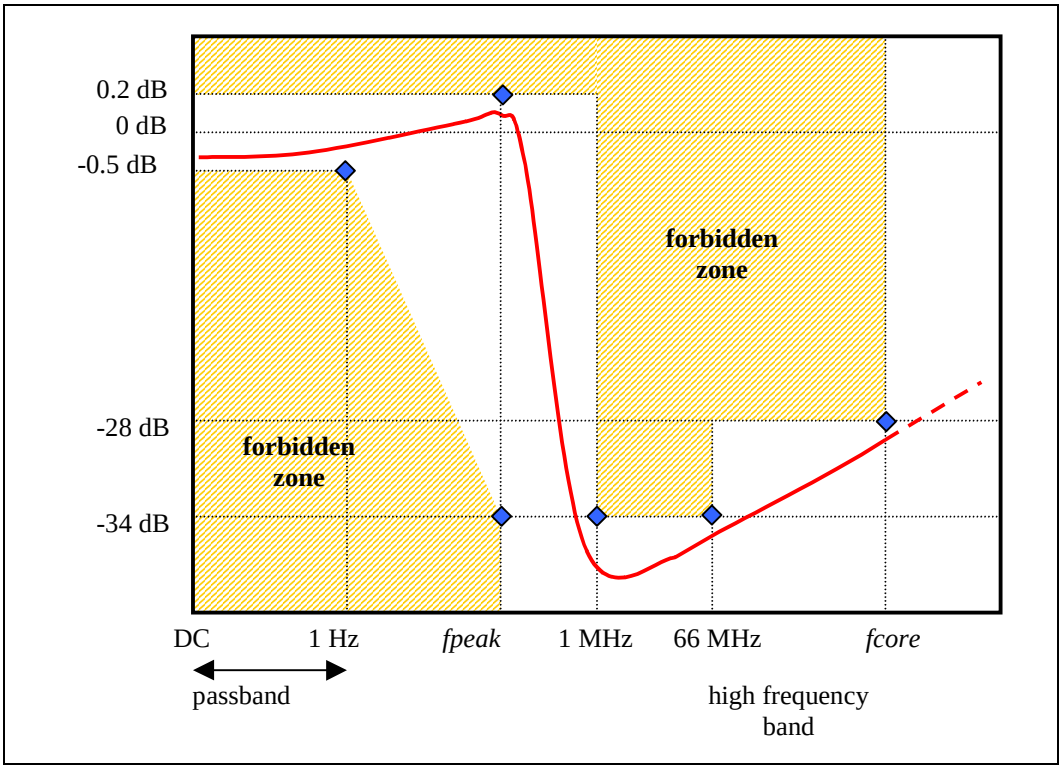


Figure 3. Phase-Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond fcore (core frequency).
3. fpeak, if existent, should be less than 0.05 MHz.

2.5 Reserved, Unused Pins, and TESTHI[12:0]

All RESERVED pins must remain unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future Pentium 4 processors. See Chapter 5.0 for a pin listing of the processor and the location of all RESERVED pins.

For reliable operation, always connect unused inputs or bidirectional signals that are not terminated on the die to an appropriate signal level. Note that on-die termination has been included on the Pentium 4 processor to allow signals to be terminated within the processor silicon. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Table 3 lists details on AGTL+ signals that do not include on-die termination. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

Unused outputs can be left unconnected, however, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals that don't have on-die termination, use pull-up resistors of the same value in place of the on-die termination resistors (R_{TT}). See Table 13.

The TAP, Asynchronous GTL+ inputs, and Asynchronous GTL+ outputs do not include on-die termination. Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left unconnected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. Signal termination for these signal types is discussed in the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

The TESTHI pins should be tied to the processor V_{CC} using a matched resistor, where a matched resistor has a resistance value within ± 20% of the impedance of the board transmission line traces. For example, If the trace impedance is 50 Ω, then a value between 40 and 60 Ω is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. A matched resistor should be used for each group:

1. TESTHI[1:0]
2. TESTHI[5:2]
3. TESTHI[10:8]
4. TESTHI[12:11]

Additionally, if the ITPCLKOUT[1:0] pins are not used (refer to Section 5.2) then they may be connected individually to V_{CC} using matched resistors or grouped with TESTHI[5:2] with a single matched resistor. If they are being used, individual termination with 1 kΩ resistors is acceptable. Tying ITPCLKOUT[1:0] directly to V_{CC} or sharing a pull-up resistor to V_{CC} will prevent use of debug interposers. **This implementation is strongly discouraged for system boards that do not implement an onboard debug port.**

As an alternative, group 2 (TESTHI [5:2]) and the ITPCLKOUT[1:0] pins may be tied directly to the processor V_{CC}. This has no impact on system functionality. TESTHI0 and TESTHI12 may also be tied directly to processor V_{CC} if resistor termination is a problem, but matched resistor termination is recommended. **In the case of the ITPCLKOUT[1:0], direct tie to V_{CC} is strongly discouraged for system boards that do not implement an onboard debug port.**

2.6 System Bus Signal Groups

In order to simplify the following discussion, the system bus signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 3 identifies which signals are common clock, source synchronous, and asynchronous.

Table 3. System Bus Pin Groups

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Common Clock	BPRI#, DEFER#, RESET#[2], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Common Clock	AP[1:0]#, ADS#, BINIT#, BNR#, BPM[5:0]#[2], BR0#[2], DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Source Synchronous I/O	Source Synchronous	<table><tr><th>Signals</th><th>Associated Strobe</th></tr><tr><td>REQ[4:0]#, A[16:3]#[5]</td><td>ADSTB0#</td></tr><tr><td>A[35:17]#[5]</td><td>ADSTB1#</td></tr><tr><td>D[15:0]#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16]#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32]#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table>
AGTL+ Strobes	Common Clock	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
Asynchronous GTL+ Input[4,5]	Asynchronous	A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, STPCLK#
Asynchronous GTL+ Output[4]	Asynchronous	FERR#, IERR#[2], THERMTRIP#, PROCHOT#
TAP Input[4]	TAP Input	TCK, TDI, TMS, TRST#
TAP Output[4]	TAP Output	TDO
System Bus Clock	N/A	BCLK[1:0], ITP_CLK[1:0][3]
Power/Other	N/A	V_{CC}, V_{CCA}, $V_{CCIOPLL}$, VCCVID, VID[4:0], V_{SS}, V_{SSA}, GTLREF[3:0], COMP[1:0], RESERVED, TESTHI[5:0], TESTHI[12:8], ITPCLKOUT[1:0],THERMDA, THERMDC, SKTOCC#, V_{CC_SENSE}, V_{SS_SENSE}, BSEL[1:0][4], DBR#[3]

NOTES:

1. Refer to Section 5.2 for signal descriptions.
2. These AGTL+ signals do not have on-die termination. Refer to Section 2.5 and the *Pentium® 4 Processor Debug Port Design Guide* for termination requirements.
3. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
4. These signal groups are not terminated by the processor. Refer to Section 2.5, the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for termination requirements and further details.
5. The value of these pins during the active-to-inactive edge of RESET# defines the processor configuration options. See Section 7.1 for details.

2.7 Asynchronous GTL+ Signals

Pentium 4 processors do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. These signals follow the similar DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them. See Section 2.11 and Section 2.13 for the DC and AC specifications for the Asynchronous GTL+ signal groups. See Section 7.2 for additional timing requirements for entering and leaving the low power states.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, it is recommended that the Pentium 4 processor be first in the TAP chain and followed by any other components within the system. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage level. Similar considerations must be made for TCK, TMS, and TRST#. Two copies of each signal may be required, with each driving a different voltage level.

2.9 System Bus Frequency Select Signals (BSEL[1:0])

The BSEL[1:0] are output signals used to select the frequency of the processor input clock (BCLK[1:0]). Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All agents must operate at the same frequency.

The Pentium 4 processor currently operates at a 400 MHz system bus frequency (selected by a 100 MHz BCLK[1:0] frequency). Individual processors will only operate at their specified system bus frequency.

For more information about these pins refer to Section 5.2 and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for termination requirements and further details.

Table 4. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
L	L	100 MHz
L	H	RESERVED
H	L	RESERVED
H	H	RESERVED

2.10 Maximum Ratings

Table 5 lists the processor's maximum environmental stress ratings. The processor should not receive a clock while subjected to these conditions. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the processor contains protective circuitry to resist damage from Electro Static Discharge (ESD), one should always take precautions to avoid exposing the processor to high static voltages or electric fields.

Table 5. Processor DC Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{STORAGE}$	Processor storage temperature	-40	85	°C	2
V_{CC}	Any processor supply voltage with respect to V_{SS}	-0.3	1.75	V	1
$V_{inAGTL+}$	AGTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.75	V	
$V_{inAsynch\_GTL+}$	Asynch GTL+ buffer DC input voltage with respect to V_{SS}	-0.1	1.75	V	
I_{VID}	Max VID pin current		5	mA	

1. This rating applies to any processor pin.
2. Contact Intel for storage requirements in excess of one year.

2.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core silicon unless noted otherwise. See Chapter 5.0 for the pin signal definitions and signal pin assignments. Most of the signals on the processor system bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 9.

Previously, legacy signals and Test Access Port (TAP) signals to the processor used low-voltage CMOS buffer types. However, these interfaces now follow DC specifications similar to GTL+. The DC specifications for these signal groups are listed in Table 10.

Table 6 through Table 10 list the DC specifications for the Pentium 4 processor and are valid only while meeting specifications for case temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 6. Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{CC}	V_{CC} for Processor at VID=1.500V: 1.60 GHz 1.80 GHz 2 GHz	 1.370 1.365 1.355	Refer to Table 7 and Figure 4		V	2, 3, 4, 5, 9
VCCVID	V_{CC} for voltage identification circuit	-5%	1.2V	+10%	V	11
I_{CC}	I_{CC} for Processor at VID=1.500V: 1.60 GHz 1.80 GHz 2 GHz			 32.8 35.7 38.6	A	4, 5, 7, 9
I_{SGNT} I_{SLP}	I_{CC} for Stop-Grant and Sleep			14.0	A	6, 8
I_{DSLP}	I_{CC} for Deep Sleep			12.0	A	
I_{TCC}	I_{CC} TCC active			I_{CC}	A	7
$I_{CC\ PLL}$	I_{CC} for PLL pins			60	mA	

NOTES:

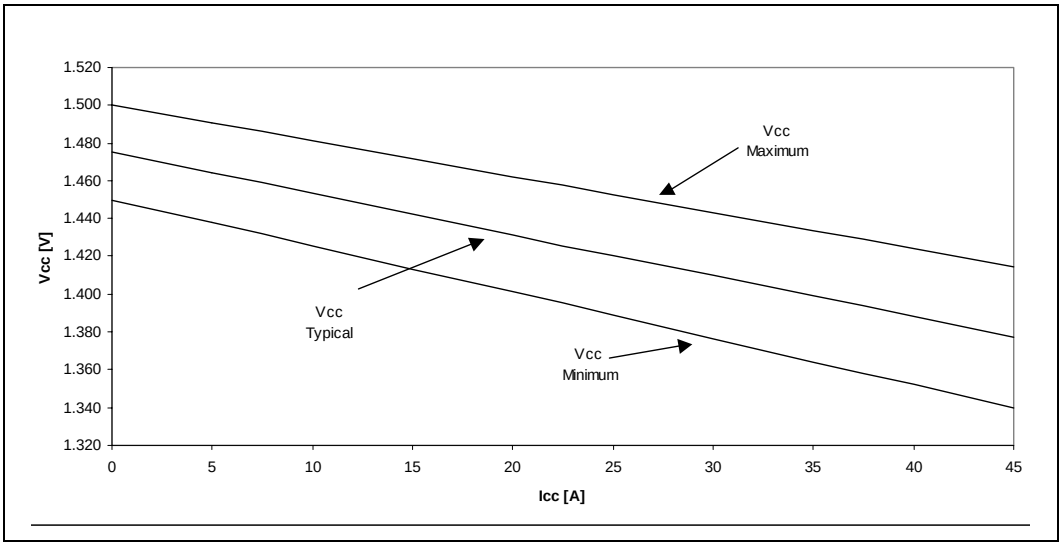
1. Unless otherwise noted, all specifications in this table are based on characterized data from silicon measurements.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.4 and Table 2 for more information. The VID bits will set the maximum V_{CC} with the minimum being defined according to current consumption at that voltage.
3. The voltage specification requirements are measured across $V_{CCSENSE}$ and $V_{SSSENSE}$ pins at the socket with a 100MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.
4. Refer to Table 7 and Figure 4 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current. Moreover, V_{CC} should never exceed the VID voltage. Failure to adhere to this specification can affect the long term reliability of the processor.
5. V_{CC_MIN} is defined at I_{CC_MAX}.
6. The current specified is also for AutoHALT State.
7. The maximum instantaneous current the processor will draw while the thermal control circuit is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
8. I_{CC} Stop-Grant and I_{CC} Sleep are specified at V_{CC_MAX}.
9. These specifications apply to processor with VID setting of 1.500V.
10. These specifications apply to processor with VID setting of 1.400V.
11. This specification applies to both static and transient components. The rising edge of VCCVID must be monotonic from 0 to 1.1V. See Figure 1 for current requirements. In this case monotonic is defined as continuously increasing with less than 50mV of peak to peak noise for any width greater than 2ns superimposed on the rising edge.

Table 7. Vcc Static and Transient Tolerance

Icc (A)	Voltage Deviation from VID Setting (V)[1,2,3,4]		
	Maximum	Typical	Minimum
0	0.000	-0.025	-0.050
5	-0.010	-0.036	-0.062
10	-0.019	-0.047	-0.075
15	-0.029	-0.058	-0.087
20	-0.038	-0.069	-0.099
25	-0.048	-0.079	-0.111
30	-0.057	-0.090	-0.124
35	-0.067	-0.101	-0.136
40	-0.076	-0.112	-0.148
45	-0.085	-0.123	-0.160

NOTES:
1. The loadline specifications include both static and transient limits.
2. This table is intended to aid in reading discrete points on the loadline figure below.
3. The loadlines specify voltage limits at the die measured at $V_{CCSENSE}$ and $V_{SSSENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines* for V_{CC} and V_{SS} socket loadline specifications and VR implementation details.
4. Adherence to this loadline specification for the Pentium 4 processor is required to ensure reliable processor operation.
5. Adherence to this loadline specification for the Pentium 4 processor is required to ensure reliable processor operation.

Figure 4. V_{CC} Static and Transient Tolerance (VID = 1.500V)



NOTES:
1. The loadline specification includes both static and transient limits.
2. This loadline specification applies to processors with a VID setting of 1.500V.
3. The loadlines specify voltage limits at the die measured at $V_{CCSENSE}$ and $V_{SSSENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins. Refer to the *Intel®*

Pentium® 4 Processor VR-Down Design Guidelines V_{CC} and V_{SS} socket loadline specifications and VR implementation details.

4. Adherence to this loadline specification for the Pentium 4 processor is required to ensure reliable processor operation.

Table 8. System Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes[1]
V_L	Input Low Voltage	-0.150	0.000		V	8	
V_H	Input High Voltage	0.660	0.710	0.850	V	8	
$V_{CROSS(ABS)}$	Absolute Crossing Point	0.250		0.550	V	8, 9	2, 8
$V_{CROSS(REL)}$	Relative Crossing Point	0.250 + 0.5 * (V_{Havg} - 0.710)		0.550 + 0.5 * (V_{Havg} - 0.710)	V	8, 9	2, 3, 8, 9
ΔV_{CROSS}	Range of Crossing Points			0.140	V	8, 9	2
V_{OV}	Overshoot			V_H + 0.3	V	8	4
V_{US}	Undershoot	-0.300			V	8	5
V_{RBM}	Ringback Margin	0.200			V	8	6
V_{TM}	Threshold Margin	V_{CROSS} -0.100		V_{CROSS}+0.100	V	8	7

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 equals the falling edge of BCLK1.
3. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
4. Overshoot is defined as the absolute value of the maximum voltage.
5. Undershoot is defined as the absolute value of the minimum voltage.
6. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
7. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
8. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
9. V_{Havg} can be measured directly using "Vtop" on Agilent* scopes and "High" on Tektronix* scopes.

Table 9. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
GTLREF	Reference Voltage	2/3 V_{CC} - 2%	2/3 V_{CC} + 2%	V	
V_{IH}	Input High Voltage	1.10*GTLREF	V_{CC}	V	2, 6
V_{IL}	Input Low Voltage	0.0	0.9*GTLREF	V	3, 4, 6
V_{OH}	Output High Voltage		V_{CC}	V	7
I_{OL}	Output Low Current		50	mA	6
I_{LO}	Pin Leakage Low		± 500	µA	9
I_{HI}	Pin Leakage High		± 100	µA	9
R_{ON}	Buffer On Resistance	7	11	Ω	5

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.

4. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
5. Refer to processor I/O Buffer Models for I/V characteristics.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.
7. V_{OL} max of 0.450 Volts is guaranteed when driving into a test load of 50Ω as indicated in Figure 6.
8. Leakage to V_{CC} with pin held at 300mV.
9. Leakage to V_{SS} with pin held at V_{CC}.

Table 10. Asynchronous GTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{IH}	Input High Voltage Asynch GTL+	1.10*GTLREF	V_{CC}	V	3, 4, 5
V_{IL}	Input Low Voltage Asynch. GTL+	0.0	0.9*GTLREF	V	5
V_{OH}	Output High Voltage		V_{CC}	V	2, 3, 4
I_{OL}	Output Low Current		50	mA	6, 8
I_{LO}	Pin Leakage Low		± 500	µA	9
I_{HI}	Pin Leakage High		± 100	µA	10
R_{ON}	Buffer On Resistance Asynch GTL+	7	11	Ω	5, 7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.
3. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Chapter 3.0.
4. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
5. This specification applies to the asynchronous GTL+ signal group.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 6.
7. Refer to the processor I/O Buffer Models for I/V characteristics.
8. V_{OL} max of 0.270 Volts is guaranteed when driving into a test load of 50Ω as indicated in Figure 6, with R_{TT} enabled.
9. Leakage to V_{CC} with pin held at 300mV.
10. Leakage to V_{SS} with pin held at V_{CC}.

Table 11. TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{HYS}	TAP Input Hysteresis	200	300	mV	8
V_{T+}	TAP Input Low to High Threshold Voltage	$1/2*(V_{CC}+V_{HYS\_MIN})$	$1/2*(V_{CC}+V_{HYS\_MAX})$	V	5
V_{T-}	TAP Input High to Low Threshold Voltage	$1/2*(V_{CC}-V_{HYS\_MAX})$	$1/2*(V_{CC}-V_{HYS\_MIN})$	V	5
V_{OH}	Output High Voltage		V_{CC}	V	2, 3, 5
I_{OL}	Output Low Current		40	mA	6, 7
I_{LO}	Pin Leakage Low		± 500	µA	9
I_{HI}	Pin Leakage High		± 100	µA	10
R_{ON}	Buffer On Resistance	8.75	13.75	Ω	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All outputs are open-drain.

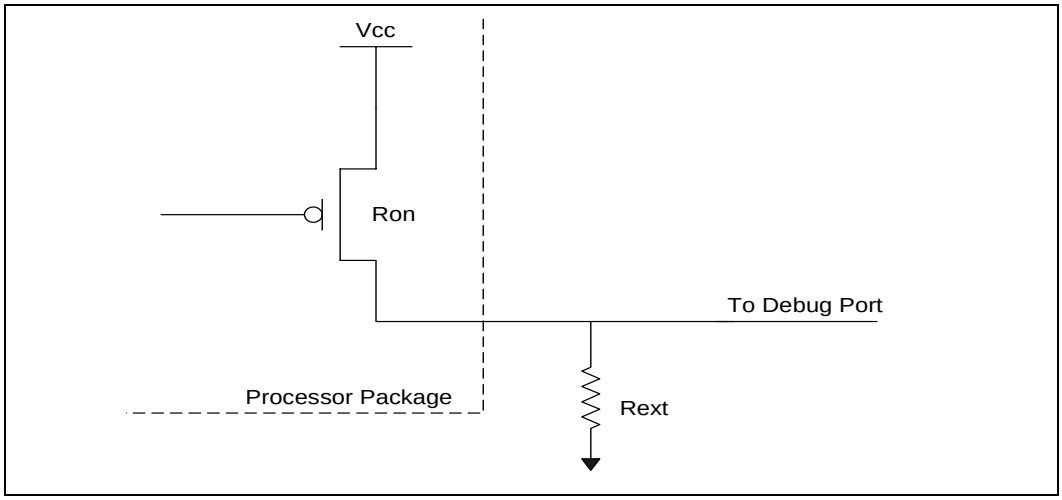
3. The TAP signal group must comply with the signal quality specifications in Chapter 3.0.
4. Refer to I/O Buffer Models for I/V characteristics.
5. The V_{CC} referred to in these specifications refers to instantaneous V_{CC}.
6. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load shown in Figure 6.
7. V_{OL} max of 0.320 Volts is guaranteed when driving into a test load of 50Ω as indicated in Figure 6 for the TAP Signals.
8. V_{HYS} represents the amount of hysteresis, nominally centered about 1/2 V_{CC} for all TAP inputs
9. Leakage to V_{CC} with pin held at 300mV.
10. Leakage to V_{SS} with pin held at V_{CC}..

Table 12. ITPCLKOUT[1:0] DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
R_{ON}	Buffer On Resistance	27	46	Ω	2, 3

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. See Figure 5 for ITPCLKOUT[1:0] output buffer diagram.

Figure 5. ITPCLKOUT[1:0] Output Buffer Diagram



NOTES:
1. See Table 12 for range of R_{ON}.
2. The V_{CC} referred to in this figure is the instantaneous V_{CC}.
3. Refer to the *Pentium® 4 Processor Debug Port Design Guide* and *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for the value of R_{EXT}.

2.12 AGTL+ System Bus Specifications

Routing topology recommendations may be found in the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.* Termination resistors are not required for most AGTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF.

Table 13 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled. For more details on platform design see the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide.*

Table 13. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
GTLREF	Bus Reference Voltage	2/3 V_{CC} -2%	2/3 V_{CC}	2/3 V_{CC} +2%	V	2, 3, 6
R_{TT}	Termination Resistance	45	50	55	Ω	4
COMP[1:0]	COMP Resistance	50.49	51	51.51	Ω	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The tolerances for this specification have been stated generically to enable the system designer to calculate the minimum and maximum values across the range of V_{CC}.
3. GTLREF should be generated from V_{CC} by a voltage divider of 1% tolerance resistors or 1% tolerance, matched resistors. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for implementation details.
4. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Refer to processor I/O buffer models for I/V characteristics.
5. COMP resistance must be provided on the system board with 1% tolerance resistors. See the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for implementation details.
6. The V_{CC} referred to in these specifications is the instantaneous V_{CC}.

2.13 System Bus AC Specifications

The processor system bus timings specified in this section are defined at the processor silicon. See Chapter 5.0 for the Pentium 4 processor pin signal definitions. Table 14 through Table 19 list the AC specifications associated with the processor system bus. All AGTL+ timings are referenced to GTLREF for both '0' and '1' logic levels unless otherwise specified.

The timings specified in this section should be used in conjunction with the I/O buffer models provided by Intel. These I/O buffer models, which include package information, are available for the Pentium 4 processor in IBIS format. AGTL+ layout guidelines are also available in the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide*.

Care should be taken to read all notes associated with a particular timing parameter.

Table 14. System Bus Differential Clock Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
System Bus Frequency			100	MHz		
T1: BCLK[1:0] Period	10.0		10.2	ns	8	2
T2: BCLK[1:0] Period Stability			200	ps		3, 4
T3: BCLK[1:0] High Time	3.94	5	6.12	ns	8	
T4: BCLK[1:0] Low Time	3.94	5	6.12	ns	8	
T5: BCLK[1:0] Rise Time	175		700	ps	8	5
T6: BCLK[1:0] Fall Time	175		700	ps	8	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2).
3. For the clock jitter specification, refer to the *CK408 Clock Synthesizer/Driver Design Guidelines*.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Slew rate is measured between the 35% and 65% points of the clock swing (V_L to V_H).

Table 15. System Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3]
T10: Common Clock Output Valid Delay	0.12	1.27	ns	10	4
T11: Common Clock Input Setup Time	0.65		ns	10	5
T12: Common Clock Input Hold Time	0.40		ns	10	5
T13: RESET# Pulse Width	1	10	ms	11	6, 7, 8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at the rising edge of BCLK0. All common clock AGTL+ signal timings are referenced to GTLREF at the processor core.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 6 and with GTLREF at 2/3 V_{CC} ± 2%.
5. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.4 V/ ns to 4.0V/ns.
6. RESET# can be asserted asynchronously, but must be deasserted synchronously.
7. This should be measured after V_{CC} and BCLK[1:0] become stable
8. Maximum specification applies only while PWRGOOD is asserted.

Table 16. System Bus Source Synch AC Specifications AGTL+ Signal Group

T# Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2,3,4]
T20: Source Synchronous Data Output Valid Delay (first data/address only)	0.20		1.20	ns	12, 13	5
T21: T_{VBD}: Source Synchronous Data Output Valid Before Strobe	0.85			ns	13	5, 8
T22: T_{VAD}: Source Synchronous Data Output Valid After Strobe	0.85			ns	13	5, 8
T23: T_{VBA}: Source Synchronous Address Output Valid Before Strobe	1.88			ns	12	5, 8
T24: T_{VAA}: Source Synchronous Address Output Valid After Strobe	1.88			ns	12	5, 9
T25: T_{SUSS}: Source Synchronous Input Setup Time to Strobe	0.21			ns	12, 13	6
T26: T_{HSS}: Source Synchronous Input Hold Time to Strobe	0.21			ns	12, 13	6
T27: T_{SUCC}: Source Synchronous Input Setup Time to BCLK[1:0]	0.65			ns	12, 13	7
T28: T_{FASS}: First Address Strobe to Second Address Strobe		1/2		BCLK	12	10
T29: T_{FDSS}: First Data Strobe to Subsequent Strobes		n/4		BCLK	13	11, 12
T30: Data Strobe ‘n’ (DSTBN#) Output valid Delay	8.80		10.20	ns	13	13
T31: Address Strobe Output Valid Delay	2.27		4.23	ns	12	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies and cache sizes.
2. Not 100% tested. Specified by design characterization.
3. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced to GTLREF at the processor core.
4. Unless otherwise noted these specifications apply to both data and address timings.
5. Valid delay timings for these signals are specified into the test circuit described in Figure 6 and with GTLREF at 2/3 V_{CC} ± 2%.
6. Specification is for a minimum swing defined between AGTL+ V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.3 V/ns to 4.0V/ns.
7. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
8. This specification represents the minimum time the data or address will be valid before its strobe. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for more information on the definitions and use of these specifications.
9. This specification represents the minimum time the data or address will be valid after its strobe. Refer to the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide* for more information on the definitions and use of these specifications.
10. The rising edge of ADSTB# must occur approximately 1/2 BCLK period (5 ns) after the falling edge of ADSTB#.
11. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
12. The second data strobe (falling edge of DSTBn#) must come approximately 1/4 BCLK period (2.5 ns) after the first falling edge of DSTBp#. The third data strobe (falling edge of DSTBp#) must come approximately 2/4 BCLK period (5 ns) after the first falling edge of DSTBp#. The last data strobe (falling edge of DSTBn#) must come approximately 3/4 BCLK period (7.5 ns) after the first falling edge of DSTBp#.
13. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.

Table 17. Asynchronous GTL+ Signals AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes[1,2,3,6]
T35: Asynch GTL+ Input Pulse Width, except PWRGOOD	2		BCLKs		
T36: PWRGOOD to RESET# de-assertion time	1	10	ms	14	
T37: PWRGOOD Inactive Pulse Width	10		BCLKs	14	4
T38: PROCHOT# pulse width	TBD		µs	15	5
T39: THERMTRIP# to V_{CC} Removal		0.5	s		
T40: FERR# Valid Delay from STPCLK# Deassertion	0	5	BCLKs	19	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timings for the Asynch GTL+ signals are referenced to the BCLK0 rising edge at Crossing Voltage. All Asynch GTL+ signal timings are referenced at GTLREF.
3. These signals may be driven asynchronously.
4. Refer to the PWRGOOD definition for more details regarding the behavior of this signal.
5. Length of assertion for PROCHOT# does not equal internal clock modulation time. Time is allocated after the assertion and before the deassertion of PROCHOT# for the processor to complete current instruction execution.
6. See Section 7.2 for additional timing requirements for entering and leaving the low power states.

Table 18. System Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes
T45: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Setup Time	4		BCLKs	11	1
T46: Reset Configuration Signals (A[31:3]#, BR0#, INIT#, SMI#) Hold Time	2	20	BCLKs	11	2

NOTES:
1. Before the deassertion of RESET#.
2. After clock that deasserts RESET#.

Table 19. TAP Signals AC Specifications

Parameter	Min	Max	Unit	Figure	Notes[1,2,3]
T55: TCK Period	60.0		ns	7	
T56: TCK Rise Time		10.0	ns	7	4
T57: TCK Fall Time		10.0	ns	7	4
T58: TMS Rise Time		8.5	ns	7	4
T59: TMS Fall Time		8.5	ns	7	4, 9
T61: TDI Setup Time	0.0		ns	20	5, 7
T62: TDI Hold Time	3		ns	20	5, 7
T63: TDO Clock to Output Delay		3.5	ns	20	6
T64: TRST# Assert Time	2		TCK	16	8, 9

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.

3. All AC timings for the TAP signals are referenced to the TCK signal at 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced to 0.5 * V_{CC} at the processor pins.
4. Rise and fall times are measured from the 20% to 80% points of the signal swing.
5. Referenced to the rising edge of TCK.
6. Referenced to the falling edge of TCK.
7. Specifications for a minium swing defined between TAP V_{T-} to V_{T+}. This assumes a minimum edge rate of 0.5 V/ns
8. TRST# must be held asserted for 2 TCK periods to be guaranteed that it is recognized by the processor.
9. It is recommended that TMS be asserted while TRST# is being deasserted.

Table 20. ITPCLKOUT[1:0] AC Specifications

Parameter	Min	Typ	Max	Unit	Figure	Notes[1,2]
T65: ITPCLKOUT Delay	400		560	ps	18	3
T66: Slew Rate	2		8	V/ns		
T67: ITPCLKOUT[1:0] High Time	3.89	5	6.17	ns		
T68: ITPCLKOUT[1:0] Low Time	3.89	5	6.17	ns		

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. These parameters are not tested and are based on design simulations.
3. This delay is from rising edge of BCLK0 to the falling edge of ITPCLK0.

2.14 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 14 through Table 19.

Note: For Figure 7 through Figure 16, the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced to GTLREF at the processor core.

2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) to GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced to GTLREF at the processor core silicon.

3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor core silicon.

4. All AC timings for the TAP signals are referenced to the TCK signal to 0.5 * V_{CC} at the processor pins. All TAP signal timings (TMS, TDI, etc) are referenced to 0.5 * V_{CC} at the processor pins.

The circuit used to test the AC specifications is shown in Figure 6.

Figure 6. AC Test Circuit

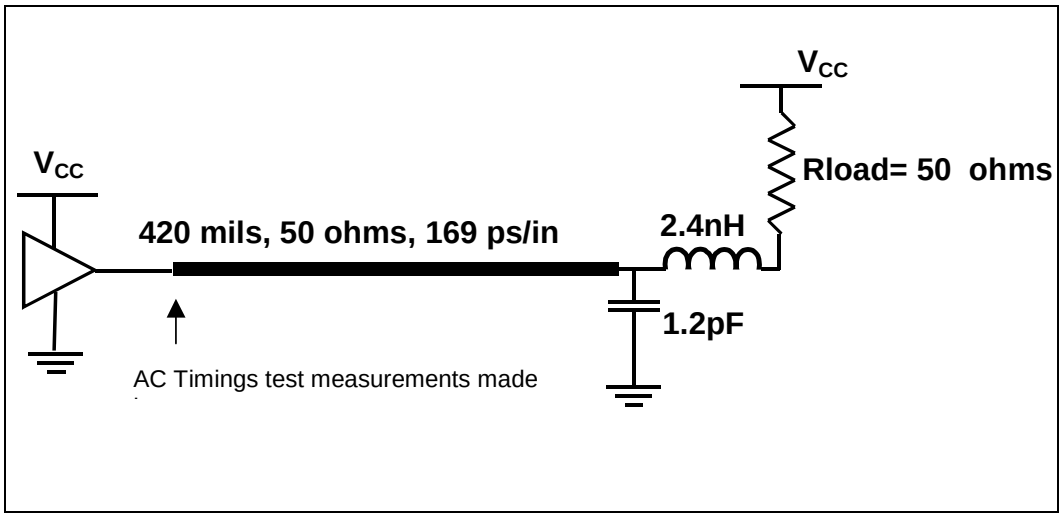


Figure 7. TCK Clock Waveform

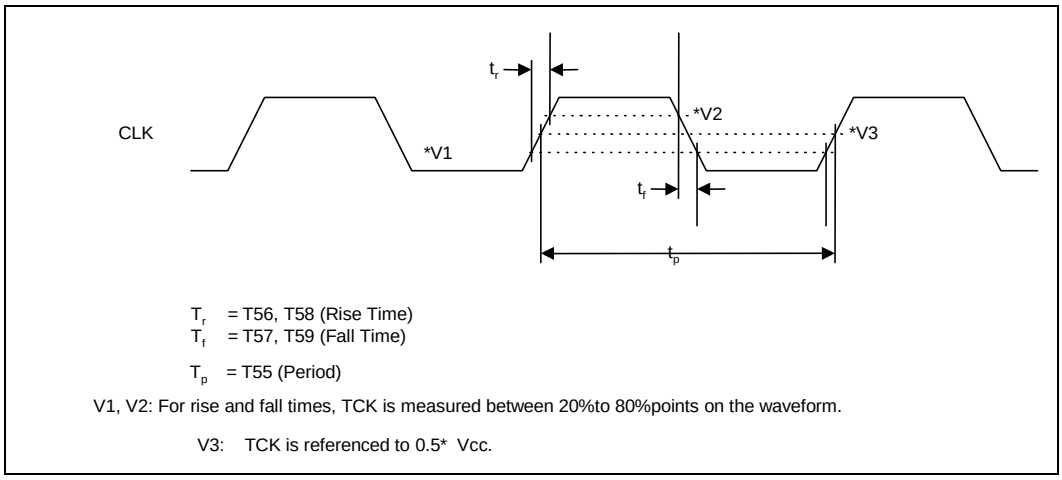
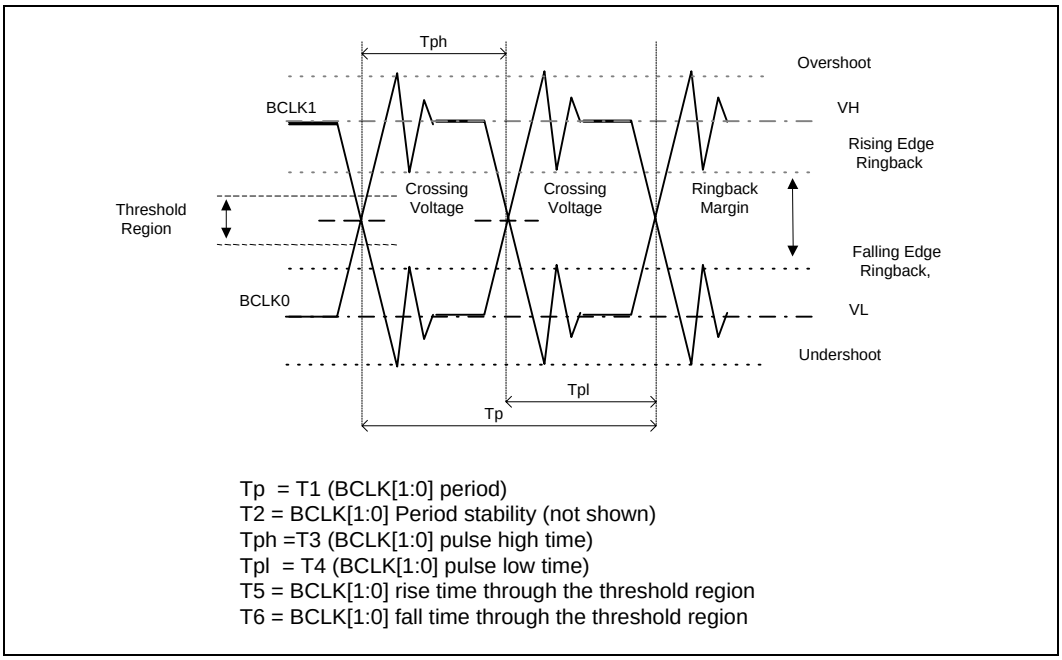


Figure 8. Differential Clock Waveform



Tp = T1 (BCLK[1:0] period)
T2 = BCLK[1:0] Period stability (not shown)
Tph =T3 (BCLK[1:0] pulse high time)
Tpl = T4 (BCLK[1:0] pulse low time)
T5 = BCLK[1:0] rise time through the threshold region
T6 = BCLK[1:0] fall time through the threshold region

Figure 9. Differential Clock Crosspoint Specification

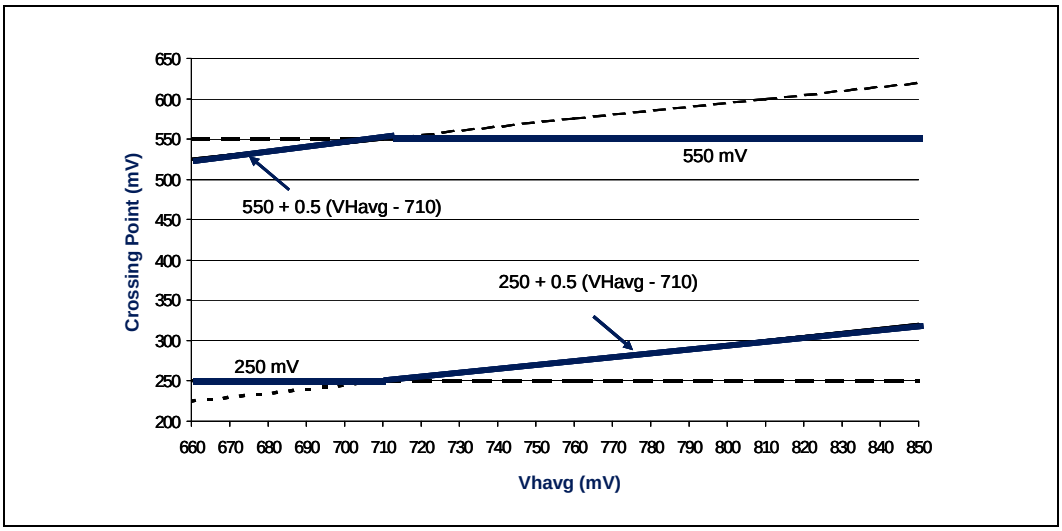


Figure 10. System Bus Common Clock Valid Delay Timings

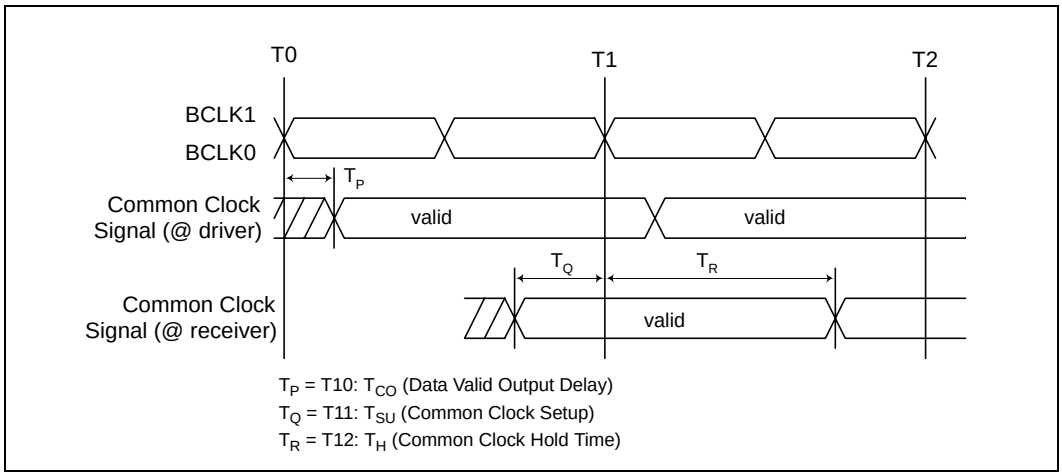


Figure 11. System Bus Reset and Configuration Timings

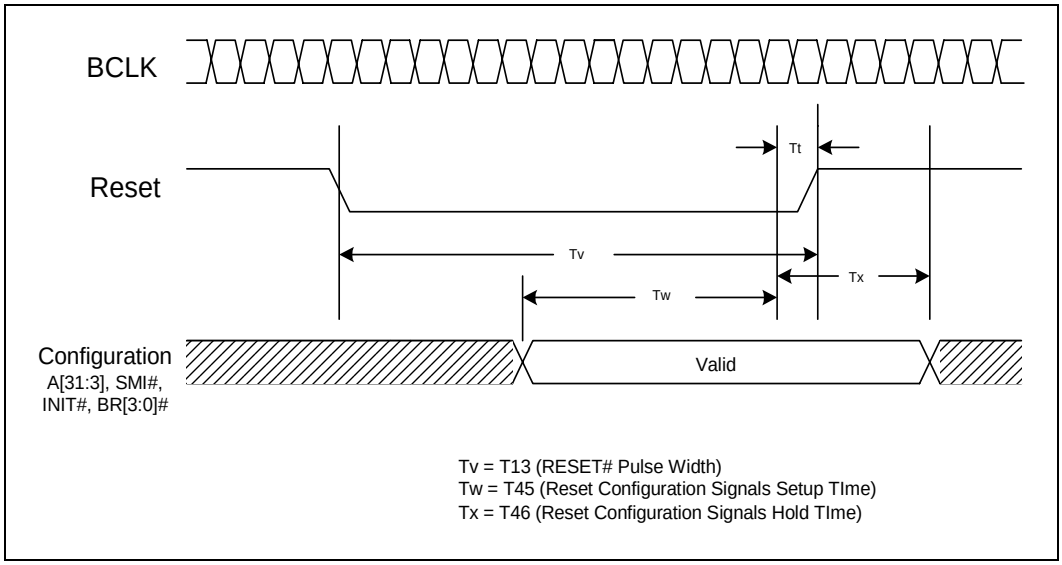
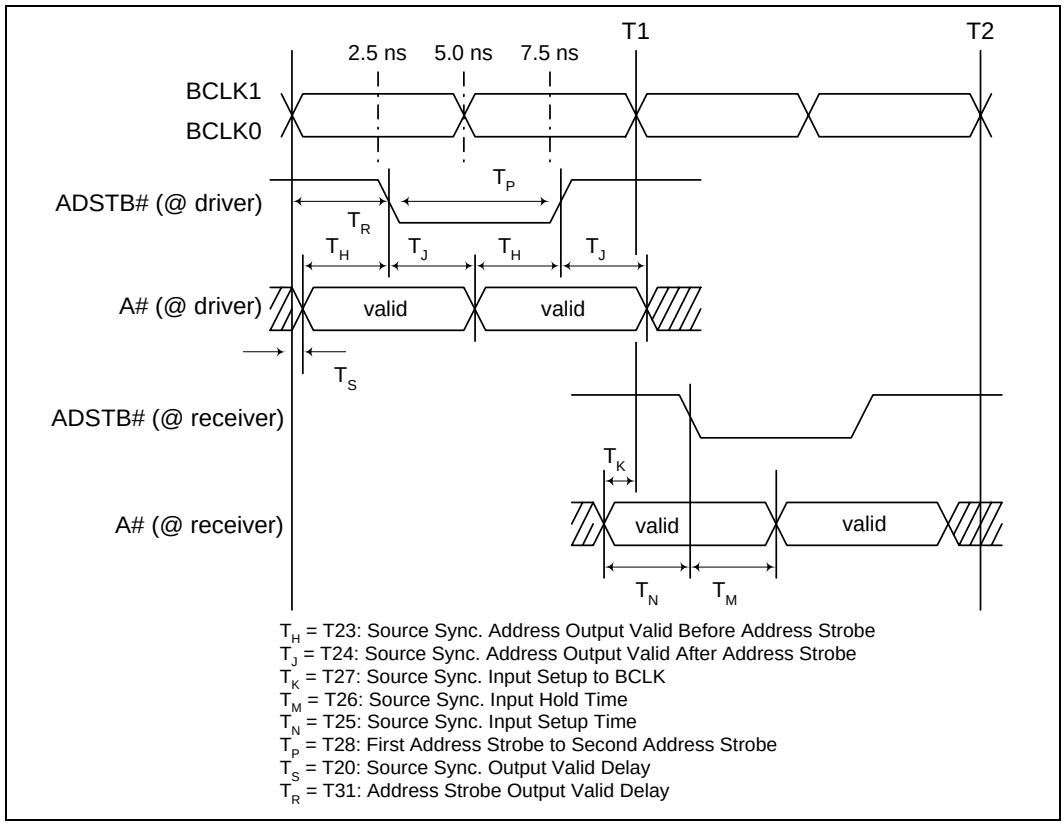
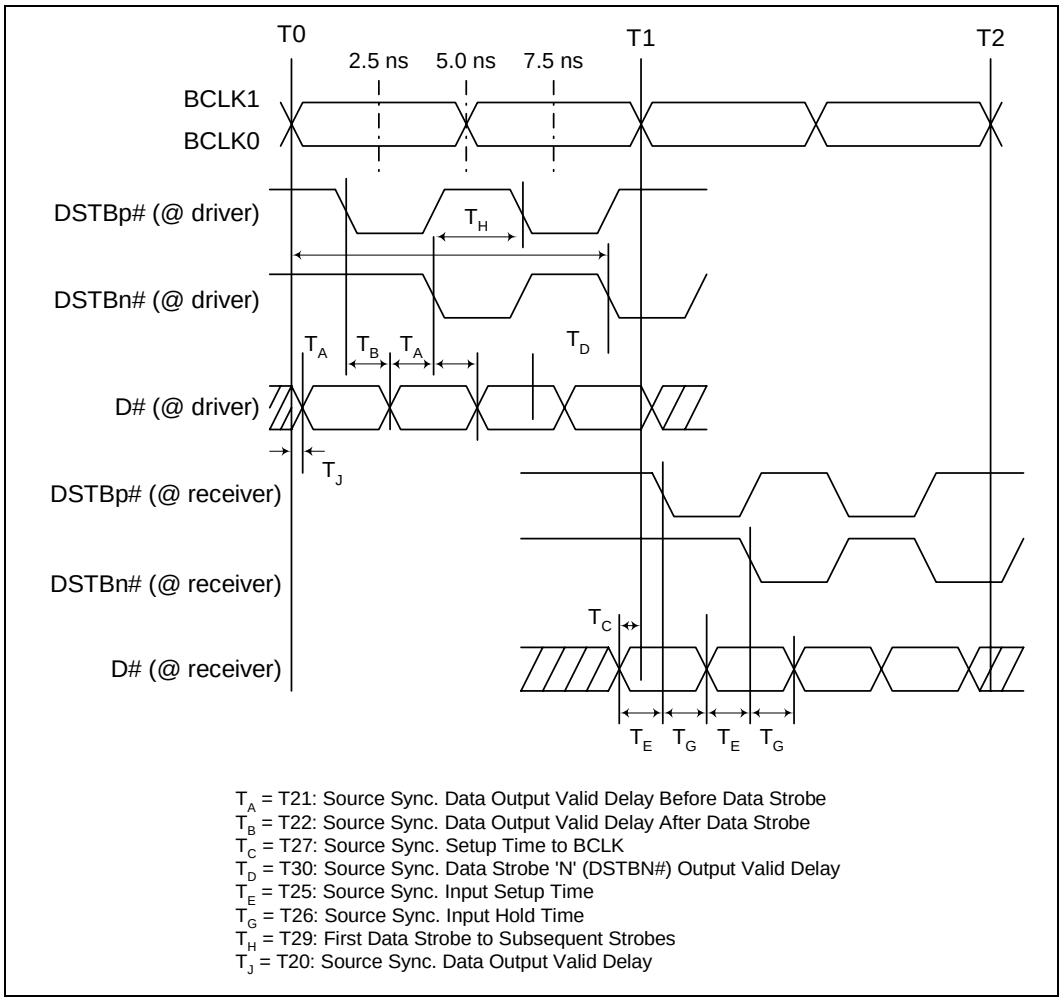


Figure 12. Source Synchronous 2X (Address) Timings



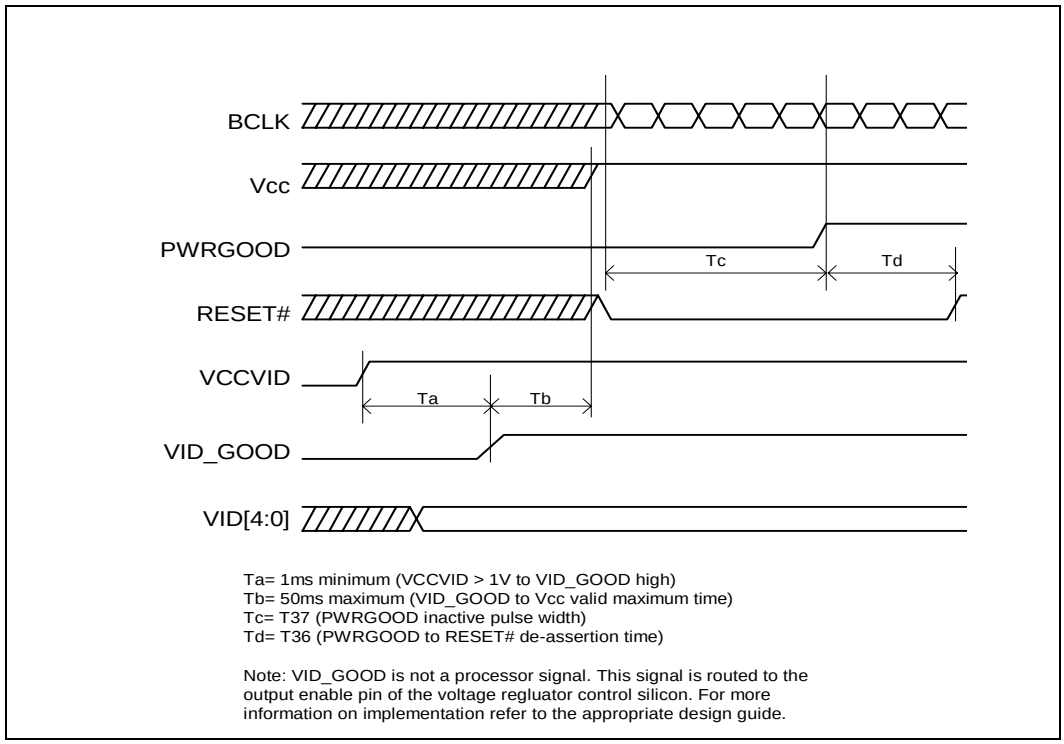
T_H = T23: Source Sync. Address Output Valid Before Address Strobe
T_J = T24: Source Sync. Address Output Valid After Address Strobe
T_K = T27: Source Sync. Input Setup to BCLK
T_M = T26: Source Sync. Input Hold Time
T_N = T25: Source Sync. Input Setup Time
T_P = T28: First Address Strobe to Second Address Strobe
T_S = T20: Source Sync. Output Valid Delay
T_R = T31: Address Strobe Output Valid Delay

Figure 13. Source Synchronous 4X (Data) Timings



T_A = T21: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T22: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T27: Source Sync. Setup Time to BCLK
T_D = T30: Source Sync. Data Strobe 'N' (DSTBN#) Output Valid Delay
T_E = T25: Source Sync. Input Setup Time
T_G = T26: Source Sync. Input Hold Time
T_H = T29: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

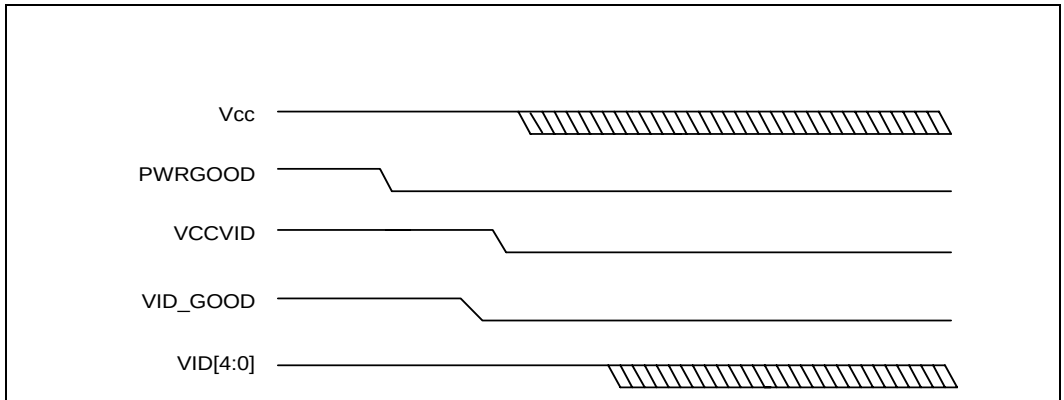
Figure 14. Power Up Sequence



Ta= 1ms minimum (VCCVID > 1V to VID_GOOD high)
Tb= 50ms maximum (VID_GOOD to Vcc valid maximum time)
Tc= T37 (PWRGOOD inactive pulse width)
Td= T36 (PWRGOOD to RESET# de-assertion time)

Note: VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regluator control silicon. For more information on implementation refer to the appropriate design guide.

Figure 15. Power Down Sequence



Note: VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regluator control silicon. For more information on implementation refer to the appropriate design guide.

1. This timing diagram is not intended to show specific times. Instead a general ordering of events with respect to time should be observed.
2. When VCCVID is less than 1V, VID_GOOD must be low.
3. Vcc must be disabled before VID[4:0] becomes invalid.

Figure 16. Test Reset Timings

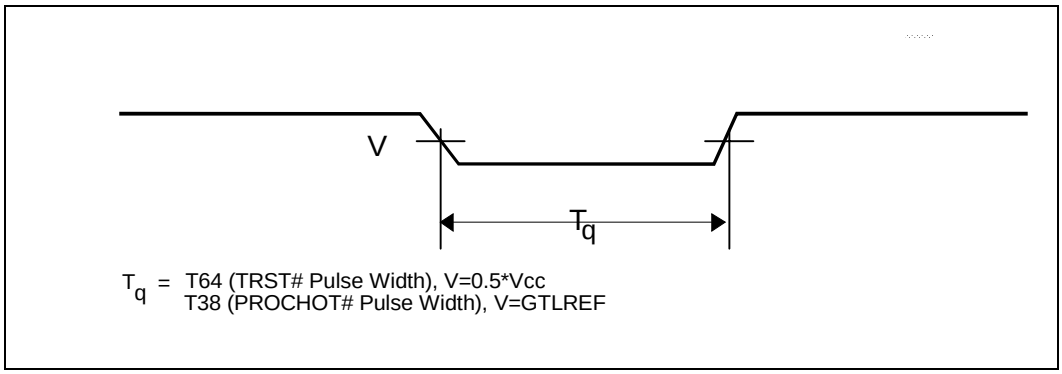


Figure 17. THERMTRIP# Power Down Sequence

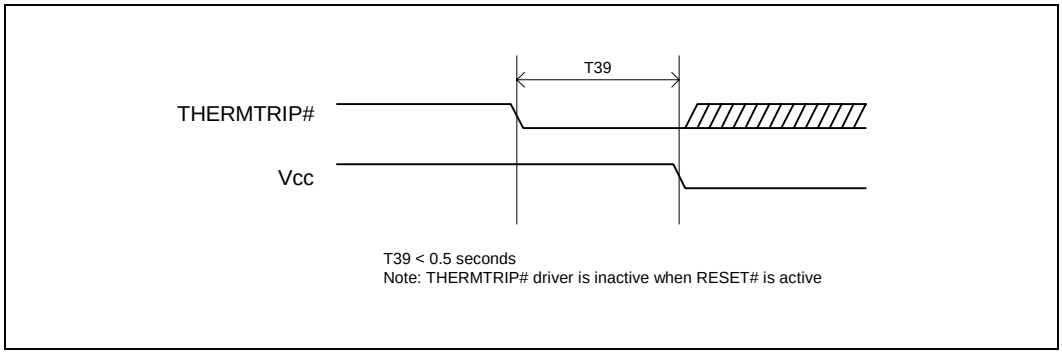


Figure 18. ITPCLKOUT Valid Delay Timing

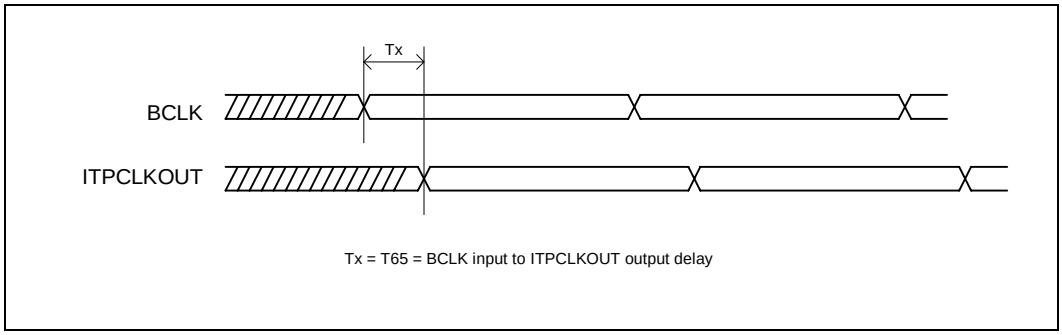
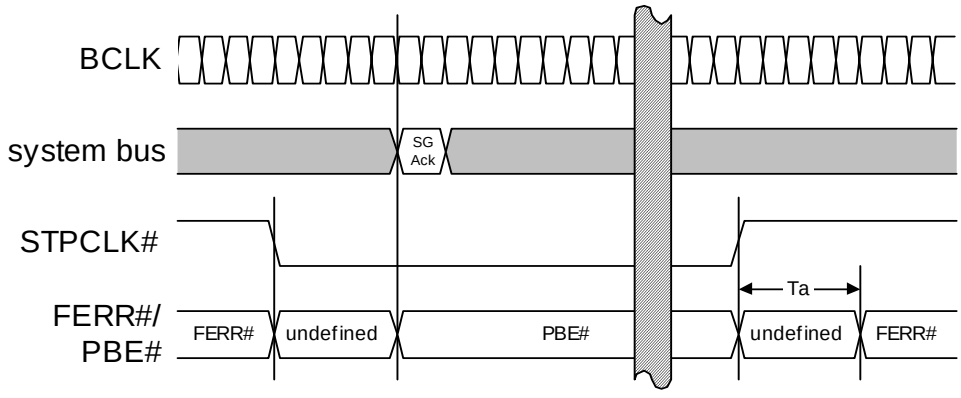


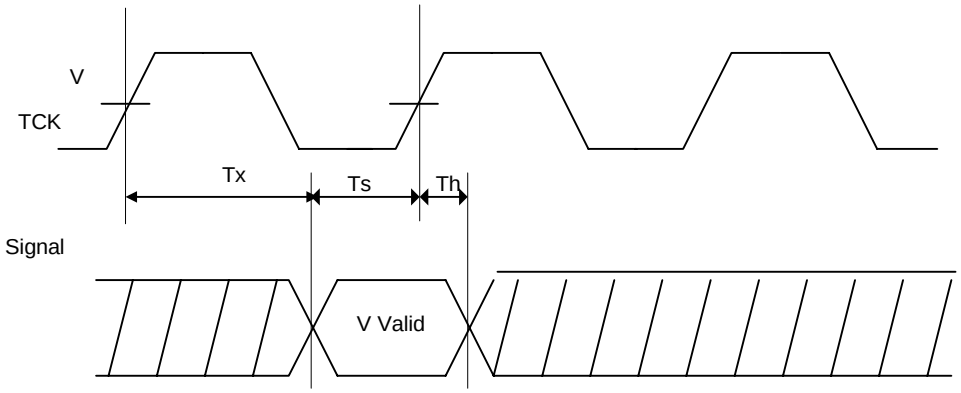
Figure 19. FERR#/PBE# Timings



Ta = T40 (FERR# Valid Delay from STPCLK# Deassertion)

Note: FERR#/PBE# is undefined from STPCLK# assertion until the stop grant acknowledge is driven on the processor system bus. FERR#/PBE# is also undefined for a period of Ta from STPCLK# deassertion. Inside these undefined regions the PBE# signal is driven. FERR# is driven at all other times.

Figure 20. TAP Valid Delay Timing Waveform



Tx = T63 (Valid Time)
Ts = T61 (Setup Time)
Th = T62 (Hold Time)
V = 0.5 * Vcc

3.0 System Bus Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, overshoot and undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects. For these reasons, it is important that the designer work to achieve a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation and for interpreting results for signal quality measurements of actual designs. The Intel® Pentium® 4 processor with 512KB L2 cache *Overshoot Checker Tool* should be utilized to determine pass/fail signal quality conditions found through simulation analysis with the *Intel® Pentium® 4 processor with 512KB L2 cache I/O Buffer Models (IBIS format).* This tool takes into account the specifications contained in this section.

3.1 System Bus Clock (BCLK) Signal Quality Specifications

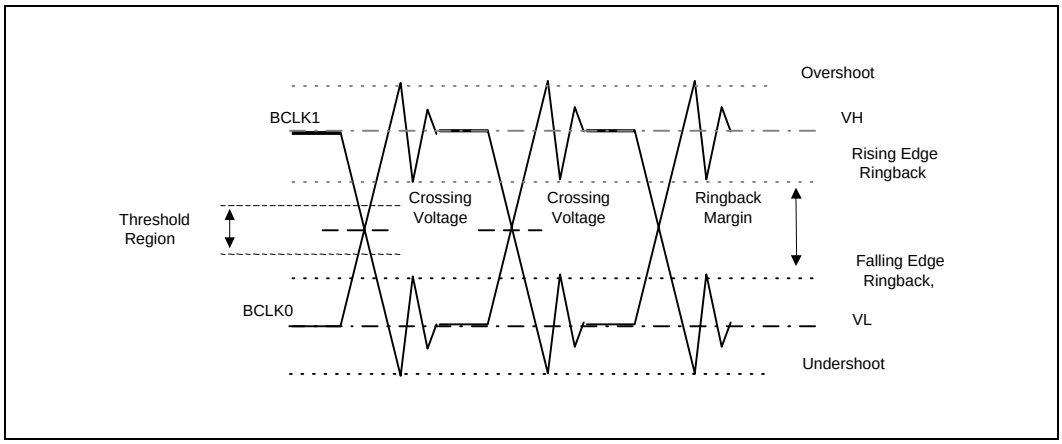
Table 21 describes the signal quality specifications at the processor core silicon for the processor system bus clock (BCLK) signals. Figure 21 illustrates the signal quality waveform for the system bus clock at the processor core silicon.

Table 21. BCLK Signal Quality Specifications

Parameter	Min	Max	Unit	Figure	Notes[1]
BCLK[1:0] Overshoot	N/A	0.30	V	21	
BCLK[1:0] Undershoot	N/A	0.30	V	21	
BCLK[1:0] Ringback Margin	0.20	N/A	V	21	2
BCLK[1:0] Threshold Region	N/A	0.10	V	21	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage the BCLK signal can dip back to after passing the V_{IH} (rising) or V_{IL} (falling) voltage limits. This specification is an absolute value.

Figure 21. BCLK Signal Integrity Waveform



3.2 System Bus Signal Quality Specifications and Measurement Guidelines

Various scenarios have been simulated to generate a set of AGTL+ layout guidelines which are available in the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 850 Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package and Intel® 845 Chipset Platform Design Guide*.

Table 22 provides the signal quality specifications for all processor signals for use in simulating signal quality at the processor core silicon. The *Intel® Pentium® 4 processor with 512KB L2 cache Overshoot, Undershoot and Timing Validation Guidelines* will be available to assist in comparing specifications for signal quality at the processor core silicon with measurements taken at the processor pins.

Intel® Pentium® 4 processor with 512KB L2 cache maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 24 through Table 27. Figure 22 shows the system bus ringback tolerance for low-to-high transitions and Figure 23 shows ringback tolerance for high-to-low transitions.

Table 22. Ringback Specifications for AGTL+ and Asynchronous GTL+ Signals Groups.

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
All Signals	0 → 1	GTLREF + 10%	V	22	1,2,3,4,5,6,7
All Signals	1 → 0	GTLREF - 10%	V	23	1,2,3,4,5,6,7

NOTES:
1. All signal integrity specifications are measured at the processor silicon.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Specifications are for the edge rate of 0.3 - 4.0V/ns.
4. All values specified by design characterization.
5. Please see Section 3.3 for maximum allowable overshoot duration.
6. Ringback between GTLREF + 10% and GTLREF - 10% is not supported.

7. Intel recommends simulations not exceed a ringback value of GTLREF +/- 200 mV to allow margin for other sources of system noise.

Table 23. Ringback Specifications for TAP Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
All Signals	0 → 1	Vt+(max) TO Vt-(max)	V	24	1,2,3,4
All Signals	1 → 0	Vt-(min) TO Vt+(min)	V	25	1,2,3,4

NOTES:
1. All signal integrity specifications are measured at the processor silicon.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Please see Section 3.3 for maximum allowable overshoot.
4. Please see Section 2.11 for the DC specifications.

Figure 22. Low-to-High System Bus Receiver Ringback Tolerance

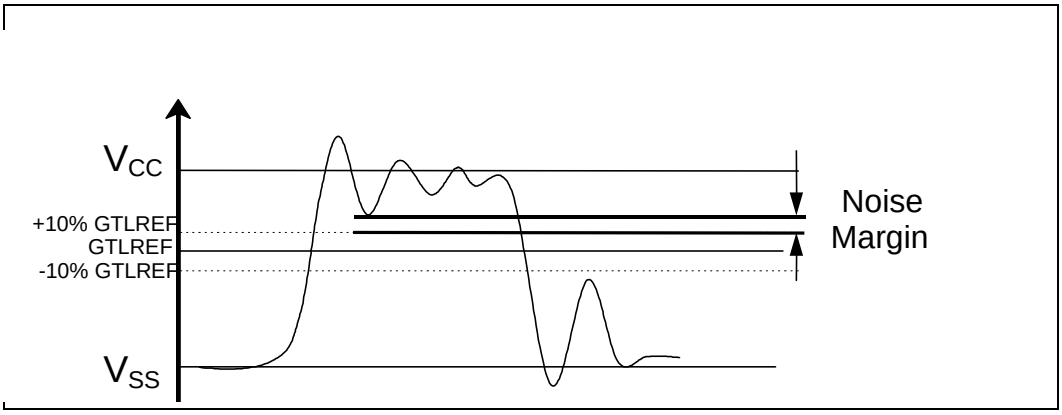


Figure 23. High-to-Low System Bus Receiver Ringback Tolerance

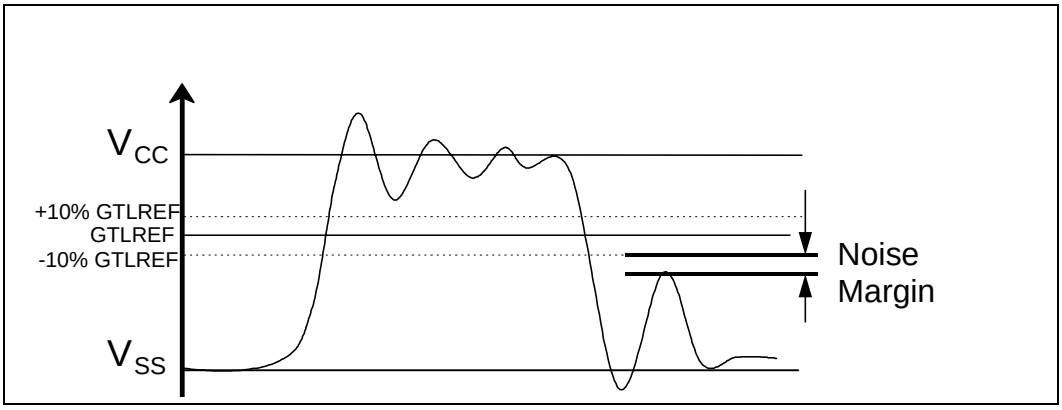


Figure 24. Low-to-High System Bus Receiver Ringback Tolerance for TAP Buffers

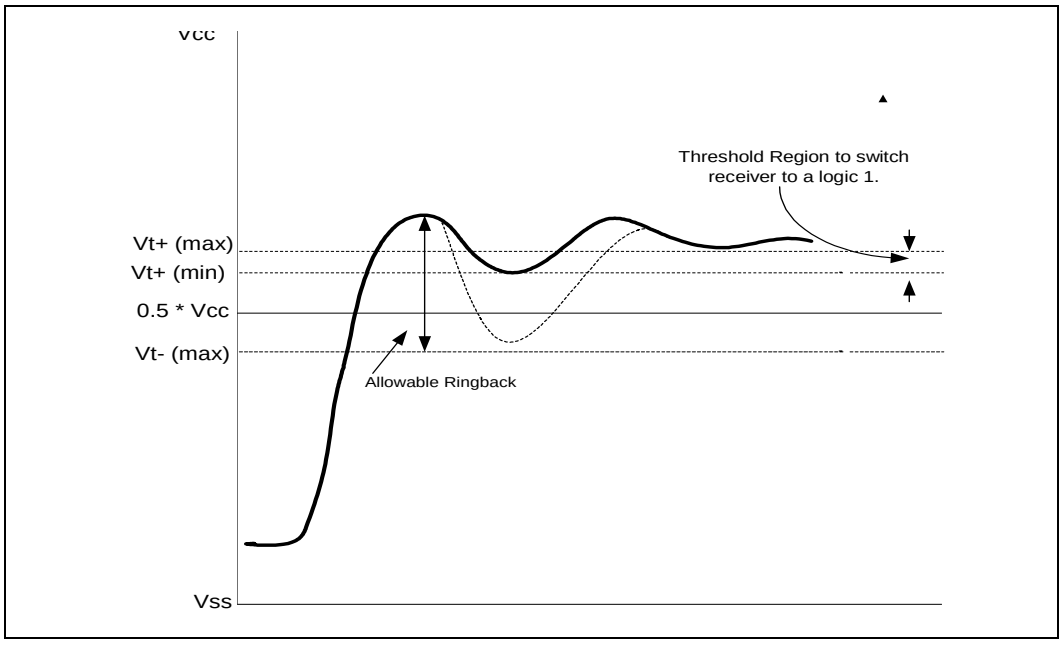
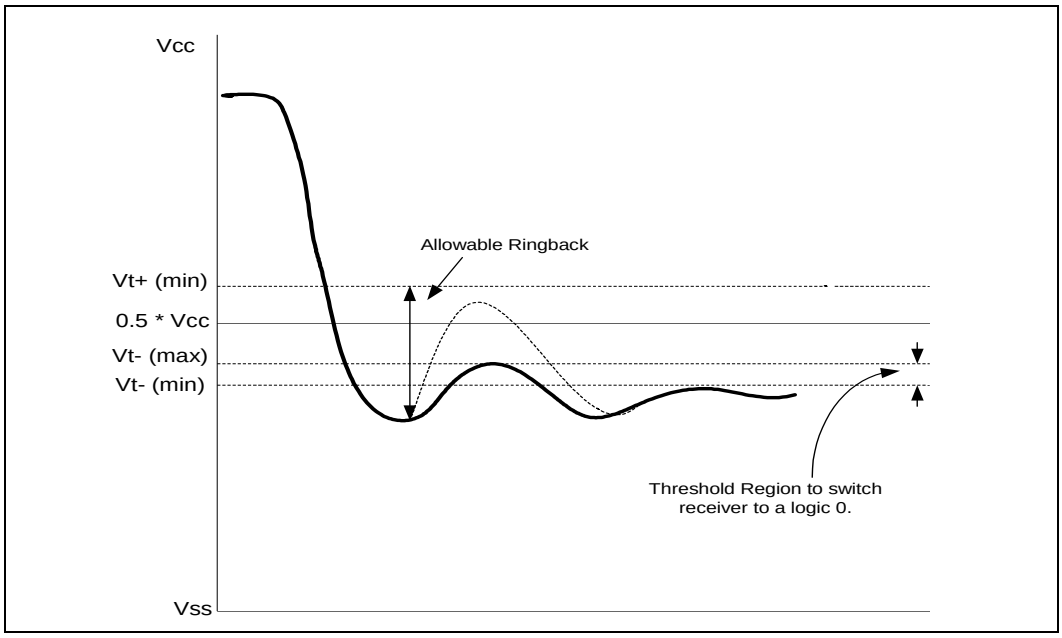


Figure 25. High-to-Low System Bus Receiver Ringback Tolerance for TAP Buffers



3.3 System Bus Signal Quality Specifications and Measurement Guidelines

3.3.1 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage (or below V_{SS}) as shown in Figure 26. The overshoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine the impact of overshoot and undershoot events, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the processor system bus, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

3.3.2 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the Intel® Pentium® 4 processor with 512KB L2 cache both are referenced to V_{SS}. It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

Overshoot/undershoot magnitude levels must observe the absolute maximum specifications listed in Table 24 through Table 27. These specifications must not be violated at any time regardless of bus activity or system state. Within these specifications are threshold levels that define different allowed pulse durations. Provided that the magnitude of the overshoot/undershoot is within the absolute maximum specifications, the pulse magnitude, duration and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.3.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total time an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage (maximum overshoot = 1.800 V, maximum undershoot = -0.335 V). The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/ undershoot event may need to be measured to determine the total pulse duration.

Note 1: Oscillations below the reference voltage can not be subtracted from the total overshoot/undershoot pulse duration.

3.3.4 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs EVERY OTHER clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge, since the highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. An AF = 1 indicates that the specific overshoot (undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 24 through Table 27 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note 1: Activity factor for AGTL+ signals is referenced to BCLK[1:0] frequency.

Note 2: Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.

Note 3: Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]# and DSTBN[3:0]#.

3.3.5 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot (as measured above V_{CC}) and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* a particular signal falls into. If the signal is an AGTL+ signal operating in the common clock domain, use Table 26. For AGTL+ signals operating in the 2x source synchronous domain, use Table 25. For AGTL+ signals operating in the 4x source synchronous domain, use Table 24. Finally, all other signals reside in the 100MHz domain (asynchronous GTL+, TAP, etc.) and are referenced in Table 27.
2. Determine the *magnitude* of the overshoot (relative to V_{SS})
3. Determine the *activity factor* (how often does this overshoot occur?)
4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

The above procedure is similar for undershoot after the undershoot waveform has been converted to look like an overshoot. Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.3.6 Conformance Determination to Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF, and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. Ensure no signal ever exceeds V_{CC} or -0.25V OR
2. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables OR
3. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

The following notes apply to Table 24 through Table 27.

NOTES:
1. Absolute Maximum Overshoot magnitude of 1.80V must never be exceeded.
2. Absolute Maximum Overshoot is measured relative to V_{SS}, Pulse Duration of overshoot is measured relative to V_{CC}.
3. Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to V_{CC}.
4. Ringback below V_{CC} can not be subtracted from overshoots/undershoots. Lesser undershoot does not allocate longer or larger overshoot.
5. OEM's are strongly encouraged to follow Intel provided layout guidelines.
6. All values specified by design characterization.

Table 24. Source Synchronous (400MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
1.800	-0.335	0.02	0.19	1.91	
1.750	-0.285	0.04	0.54	5.00	
1.700	-0.235	0.10	1.56	5.00	
1.650	-0.185	0.29	4.51	5.00	
1.600	-0.135	0.87	5.00	5.00	
1.550	-0.085	3.05	5.00	5.00	

NOTES:

1. These specifications are measured at the processor core silicon.
2. BCLK period is 10 ns.

Table 25. Source Synchronous (200MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
1.800	-0.335	0.03	0.29	3.83	
1.750	-0.285	0.07	0.70	10.00	
1.700	-0.235	0.20	2.00	10.00	
1.650	-0.185	0.58	5.80	10.00	
1.600	-0.135	1.74	10.00	10.00	
1.550	-0.085	6.10	10.00	10.00	

NOTES:
1. These specifications are measured at the processor core silicon.
2. BCLK period is 10 ns.

Table 26. Common Clock (100MHz) AGTL+ Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
1.800	-0.335	0.06	0.584	7.66	
1.750	-0.285	0.14	1.40	20.00	
1.700	-0.235	0.40	4.00	20.00	
1.650	-0.185	1.16	11.60	20.00	
1.600	-0.135	3.48	20.00	20.00	
1.550	-0.085	12.20	20.00	20.00	

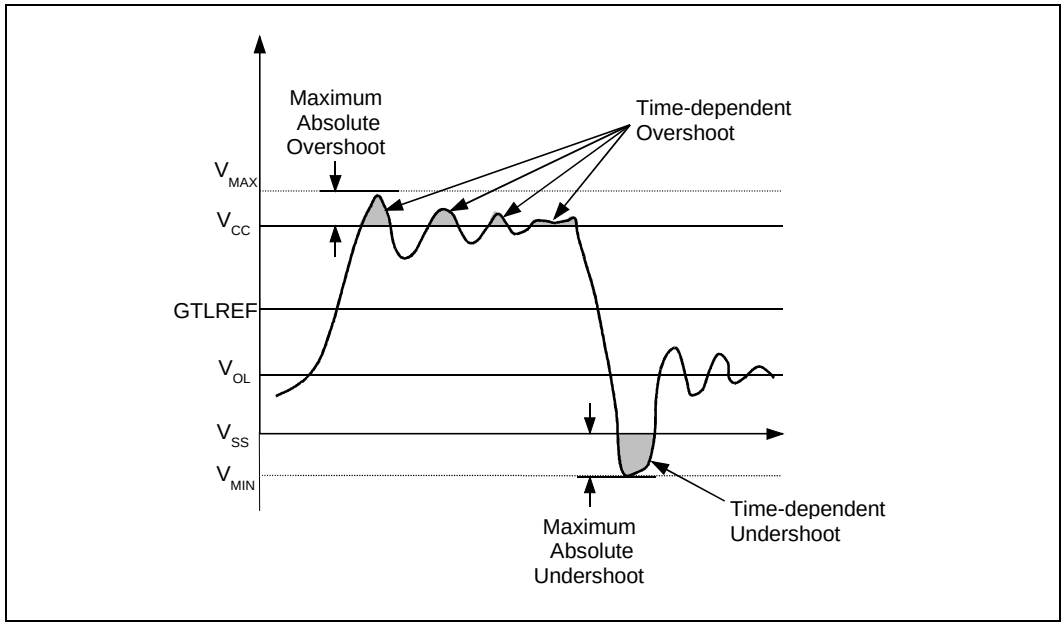
NOTES:
1. These specifications are measured at the processor core silicon.
2. BCLK period is 10 ns.

Table 27. Asynchronous GTL+ and TAP Signal Groups Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1	Pulse Duration (ns) AF = 0.01	Notes [1,2]
1.800	-0.335	0.18	1.75	22.98	
1.750	-0.285	0.42	4.20	60.00	
1.700	-0.235	1.20	12.00	60.00	
1.650	-0.185	3.48	34.80	60.00	
1.600	-0.135	10.44	60.00	60.00	
1.550	-0.085	36.60	60.00	60.00	

NOTES:
1. These specifications are measured at the processor core silicon.
2. BCLK period is 10 ns.

Figure 26. Maximum Acceptable Overshoot/Undershoot Waveform



4.0 Package Mechanical Specifications

The Intel® Pentium® 4 processor with 512KB L2 cache is packaged in a Flip-Chip Pin Grid Array (FC-PGA2) package. Components of the package include an integrated heat spreader (IHS), processor die, and the substrate which is the pin carrier. Mechanical specifications for the processor are given in this section. See Section 1.1. for a terminology listing. The processor socket which accepts the Intel® Pentium® 4 processor with 512KB L2 cache is referred to as a 478-Pin micro PGA (mPGA478B) socket. See the *mPGA479, mPGA478A, mPGA478B, mPGA478C, and mPGA476 Socket Design Guidelines* for complete details on the mPGA478B socket.

NOTES: For Figure 27 through Figure 33, the following notes apply:

1. Unless otherwise specified, the following drawings are dimensioned in millimeters.
2. Figures and drawings labeled as “Reference Dimensions” are provided for informational purposes only. Reference dimensions are extracted from the mechanical design database and are nominal dimensions with no tolerance information applied. Reference dimensions are NOT checked as part of the processor manufacturing process. Unless noted as such, dimensions in parentheses without tolerances are reference dimensions.
3. Drawings are not to scale.

Note: The drawing below is not to scale and is for reference only. The socket and system board are supplied as a reference only.

Figure 27. Exploded View of Processor Components on a System Board

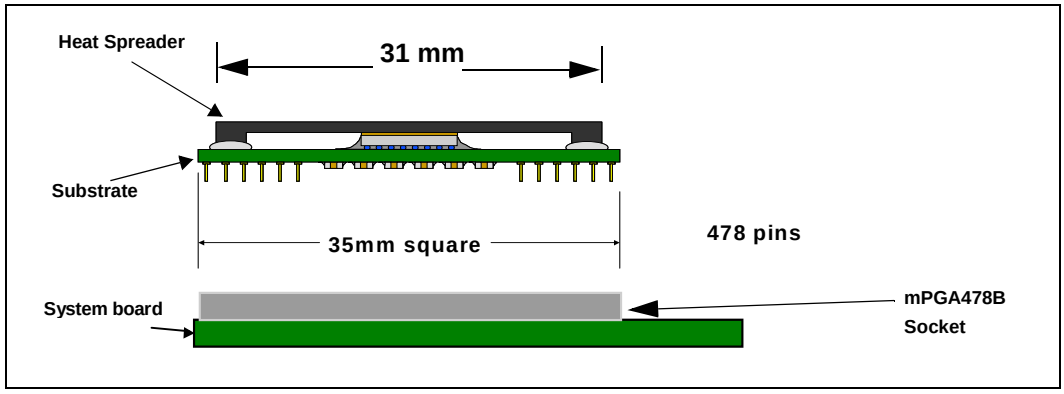


Figure 28. Intel®Pentium® 4 Processor Package

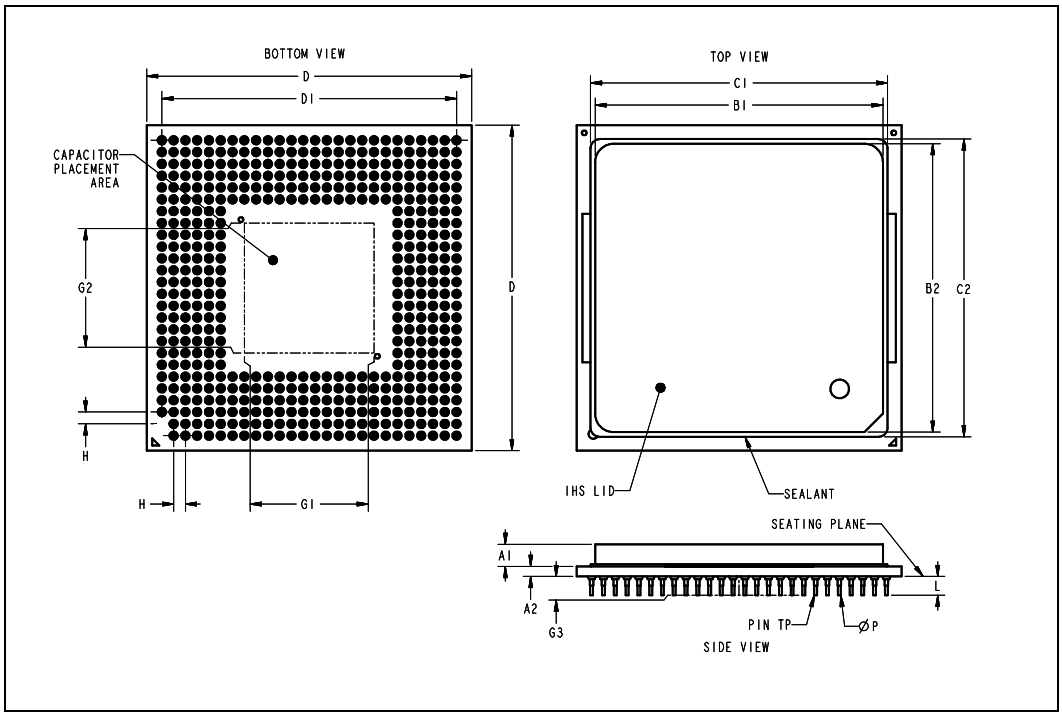


Table 28. Description Table for Processor Dimensions

Code Letter	Dimension (mm)			Notes
	Min	Nominal	Max	
A1	2.266	2.378	2.490	
A2	0.980	1.080	1.180	
B1	30.800	31.000	31.200	
B2	30.800	31.000	31.200	
C1			33.000	Includes Placement Tolerance
C2			33.000	Includes Placement Tolerance
D	34.900	35.000	35.100	
D1	31.500	31.750	32.000	
G1			13.970	Keep-In Zone Dimension
G2			13.970	Keep-In Zone Dimension
G3			1.250	Keep-In Zone Dimension
H		1.270		
L	1.950	2.030	2.110	
ϕP	0.280	0.305	0.330	
PIN TP			0.254	Diametric True Position (Pin-to-Pin)
IHS Flatness			0.05	

Figure 29 details the keep-in specification for pin-side components. The Intel® Pentium® 4 processor with 512KB L2 cache may contain pin side capacitors mounted to the processor package.

Figure 31 details the flatness and tilt specifications for the IHS. Tilt is measured with the reference datum set to the bottom of the processor susbstrate.

Figure 29. Processor Cross-Section and Keep-In

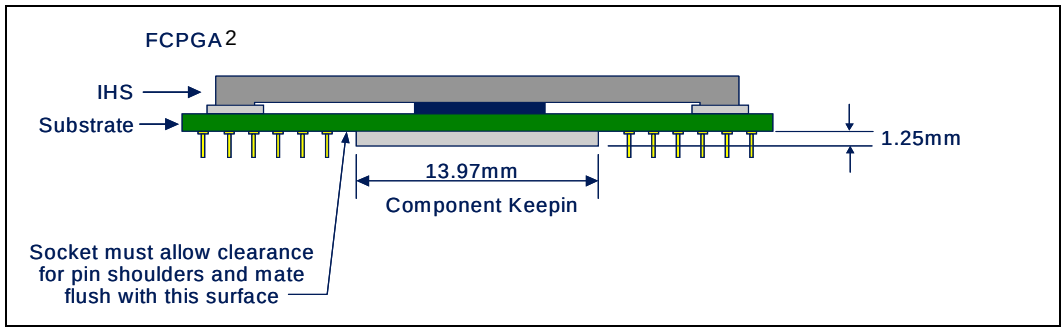
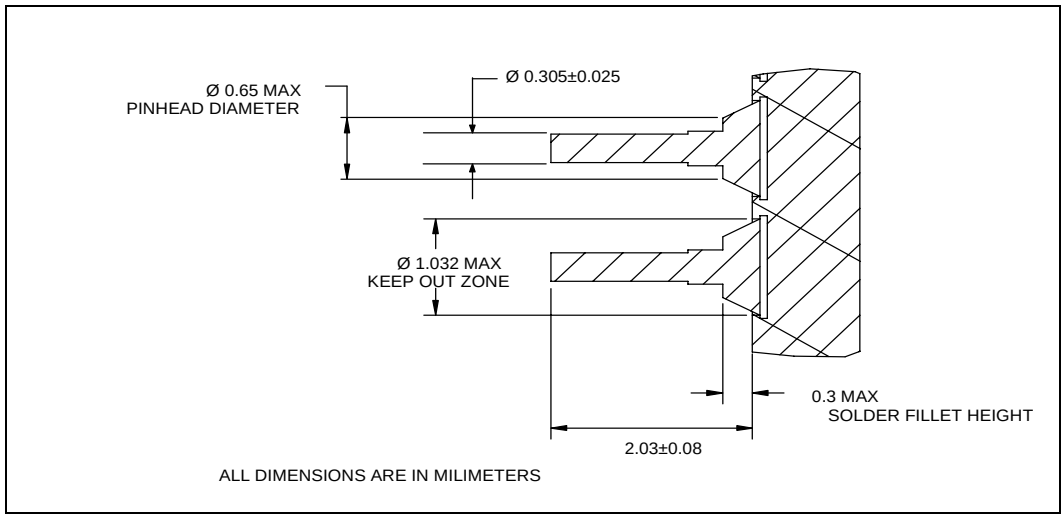
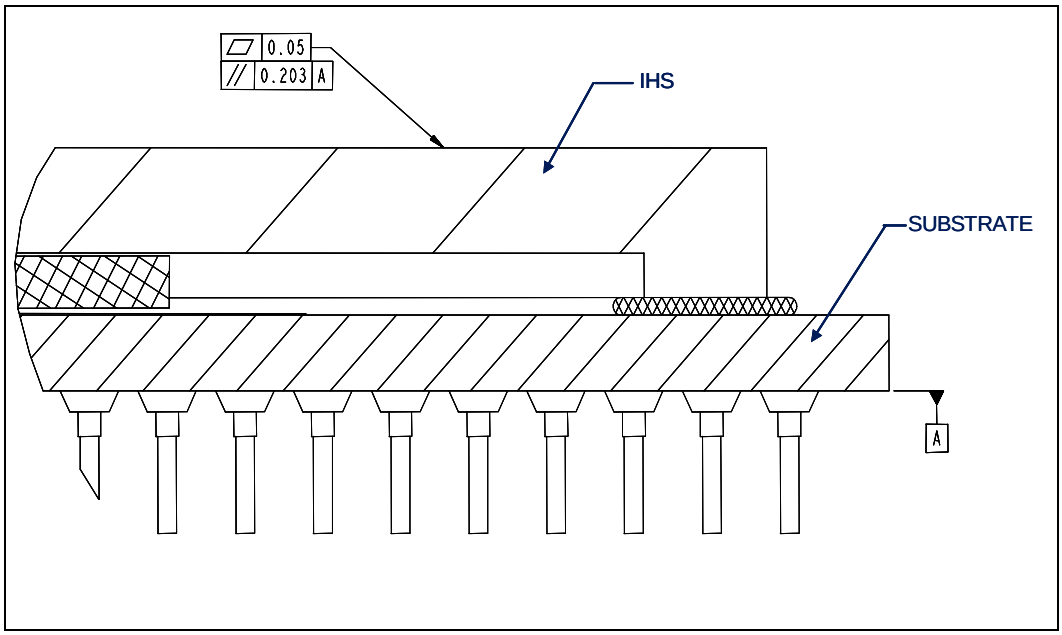


Figure 30. Processor Pin Detail



NOTES:
1. Pin plating consists of 0.2 micrometers Au over 2.0 micrometer Ni.
2. 0.254 mm diametric true position, pin to pin.

Figure 31. IHS Flatness Specification



NOTES:
1. Flatness is specific as overall, not per unit of length.
2. All Dimensions are in millimeters.

4.1 Package Load Specifications

Table 29 provides dynamic and static load specifications for the IHS. These mechanical load limits should not be exceeded during heatsink assembly, mechanical stress testing, or standard drop and shipping conditions. The heatsink attach solutions must not induce continuous stress onto the processor with the exception of a uniform load to maintain the heatsink-to-processor thermal interface contact. It is not recommended to use any portion of the processor substrate as a mechanical reference or load bearing surface for thermal solutions.

Table 29. Package Dynamic and Static Load Specifications

Parameter	Max	Unit	Notes
Static	100	lbf	1, 2, 3
Dynamic	200	lbf	1, 3, 4

NOTES:
1. This specification applies to a uniform compressive load.
2. This is the maximum static force that can be applied by the heatsink and clip to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization.
4. Dynamic loading specifications are defined assuming a maximum duration of 11ms and 200 lbf is achieved by superimposing a 100 lbf dynamic load (1 lbm heatsink at 50g) on the static compressive load.

4.2 Processor Insertion Specifications

The Intel® Pentium® 4 processor with 512KB L2 cache can be inserted and removed 15 times from a mPGA478B socket meeting the *mPGA479, mPGA478A, mPGA478B, mPGA478C, and mPGA476 Socket Design Guidelines* document.

4.3 Processor Mass Specifications

Table 30 specifies the processor's mass. This includes all components which make up the entire processor product.

Table 30. Processor Mass

Processor	Mass (grams)
Intel® Pentium® 4 processor with 512KB L2 cache	19

4.4 Processor Materials

The Intel® Pentium® 4 processor with 512KB L2 cache is assembled from several components. The basic material properties are described in Table 31.

Table 31. Processor Material Properties

Component	Material	Notes
Integrated Heat Spreader	Nickel over copper or copper	
Substrate	Fiber-reinforced resin	
Substrate pins	Gold over nickel	

4.5 Processor Markings

The following section details the processor top-side markings and is provided to aid in the identification of the Intel® Pentium® 4 processor with 512KB L2 cache.

Figure 32. Processor Markings

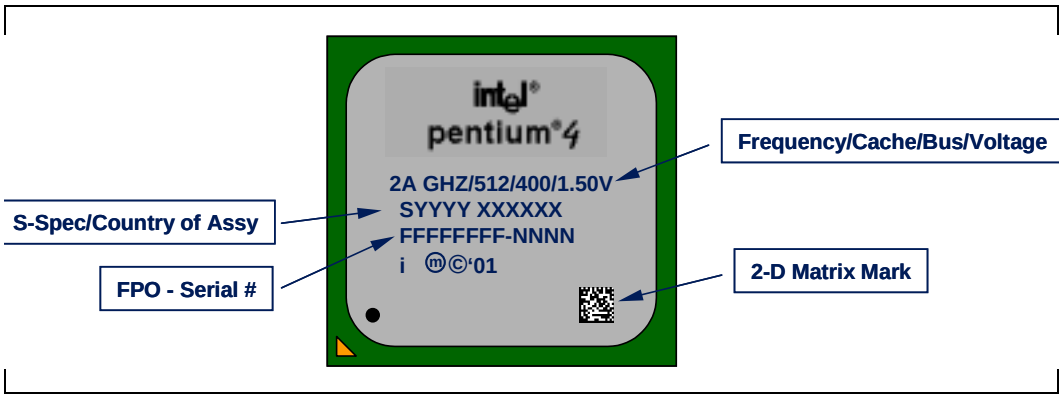
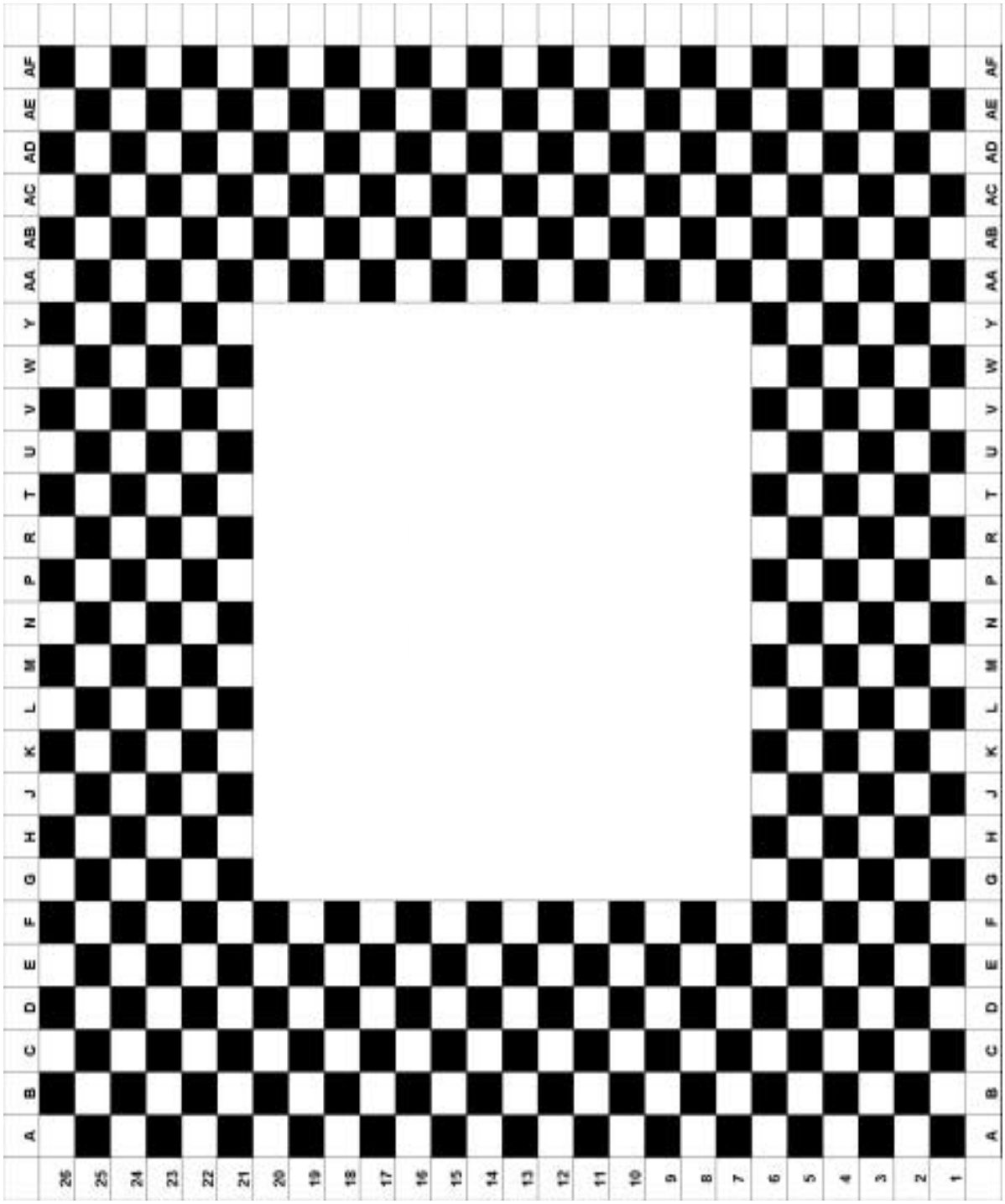


Figure 33. Coordinates of the processor pins as viewed from the top of the package.



5.0 Pin Listing and Signal Definitions

5.1 Intel®Pentium® 4 Processor Pin Assignments

Section 5.1 contains the pinlist for the Intel® Pentium® 4 processor with 512KB L2 cache in Table 32 and Table 33. Table 32 is a listing of all processor pins ordered alphabetically by pin name. Table 33 is also a listing of all processor pins but ordered by pin number.

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A03#	K2	Source Synch	Input/Output
A04#	K4	Source Synch	Input/Output
A05#	L6	Source Synch	Input/Output
A06#	K1	Source Synch	Input/Output
A07#	L3	Source Synch	Input/Output
A08#	M6	Source Synch	Input/Output
A09#	L2	Source Synch	Input/Output
A10#	M3	Source Synch	Input/Output
A11#	M4	Source Synch	Input/Output
A12#	N1	Source Synch	Input/Output
A13#	M1	Source Synch	Input/Output
A14#	N2	Source Synch	Input/Output
A15#	N4	Source Synch	Input/Output
A16#	N5	Source Synch	Input/Output
A17#	T1	Source Synch	Input/Output
A18#	R2	Source Synch	Input/Output
A19#	P3	Source Synch	Input/Output
A20#	P4	Source Synch	Input/Output
A21#	R3	Source Synch	Input/Output
A22#	T2	Source Synch	Input/Output
A23#	U1	Source Synch	Input/Output
A24#	P6	Source Synch	Input/Output
A25#	U3	Source Synch	Input/Output
A26#	T4	Source Synch	Input/Output
A27#	V2	Source Synch	Input/Output
A28#	R6	Source Synch	Input/Output
A29#	W1	Source Synch	Input/Output
A30#	T5	Source Synch	Input/Output

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
A31#	U4	Source Synch	Input/Output
A32#	V3	Source Synch	Input/Output
A33#	W2	Source Synch	Input/Output
A34#	Y1	Source Synch	Input/Output
A35#	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB0#	L5	Source Synch	Input/Output
ADSTB1#	R5	Source Synch	Input/Output
AP0#	AC1	Common Clock	Input/Output
AP1#	V5	Common Clock	Input/Output
BCLK0	AF22	Bus Clock	Input
BCLK1	AF23	Bus Clock	Input
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BPM0#	AC6	Common Clock	Input/Output
BPM1#	AB5	Common Clock	Input/Output
BPM2#	AC4	Common Clock	Input/Output
BPM3#	Y6	Common Clock	Input/Output
BPM4#	AA5	Common Clock	Input/Output
BPM5#	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP0	L24	Power/Other	Input/Output
COMP1	P1	Power/Other	Input/Output
D00#	B21	Source Synch	Input/Output
D01#	B22	Source Synch	Input/Output

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D02#	A23	Source Synch	Input/Output
D03#	A25	Source Synch	Input/Output
D04#	C21	Source Synch	Input/Output
D05#	D22	Source Synch	Input/Output
D06#	B24	Source Synch	Input/Output
D07#	C23	Source Synch	Input/Output
D08#	C24	Source Synch	Input/Output
D09#	B25	Source Synch	Input/Output
D10#	G22	Source Synch	Input/Output
D11#	H21	Source Synch	Input/Output
D12#	C26	Source Synch	Input/Output
D13#	D23	Source Synch	Input/Output
D14#	J21	Source Synch	Input/Output
D15#	D25	Source Synch	Input/Output
D16#	H22	Source Synch	Input/Output
D17#	E24	Source Synch	Input/Output
D18#	G23	Source Synch	Input/Output
D19#	F23	Source Synch	Input/Output
D20#	F24	Source Synch	Input/Output
D21#	E25	Source Synch	Input/Output
D22#	F26	Source Synch	Input/Output
D23#	D26	Source Synch	Input/Output
D24#	L21	Source Synch	Input/Output
D25#	G26	Source Synch	Input/Output
D26#	H24	Source Synch	Input/Output
D27#	M21	Source Synch	Input/Output
D28#	L22	Source Synch	Input/Output
D29#	J24	Source Synch	Input/Output
D30#	K23	Source Synch	Input/Output
D31#	H25	Source Synch	Input/Output
D32#	M23	Source Synch	Input/Output
D33#	N22	Source Synch	Input/Output
D34#	P21	Source Synch	Input/Output
D35#	M24	Source Synch	Input/Output
D36#	N23	Source Synch	Input/Output
D37#	M26	Source Synch	Input/Output
D38#	N26	Source Synch	Input/Output
D39#	N25	Source Synch	Input/Output
D40#	R21	Source Synch	Input/Output

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
D41#	P24	Source Synch	Input/Output
D42#	R25	Source Synch	Input/Output
D43#	R24	Source Synch	Input/Output
D44#	T26	Source Synch	Input/Output
D45#	T25	Source Synch	Input/Output
D46#	T22	Source Synch	Input/Output
D47#	T23	Source Synch	Input/Output
D48#	U26	Source Synch	Input/Output
D49#	U24	Source Synch	Input/Output
D50#	U23	Source Synch	Input/Output
D51#	V25	Source Synch	Input/Output
D52#	U21	Source Synch	Input/Output
D53#	V22	Source Synch	Input/Output
D54#	V24	Source Synch	Input/Output
D55#	W26	Source Synch	Input/Output
D56#	Y26	Source Synch	Input/Output
D57#	W25	Source Synch	Input/Output
D58#	Y23	Source Synch	Input/Output
D59#	Y24	Source Synch	Input/Output
D60#	Y21	Source Synch	Input/Output
D61#	AA25	Source Synch	Input/Output
D62#	AA22	Source Synch	Input/Output
D63#	AA24	Source Synch	Input/Output
DBI0#	E21	Source Synch	Input/Output
DBI1#	G25	Source Synch	Input/Output
DBI2#	P26	Source Synch	Input/Output
DBI3#	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP0#	J26	Common Clock	Input/Output
DP1#	K25	Common Clock	Input/Output
DP2#	K26	Common Clock	Input/Output
DP3#	L25	Common Clock	Input/Output
DRDY#	H2	Common Clock	Input/Output
DSTBN0#	E22	Source Synch	Input/Output
DSTBN1#	K22	Source Synch	Input/Output
DSTBN2#	R22	Source Synch	Input/Output
DSTBN3#	W22	Source Synch	Input/Output

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
DSTBP0#	F21	Source Synch	Input/Output
DSTBP1#	J23	Source Synch	Input/Output
DSTBP2#	P23	Source Synch	Input/Output
DSTBP3#	W23	Source Synch	Input/Output
FERR#	B6	Asynch AGL+	Output
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Common Clock	Output
IGNNE#	B2	Asynch GTL+	Input
INIT#	W5	Asynch GTL+	Input
ITPCLKOUT0	AA20	Power/Other	Output
ITPCLKOUT1	AB22	Power/Other	Output
ITP_CLK0	AC26	TAP	input
ITP_CLK1	AD26	TAP	input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
PROCHOT#	C3	Asynch GTL+	Output
PWRGOOD	AB23	Asynch GTL+	Input
REQ0#	J1	Source Synch	Input/Output
REQ1#	K5	Source Synch	Input/Output
REQ2#	J4	Source Synch	Input/Output
REQ3#	J3	Source Synch	Input/Output
REQ4#	H3	Source Synch	Input/Output
RESERVED	A22		
RESERVED	A7		
RESERVED	AD2		
RESERVED	AD3		
RESERVED	AE21		
RESERVED	AF3		
RESERVED	AF24		
RESERVED	AF25		
RESET#	AB25	Common Clock	Input
RS0#	F1	Common Clock	Input

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
RS1#	G5	Common Clock	Input
RS2#	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SMI#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
TESTHI11	A6	Power/Other	Input
TESTHI12	AD25	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A14	Power/Other	
VCC	A16	Power/Other	
VCC	A18	Power/Other	
VCC	A20	Power/Other	
VCC	A8	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	
VCC	AA14	Power/Other	
VCC	AA16	Power/Other	
VCC	AA18	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	AA8	Power/Other	
VCC	AB11	Power/Other	
VCC	AB13	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB19	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC14	Power/Other	
VCC	AC16	Power/Other	
VCC	AC18	Power/Other	
VCC	AC8	Power/Other	
VCC	AD11	Power/Other	
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AD20	Power/Other	
VCCIOPLL	AE23	Power/Other	
VCCSENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VID0	AE5	Power/Other	Output

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VSS	D10	Power/Other	
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD1	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	
VSS	AE15	Power/Other	
VSS	AE17	Power/Other	
VSS	AE19	Power/Other	
VSS	AE22	Power/Other	
VSS	AE24	Power/Other	
VSS	AE26	Power/Other	
VSS	AE7	Power/Other	
VSS	AE9	Power/Other	
VSS	AF1	Power/Other	
VSS	AF10	Power/Other	
VSS	AF12	Power/Other	
VSS	AF14	Power/Other	
VSS	AF16	Power/Other	
VSS	AF18	Power/Other	
VSS	AF20	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	B10	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	B12	Power/Other	
VSS	B14	Power/Other	
VSS	B16	Power/Other	
VSS	B18	Power/Other	
VSS	B20	Power/Other	
VSS	B23	Power/Other	
VSS	B26	Power/Other	
VSS	B4	Power/Other	
VSS	B8	Power/Other	
VSS	C11	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C17	Power/Other	
VSS	C19	Power/Other	
VSS	C2	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	C5	Power/Other	
VSS	C7	Power/Other	
VSS	C9	Power/Other	
VSS	D12	Power/Other	
VSS	D14	Power/Other	
VSS	D16	Power/Other	
VSS	D18	Power/Other	
VSS	D20	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D6	Power/Other	
VSS	D8	Power/Other	
VSS	E1	Power/Other	
VSS	E11	Power/Other	
VSS	E13	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E26	Power/Other	
VSS	E4	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	E7	Power/Other	
VSS	E9	Power/Other	
VSS	F10	Power/Other	
VSS	F12	Power/Other	
VSS	F14	Power/Other	
VSS	F16	Power/Other	
VSS	F18	Power/Other	
VSS	F2	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	G21	Power/Other	
VSS	G24	Power/Other	
VSS	G3	Power/Other	
VSS	G6	Power/Other	
VSS	H1	Power/Other	
VSS	H23	Power/Other	
VSS	H26	Power/Other	
VSS	H4	Power/Other	
VSS	J2	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	J5	Power/Other	
VSS	K21	Power/Other	
VSS	K24	Power/Other	
VSS	K3	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L23	Power/Other	
VSS	L26	Power/Other	
VSS	L4	Power/Other	
VSS	M2	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	M5	Power/Other	
VSS	N21	Power/Other	
VSS	N24	Power/Other	
VSS	N3	Power/Other	

Table 32. Pin Listing by Pin Name

Pin Name	Pin Number	Signal Buffer Type	Direction
VSS	N6	Power/Other	
VSS	P2	Power/Other	
VSS	P22	Power/Other	
VSS	P25	Power/Other	
VSS	P5	Power/Other	
VSS	R1	Power/Other	
VSS	R23	Power/Other	
VSS	R26	Power/Other	
VSS	R4	Power/Other	
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	
VSS	V26	Power/Other	
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSSSENSE	A4	Power/Other	Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	VSS	Power/Other	
A4	VSSSENSE	Power/Other	Output
A5	VCCSENSE	Power/Other	Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
A6	TESTHI11	Power/Other	Input
A7	RESERVED		
A8	VCC	Power/Other	
A9	VSS	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VSS	Power/Other	
A14	VCC	Power/Other	
A15	VSS	Power/Other	
A16	VCC	Power/Other	
A17	VSS	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	VSS	Power/Other	
A22	RESERVED		
A23	D02#	Source Synch	Input/Output
A24	VSS	Power/Other	
A25	D03#	Source Synch	Input/Output
A26	VSS	Power/Other	
AA1	VSS	Power/Other	
AA2	TESTHI1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	VSS	Power/Other	
AA5	BPM4#	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA9	VSS	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VSS	Power/Other	
AA14	VCC	Power/Other	
AA15	VSS	Power/Other	
AA16	VCC	Power/Other	
AA17	VSS	Power/Other	
AA18	VCC	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AA19	VSS	Power/Other	
AA20	ITPCLK0	Power/Other	Output
AA21	GTLREF	Power/Other	Input
AA22	D62#	Source Synch	Input/Output
AA23	VSS	Power/Other	
AA24	D63#	Source Synch	Input/Output
AA25	D61#	Source Synch	Input/Output
AA26	VSS	Power/Other	
AB1	A35#	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	VSS	Power/Other	
AB4	BPM5#	Common Clock	Input/Output
AB5	BPM1#	Common Clock	Input/Output
AB6	VSS	Power/Other	
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VSS	Power/Other	
AB11	VCC	Power/Other	
AB12	VSS	Power/Other	
AB13	VCC	Power/Other	
AB14	VSS	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VSS	Power/Other	
AB19	VCC	Power/Other	
AB20	VSS	Power/Other	
AB21	VSS	Power/Other	
AB22	ITPCLK1	Power/Other	Output
AB23	PWRGOOD	Asynch GTL+	Input
AB24	VSS	Power/Other	
AB25	RESET#	Common Clock	Input
AB26	SLP#	Asynch GTL+	Input
AC1	AP0#	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Common Clock	Output
AC4	BPM2#	Common Clock	Input/Output
AC5	VSS	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AC6	BPM0#	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	input
AD1	VSS	Power/Other	
AD2	RESERVED		
AD3	RESERVED		
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	
AD11	VCC	Power/Other	
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AD19	VCC	Power/Other	
AD20	VCCA	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	TESTHI12	Power/Other	Input
AD26	ITP_CLK1	TAP	input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	RESERVED		
AE22	VSS	Power/Other	
AE23	VCCIOPLL	Power/Other	
AE24	VSS	Power/Other	
AE25	DBR#	Asynch GTL+	Output
AE26	VSS	Power/Other	
AF1	VSS	Power/Other	
AF2	VCC	Power/Other	
AF3	RESERVED		
AF4	VCCVID	Power/Other	Input
AF5	VCC	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
AF6	VSS	Power/Other	
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VSS	Power/Other	
AF13	VCC	Power/Other	
AF14	VSS	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VSS	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	BCLK0	Bus Clock	Input
AF23	BCLK1	Bus Clock	Input
AF24	RESERVED		
AF25	RESERVED		
AF26	SKTOCC#	Power/Other	Output
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	VSS	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#	Asynch AGL+	Output
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VSS	Power/Other	
B11	VCC	Power/Other	
B12	VSS	Power/Other	
B13	VCC	Power/Other	
B14	VSS	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	
B18	VSS	Power/Other	
B19	VCC	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
B20	VSS	Power/Other	
B21	D00#	Source Synch	Input/Output
B22	D01#	Source Synch	Input/Output
B23	VSS	Power/Other	
B24	D06#	Source Synch	Input/Output
B25	D09#	Source Synch	Input/Output
B26	VSS	Power/Other	
C1	TDI	TAP	Input
C2	VSS	Power/Other	
C3	PROCHOT#	Asynch GTL+	Output
C4	THERMDC	Power/Other	
C5	VSS	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	VSS	Power/Other	
C8	VCC	Power/Other	
C9	VSS	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VSS	Power/Other	
C14	VCC	Power/Other	
C15	VSS	Power/Other	
C16	VCC	Power/Other	
C17	VSS	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	VCC	Power/Other	
C21	D04#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	D07#	Source Synch	Input/Output
C24	D08#	Source Synch	Input/Output
C25	VSS	Power/Other	
C26	D12#	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	VSS	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	VSS	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
D7	VCC	Power/Other	
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VSS	Power/Other	
D11	VCC	Power/Other	
D12	VSS	Power/Other	
D13	VCC	Power/Other	
D14	VSS	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VSS	Power/Other	
D19	VCC	Power/Other	
D20	VSS	Power/Other	
D21	VSS	Power/Other	
D22	D05#	Source Synch	Input/Output
D23	D13#	Source Synch	Input/Output
D24	VSS	Power/Other	
D25	D15#	Source Synch	Input/Output
D26	D23#	Source Synch	Input/Output
E1	VSS	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input
E7	VSS	Power/Other	
E8	VCC	Power/Other	
E9	VSS	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VSS	Power/Other	
E14	VCC	Power/Other	
E15	VSS	Power/Other	
E16	VCC	Power/Other	
E17	VSS	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
E20	VCC	Power/Other	
E21	DBI0#	Source Synch	Input/Output
E22	DSTBN0#	Source Synch	Input/Output
E23	VSS	Power/Other	
E24	D17#	Source Synch	Input/Output
E25	D21#	Source Synch	Input/Output
E26	VSS	Power/Other	
F1	RS0#	Common Clock	Input
F2	VSS	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS2#	Common Clock	Input
F5	VSS	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VSS	Power/Other	
F11	VCC	Power/Other	
F12	VSS	Power/Other	
F13	VCC	Power/Other	
F14	VSS	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VSS	Power/Other	
F19	VCC	Power/Other	
F20	GTLREF	Power/Other	Input
F21	DSTBP0#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	D19#	Source Synch	Input/Output
F24	D20#	Source Synch	Input/Output
F25	VSS	Power/Other	
F26	D22#	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	VSS	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS1#	Common Clock	Input
G6	VSS	Power/Other	

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
G21	VSS	Power/Other	
G22	D10#	Source Synch	Input/Output
G23	D18#	Source Synch	Input/Output
G24	VSS	Power/Other	
G25	DBI1#	Source Synch	Input/Output
G26	D25#	Source Synch	Input/Output
H1	VSS	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ4#	Source Synch	Input/Output
H4	VSS	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D11#	Source Synch	Input/Output
H22	D16#	Source Synch	Input/Output
H23	VSS	Power/Other	
H24	D26#	Source Synch	Input/Output
H25	D31#	Source Synch	Input/Output
H26	VSS	Power/Other	
J1	REQ0#	Source Synch	Input/Output
J2	VSS	Power/Other	
J3	REQ3#	Source Synch	Input/Output
J4	REQ2#	Source Synch	Input/Output
J5	VSS	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D14#	Source Synch	Input/Output
J22	VSS	Power/Other	
J23	DSTBP1#	Source Synch	Input/Output
J24	D29#	Source Synch	Input/Output
J25	VSS	Power/Other	
J26	DP0#	Common Clock	Input/Output
K1	A06#	Source Synch	Input/Output
K2	A03#	Source Synch	Input/Output
K3	VSS	Power/Other	
K4	A04#	Source Synch	Input/Output
K5	REQ1#	Source Synch	Input/Output
K6	VSS	Power/Other	
K21	VSS	Power/Other	
K22	DSTBN1#	Source Synch	Input/Output
K23	D30#	Source Synch	Input/Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
K24	VSS	Power/Other	
K25	DP1#	Common Clock	Input/Output
K26	DP2#	Common Clock	Input/Output
L1	VSS	Power/Other	
L2	A09#	Source Synch	Input/Output
L3	A07#	Source Synch	Input/Output
L4	VSS	Power/Other	
L5	ADSTB0#	Source Synch	Input/Output
L6	A05#	Source Synch	Input/Output
L21	D24#	Source Synch	Input/Output
L22	D28#	Source Synch	Input/Output
L23	VSS	Power/Other	
L24	COMP0	Power/Other	Input/Output
L25	DP3#	Common Clock	Input/Output
L26	VSS	Power/Other	
M1	A13#	Source Synch	Input/Output
M2	VSS	Power/Other	
M3	A10#	Source Synch	Input/Output
M4	A11#	Source Synch	Input/Output
M5	VSS	Power/Other	
M6	A08#	Source Synch	Input/Output
M21	D27#	Source Synch	Input/Output
M22	VSS	Power/Other	
M23	D32#	Source Synch	Input/Output
M24	D35#	Source Synch	Input/Output
M25	VSS	Power/Other	
M26	D37#	Source Synch	Input/Output
N1	A12#	Source Synch	Input/Output
N2	A14#	Source Synch	Input/Output
N3	VSS	Power/Other	
N4	A15#	Source Synch	Input/Output
N5	A16#	Source Synch	Input/Output
N6	VSS	Power/Other	
N21	VSS	Power/Other	
N22	D33#	Source Synch	Input/Output
N23	D36#	Source Synch	Input/Output
N24	VSS	Power/Other	
N25	D39#	Source Synch	Input/Output
N26	D38#	Source Synch	Input/Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
P1	COMP1	Power/Other	Input/Output
P2	VSS	Power/Other	
P3	A19#	Source Synch	Input/Output
P4	A20#	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	A24#	Source Synch	Input/Output
P21	D34#	Source Synch	Input/Output
P22	VSS	Power/Other	
P23	DSTBP2#	Source Synch	Input/Output
P24	D41#	Source Synch	Input/Output
P25	VSS	Power/Other	
P26	DBI2#	Source Synch	Input/Output
R1	VSS	Power/Other	
R2	A18#	Source Synch	Input/Output
R3	A21#	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	ADSTB1#	Source Synch	Input/Output
R6	A28#	Source Synch	Input/Output
R21	D40#	Source Synch	Input/Output
R22	DSTBN2#	Source Synch	Input/Output
R23	VSS	Power/Other	
R24	D43#	Source Synch	Input/Output
R25	D42#	Source Synch	Input/Output
R26	VSS	Power/Other	
T1	A17#	Source Synch	Input/Output
T2	A22#	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A26#	Source Synch	Input/Output
T5	A30#	Source Synch	Input/Output
T6	VSS	Power/Other	
T21	VSS	Power/Other	
T22	D46#	Source Synch	Input/Output
T23	D47#	Source Synch	Input/Output
T24	VSS	Power/Other	
T25	D45#	Source Synch	Input/Output
T26	D44#	Source Synch	Input/Output
U1	A23#	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	A25#	Source Synch	Input/Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
U4	A31#	Source Synch	Input/Output
U5	VSS	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D52#	Source Synch	Input/Output
U22	VSS	Power/Other	
U23	D50#	Source Synch	Input/Output
U24	D49#	Source Synch	Input/Output
U25	VSS	Power/Other	
U26	D48#	Source Synch	Input/Output
V1	VSS	Power/Other	
V2	A27#	Source Synch	Input/Output
V3	A32#	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	AP1#	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI3#	Source Synch	Input/Output
V22	D53#	Source Synch	Input/Output
V23	VSS	Power/Other	
V24	D54#	Source Synch	Input/Output
V25	D51#	Source Synch	Input/Output
V26	VSS	Power/Other	
W1	A29#	Source Synch	Input/Output
W2	A33#	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input
W6	VSS	Power/Other	
W21	VSS	Power/Other	
W22	DSTBN3#	Source Synch	Input/Output
W23	DSTBP3#	Source Synch	Input/Output
W24	VSS	Power/Other	
W25	D57#	Source Synch	Input/Output
W26	D55#	Source Synch	Input/Output
Y1	A34#	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	VSS	Power/Other	
Y6	BPM3#	Common Clock	Input/Output

Table 33. Pin Listing by Pin Number

Pin Number	Pin Name	Signal Buffer Type	Direction
Y21	D60#	Source Synch	Input/Output
Y22	VSS	Power/Other	
Y23	D58#	Source Synch	Input/Output
Y24	D59#	Source Synch	Input/Output
Y25	VSS	Power/Other	
Y26	D56#	Source Synch	Input/Output

5.2 Alphabetical Signals Reference

Table 34. Signal Description (Page 1 of 8)

Name	Type	Description
A[35:3]#	Input/ Output	A[35:3]# (Address) define a 2^{36}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the Intel® Pentium® 4 processor with 512KB L2 cache system bus. A[35:3]# are protected by parity signals AP[1:0]#. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processor samples a subset of the A[35:3]# pins to determine power-on configuration. See Section 7.1 for more details.
A20M#	Input	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/ write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
ADS#	Input/ Output	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	Input/ Output	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** / **Associated Strobe** REQ[4:0]#, A[16:3]# / ADSTB0# A[35:17]# / ADSTB1#
AP[1:0]#	Input/ Output	AP[1:0]# (Address Parity) are driven by the request initiator along with ADS#, A[35:3]#, and the transaction type on the REQ[4:0]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are high. AP[1:0]# should connect the appropriate pins of all Intel® Pentium® 4 processor with 512KB L2 cache system bus agents. The following table defines the coverage model of these signals. **Request Signals** / **subphase 1** / **subphase 2** A[35:24]# / AP0# / AP1# A[23:3]# / AP1# / AP0# REQ[4:0]# / AP1# / AP0#
BCLK[1:0]	Input	The differential pair BCLK (Bus Clock) determines the system bus frequency. All processor system bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing V_{CROSS}.

Table 34. Signal Description (Page 2 of 8)

Name	Type	Description
BINIT#	Input/ Output	BINIT# (Bus Initialization) may be observed and driven by all processor system bus agents and if used, must connect the appropriate pins of all such agents. If the BINIT# driver is enabled during power-on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents do not reset their IOQ and transaction tracking state machines upon observation of BINIT# activation. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the system bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is disabled during power-on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	Input/ Output	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[5:0]#	Input/ Output	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all Intel® Pentium® 4 processor with 512KB L2 cache system bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is used by debug tools to request debug operation of the processor. Please refer to the Intel®Pentium® 4 Processor/Intel® Pentium® 4 processor with 512KB L2 cache *and* Intel® 850 *Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package*/Intel® Pentium® 4 processor with 512KB L2 cache *and Intel® 845 Chipset Platform Design Guide* for more detailed information. **These signals do not have on-die termination and must be terminated on the system board.**
BPRI#	Input	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor system bus. It must connect the appropriate pins of all processor system bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed, then releases the bus by deasserting BPRI#.
BR0#	Input/ Output	BR0# drives the BREQ0# signal in the system and is used by the processor to request the bus. During power-on configuration this pin is sampled to determine the agent ID = 0. **This signal does not have on-die termination and must be terminated.**
BSEL[1:0]	Input/ Output	BSEL[1:0] (Bus Select) are used to select the processor input clock frequency. Table 4 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset and clock synthesizer. All agents must operate at the same frequency. The Pentium 4 processor in the 478-pin package operates at a 400 MHz system bus frequency (100 MHz BCLK[1:0] frequency). For more information about these pins, including termination recommendations refer to Section 2.9 and the appropriate platform design guidelines.
COMP[1:0]	Analog	COMP[1:0] must be terminated on the system board using precision resistors. Refer to the Intel®Pentium® 4 Processor/Intel® Pentium® 4 processor with 512KB L2 cache *and* Intel® 850 *Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package*/Intel® Pentium® 4 processor with 512KB L2 cache *and Intel® 845 Chipset Platform Design Guide* for details on implementation.

Table 34. Signal Description (Page 3 of 8)

<table>
<tr><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>D[63:0]#</td><td>Input/ Output</td><td>D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor system bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer.
D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DBI#.
Quad-Pumped Signal Groups
<table>
<tr><th>Data Group</th><th>DSTBN#/ DSTBP#</th><th>DBI#</th></tr>
<tr><td>D[15:0]#</td><td>0</td><td>0</td></tr>
<tr><td>D[31:16]#</td><td>1</td><td>1</td></tr>
<tr><td>D[47:32]#</td><td>2</td><td>2</td></tr>
<tr><td>D[63:48]#</td><td>3</td><td>3</td></tr>
</table>
Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.</td></tr>
<tr><td>DBI[3:0]#</td><td>Input/ Output</td><td>DBI[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle.
DBI[3:0]# Assignment To Data Bus
<table>
<tr><th>Bus Signal</th><th>Data Bus Signals</th></tr>
<tr><td>DBI3#</td><td>D[63:48]#</td></tr>
<tr><td>DBI2#</td><td>D[47:32]#</td></tr>
<tr><td>DBI1#</td><td>D[31:16]#</td></tr>
<tr><td>DBI0#</td><td>D[15:0]#</td></tr>
</table></td></tr>
<tr><td>DBR#</td><td>Output</td><td>DBR# (Data Bus Reset) is used only in processor systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. If a debug port is implemented in the system, DBR# is a no connect in the system. DBR# is not a processor signal.</td></tr>
<tr><td>DBSY#</td><td>Input/ Output</td><td>DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor system bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor system bus agents.</td></tr>
<tr><td>DEFER#</td><td>Input</td><td>DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of all processor system bus agents.</td></tr>
<tr><td>DP[3:0]#</td><td>Input/ Output</td><td>DP[3:0]# (Data parity) provide parity protection for the D[63:0]# signals. They are driven by the agent responsible for driving D[63:0]#, and must connect the appropriate pins of all Intel® Pentium® 4 processor with 512KB L2 cache system bus agents.</td></tr>
</table>

Table 34. Signal Description (Page 4 of 8)

Name	Type	Description
DRDY#	Input/ Output	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor system bus agents.
DSTBN[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DBI0# — DSTBN0# D[31:16]#, DBI1# — DSTBN1# D[47:32]#, DBI2# — DSTBN2# D[63:48]#, DBI3# — DSTBN3#
DSTBP[3:0]#	Input/ Output	Data strobe used to latch in D[63:0]#. **Signals** / **Associated Strobe** D[15:0]#, DBI0# — DSTBP0# D[31:16]#, DBI1# — DSTBP1# D[47:32]#, DBI2# — DSTBP2# D[63:48]#, DBI3# — DSTBP3#
FERR#/PBE#	Output	FERR#/PBE# (floating point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. *When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is deasserted.* For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to volume 3 of the *Intel Architecture Software Developer's Manual* and the *Intel Processor Identification and the CPUID Instruction* application note.
GTLREF	Input	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{CC}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1. Refer to the Intel®Pentium® 4 Processor/Intel® Pentium® 4 processor with 512KB L2 cache *and* Intel® 850 *Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package*/Intel® Pentium® 4 processor with 512KB L2 cache *and Intel® 845 Chipset Platform Design Guide* for more information.
HIT# HITM#	Input/ Output Input/ Output	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any system bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.

Table 34. Signal Description (Page 5 of 8)

Name	Type	Description
IERR#	Output	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor system bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#. **This signal does not have on-die termination and must be terminated on the system board.**
IGNNE#	Input	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction.
INIT#	Input	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor system bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
ITPCLKOUT[1:0]	Output	ITPCLKOUT[1:0] is an uncompensated differential clock output that is a delayed copy of BCLK[1:0], which is an input to the processor. This clock output can be used as the differential clock into the ITP port that is designed onto the system board. If ITPCLKOUT[1:0] outputs are not used, they must be terminated properly. Refer to Section 2.5 for additional details and termination requirements. Refer to the *Pentium® 4 Processor Debug Port Design Guide* for details on implementing a debug port.
ITP_CLK[1:0]	Input	ITP_CLK[1:0] are copies of BCLK that are used only in processor systems where no debug port is implemented on the system board. ITP_CLK[1:0] are used as BCLK[1:0] references for a debug port implemented on an interposer. If a debug port is implemented in the system, ITP_CLK[1:0] are no connects in the system. These are not processor signals.
LINT[1:0]	Input	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	Input/ Output	LOCK# indicates to the system that a transaction must occur atomically. This signal must connect the appropriate pins of all processor system bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor system bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor system bus throughout the bus locked operation and ensure the atomicity of lock.

Table 34. Signal Description (Page 6 of 8)

Name	Type	Description
MCERR#	Input/ Output	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error without a bus protocol violation. It may be driven by all processor system bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined by the following options: Enabled or disabled. Asserted, if configured, for internal errors along with IERR#. Asserted, if configured, by the request initiator of a bus transaction after it observes an error. Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, please refer to the *IA-32 Software Developer's Manual, Volume 3: System Programming Guide*.
PROCHOT#	Output	PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. See Section 7.3 for more details.
PWRGOOD	Input	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 14 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 17, and be followed by a 1 to 10 ms RESET# pulse. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	Input/ Output	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor system bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB0#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.
RESET#	Input	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least one millisecond after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, all system bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms while PWRGOOD is asserted. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in the Section 7.1. **This signal does not have on-die termination and must be terminated on the system board.**
RS[2:0]#	Input	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of all processor system bus agents.

Table 34. Signal Description (Page 7 of 8)

Name	Type	Description
RSP#	Input	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor system bus agents. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. While RS[2:0]# = 000, RSP# is also high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	Output	SKTOCC# (Socket Occupied) will be pulled to ground by the processor. System board designers may use this pin to determine if the processor is present.
SLP#	Input	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will only recognize the assertion of the RESET# signal, deassertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is deasserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If the BCLK input is stopped while in the Sleep state the processor will exit the Sleep state and transition to the Deep Sleep state.
SMI#	Input	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enters System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the deassertion of RESET# the processor will tristate its outputs.
STPCLK#	Input	Assertion of STPCLK# (Stop Clock) causes the processor to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the system bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	Input	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	Input	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	Output	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TESTHI[12:8] TESTHI[5:0]	Input	TESTHI[12:8] and TESTHI[5:0] must be connected to a V_{CC} power source through a resistor for proper processor operation. See Section 2.5 for more details.
THERMDA	Other	Thermal Diode Anode. See Section 7.3.1.
THERMDC	Other	Thermal Diode Cathode. See Section 7.3.1.

Table 34. Signal Description (Page 8 of 8)

Name	Type	Description
THERMTRIP#	Output	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a level where permanent silicon damage may occur. Measurement of the temperature is accomplished through an internal thermal sensor which is configured to trip at approximately 135°C. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor, its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. See Figure and Table 17 for the appropriate power down sequence and timing requirements. Once activated, THERMTRIP# remains latched until RESET# is asserted. While the assertion of the RESET# signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.
TMS	Input	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	Input	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all system bus agents.
TRST#	Input	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset. This can be done with a 680 Ω pull-down resistor.
V_{CCA}	Input	V_{CCA} provides isolated power for the internal processor core PLL's. Refer to the Intel®Pentium® 4 Processor/Intel® Pentium® 4 processor with 512KB L2 cache *and* Intel® 850 *Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package*/Intel® Pentium® 4 processor with 512KB L2 cache *and Intel® 845 Chipset Platform Design Guide* for complete implementation details.
$V_{CCIOPLL}$	Input	$V_{CCIOPLL}$ provides isolated power for internal processor system bus PLL's. Follow the guidelines for V_{CCA}, and refer to the Intel®Pentium® 4 Processor/Intel® Pentium® 4 processor with 512KB L2 cache *and* Intel® 850 *Chipset Platform Design Guide* and the *Intel® Pentium® 4 Processor in the 478 Pin Package*/Intel® Pentium® 4 processor with 512KB L2 cache *and Intel® 845 Chipset Platform Design Guide* for complete implementation details.
$V_{CCSENSE}$	Output	$V_{CCSENSE}$ is an isolated low impedance connection to processor core power (V_{CC}). It can be used to measure power near the silicon with little noise.
VCCVID	Input	Supply for the Voltage Identification circuit of the processor. Independent 1.2V supply must be routed to VCCVID pin.
VID[4:0]	Output	VID[4:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (Vcc). Unlike previous generations of processors, these are open drain signals that are driven by the Intel® Pentium® 4 processor with 512KB L2 cache and must be pulled up to 3.3V (max.) with 1KΩ resistors. The voltage supply for these pins must be valid before the VR can supply V_{CC} to the processor. Conversely, the VR output must be disabled until the voltage supply for the VID pins becomes valid. The VID pins are needed to support the processor voltage specification variations. See Table 2 for definitions of these pins. The VR must supply the voltage that is requested by the pins, or disable itself.
V_{SSA}	Input	V_{SSA} is the isolated ground for internal PLLs.
$V_{SSSENSE}$	Output	$V_{SSSENSE}$ is an isolated low impedance connection to processor core V_{SS}. It can be used to measure ground near the silicon with little noise

6.0 Thermal Specifications and Design Considerations

The Intel® Pentium® 4 processor with 512KB L2 cache uses an integrated heat spreader (IHS) for heatsink attachment which is intended to provide an interface for multiple types of thermal solutions. This section will provide data necessary for development of a thermal solution.

6.1 Thermal Specifications

Table 35 specifies the thermal design power dissipation envelope for Intel® Pentium® 4 processor with 512KB L2 caches. The Thermal Monitor feature is designed to help protect the processor from overheating. For more details on the usage of this feature, refer to Section 7.3. **In all cases the Thermal Monitor feature must be enabled for the processor to be operating within the published specification.** Table 35 also lists the maximum and minimum processor temperature specifications for T_{CASE}. A thermal solution must be designed to ensure the temperature of the processor does not exceed these specifications.

Table 35. Intel® Pentium® 4 processor with 512KB L2 cache Thermal Design Power

Processor and Core Frequency	Thermal Design Power [2] (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
1.60 GHz	38.7	5	67	
1.80 GHz	41.6	5	68	
2 GHz	44.6	5	70	

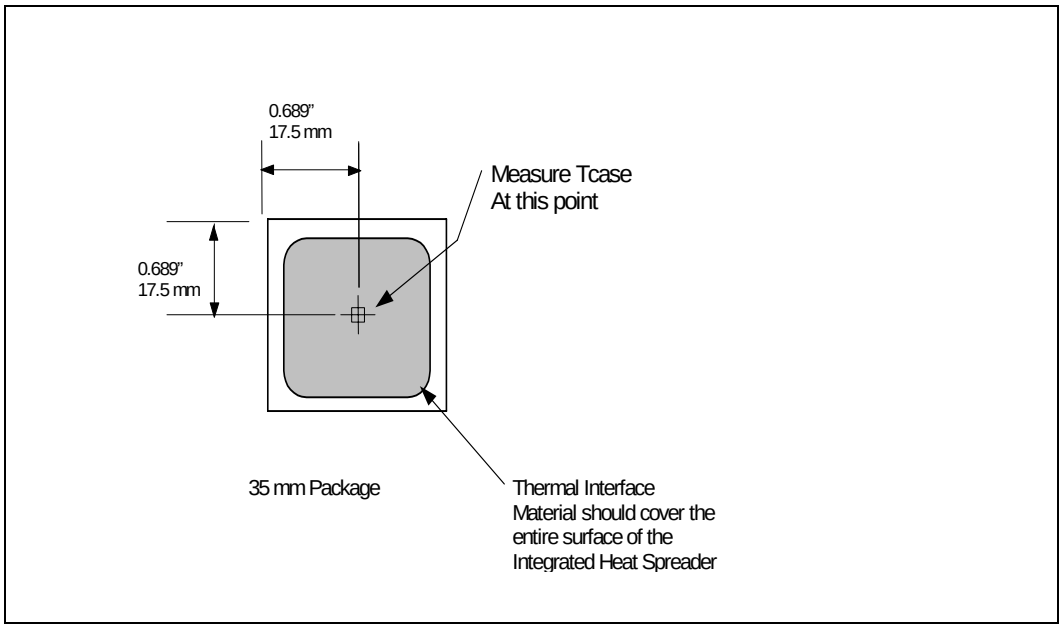
NOTES:
1. These values are specified at V_{CC_MAX} for the processor. Systems must be designed to ensure that the processor is not subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} at specified I_{CC}. Please refer to loadline specifications in Chapter 2.
2. The numbers in this column reflect Intel's recommended design point and are not indicative of the maximum power the processor can dissipate under worst case conditions.

6.1.1 Measurements For Thermal Specifications

6.1.1.1 Processor Case Temperature Measurement

The maximum and minimum case temperature (T_{CASE}) for the Intel® Pentium® 4 processor with 512KB L2 cache is specified in Table 35. This temperature specification is meant to ensure correct and reliable operation of the processor. Figure 34 illustrates where Intel recommends T_{CASE} thermal measurements should be made.

Figure 34. Guideline Locations for Case Temperature (T_{CASE}) Thermocouple Placement



7.0 Features

7.1 Power-On Configuration Options

Several configuration options can be configured by hardware. Intel® Pentium® 4 processor with 512KB L2 caches sample their hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, please refer to Table 36.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset. All resets reconfigure the processor; for reset purposes, the processor does not distinguish between a "warm" reset and a "power-on" reset.

Table 36. Power-On Configuration Option Pins

Configuration Option	Pin[1]
Output tristate	SMI#
Execute BIST	INIT#
In-Order Queue pipelining (set IOQ depth to 1)	A7#
Disable MCERR# observation	A9#
Disable BINIT# observation	A10#
APIC Cluster ID (0-3)	A[12:11]#
Disable bus parking	A15#
Symmetric agent arbitration ID	BR0#

NOTE:
1. Asserting this signal during RESET# will select the corresponding option.

7.2 Clock Control and Low Power States

The use of AutoHALT, Stop-Grant, Sleep, and Deep Sleep states is allowed in Intel® Pentium® 4 processor with 512KB L2 cache based systems to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 35 for a visual representation of the processor low power states.

7.2.1 Normal State—State 1

This is the normal operating state for the processor.

7.2.2 AutoHALT Powerdown State—State 2

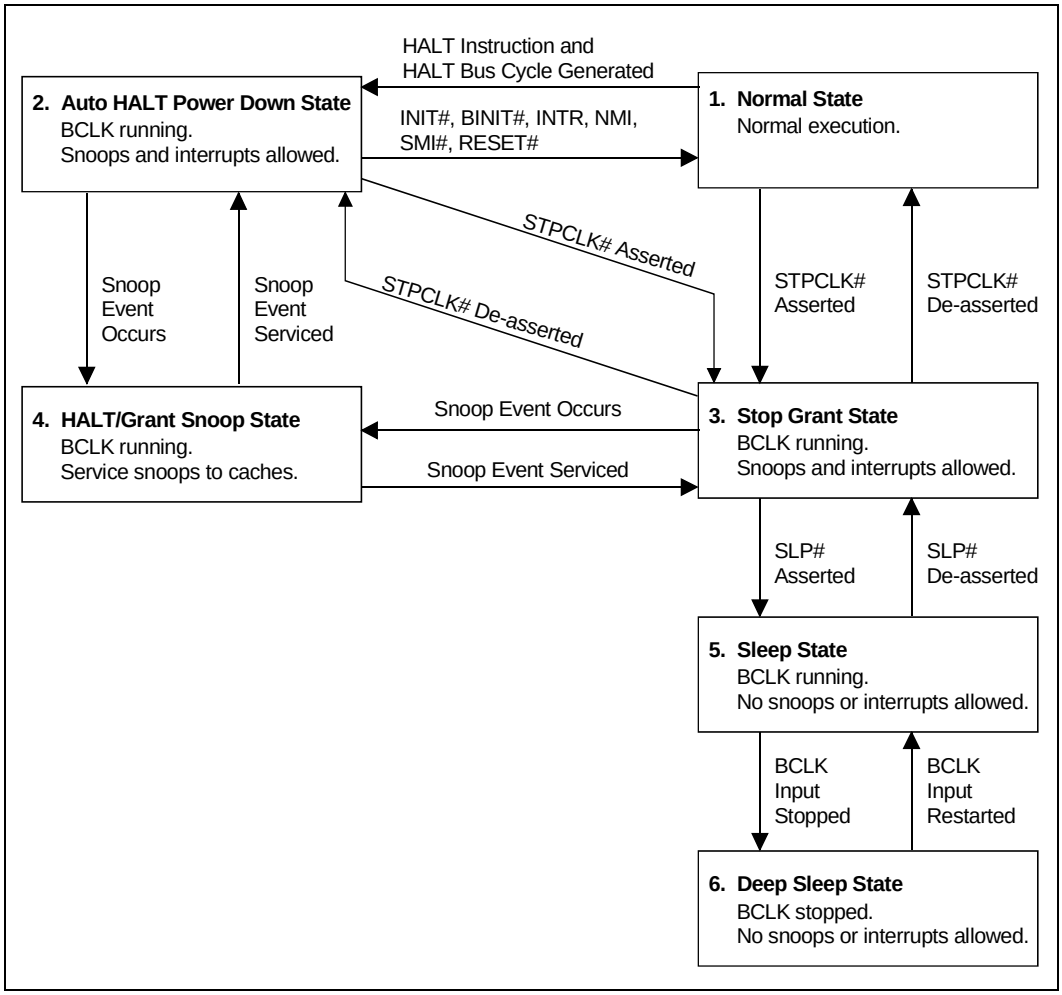
AutoHALT is a low power state entered when the processor executes the HALT instruction. The processor will transition to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, or LINT[1:0] (NMI, INTR). RESET# will cause the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the AutoHALT Power Down state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programmer's Guide* for more information.

The system can generate a STPCLK# while the processor is in the AutoHALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor will return execution to the HALT state.

While in AutoHALT Power Down state, the processor will process bus snoops.

Figure 35. Stop Clock State Machine



7.2.3 Stop-Grant State—State 3

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle.

Since the AGTL+ signal pins receive power from the system bus, these pins should not be driven (allowing the level to return to V_{CC}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the system bus should be driven to the inactive state.

BINIT# will not be serviced while the processor is in Stop-Grant state. The event will be latched and can be serviced by software upon exit from the Stop Grant state.

RESET# will cause the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state will occur with the de-assertion of the STPCLK# signal. When re-entering the Stop Grant state from the Sleep state, STPCLK# should only be de-asserted one or more bus clocks after the de-assertion of SLP#.

A transition to the HALT/Grant Snoop state will occur when the processor detects a snoop on the system bus (see Section 7.2.4). A transition to the Sleep state (see Section 7.2.5) will occur with the assertion of the SLP# signal.

While in the Stop-Grant State, SMI#, INIT#, BINIT# and LINT[1:0] will be latched by the processor, and only serviced when the processor returns to the Normal State. Only one occurrence of each event will be recognized upon return to the Normal state.

While in Stop-Grant state, the processor will process a system bus snoop.

7.2.4 HALT/Grant Snoop State—State 4

The processor will respond to snoop transactions on the system bus while in Stop-Grant state or in AutoHALT Power Down state. During a snoop transaction, the processor enters the HALT/Grant Snoop state. The processor will stay in this state until the snoop on the system bus has been serviced (whether by the processor or another agent on the system bus). After the snoop is serviced, the processor will return to the Stop-Grant state or AutoHALT Power Down state, as appropriate.

7.2.5 Sleep State—State 5

The Sleep state is a very low power state in which the processor maintains its context, maintains the phase-locked loop (PLL), and has stopped all internal clocks. The Sleep state can only be entered from Stop-Grant state. Once in the Stop-Grant state, the processor will enter the Sleep state upon the assertion of the SLP# signal. The SLP# pin should only be asserted when the processor is in the Stop Grant state. SLP# assertions while the processor is not in the Stop Grant state is out of specification and may result in erroneous processor operation.

Snoop events that occur while in Sleep State or during a transition into or out of Sleep state will cause unpredictable behavior.

In the Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals (with the exception of SLP# or RESET#) are allowed on the system bus while the processor is in Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behaviour.

If RESET# is driven active while the processor is in the Sleep state, and held active as specified in the RESET# pin specification, then the processor will reset itself, ignoring the transition through Stop-Grant State. If RESET# is driven active while the processor is in the Sleep State, the SLP# and STPCLK# signals should be deasserted immediately after RESET# is asserted to ensure the processor correctly executes the Reset sequence.

While in the Sleep state, the processor is capable of entering its lowest power state, the Deep Sleep state, by stopping the BCLK[1:0] inputs. (See Section 7.2.6). Once in the Sleep or Deep Sleep states, the SLP# pin must be de-asserted if another asynchronous system bus event needs to occur. The SLP# pin has a minimum assertion of one BCLK period.

When the processor is in Sleep state, it will not respond to interrupts or snoop transactions.

7.2.6 Deep Sleep State—State 6

Deep Sleep state is the lowest power state the processor can enter while maintaining context. Deep Sleep state is entered by stopping the BCLK[1:0] inputs (after the Sleep state was entered from the assertion of the SLP# pin). The processor is in Deep Sleep state immediately after BLCK[1:0] is stopped. The BCLK[1:0] inputs should be stopped such that one is below Vol and the other is above Voh. Stopping the BCLK input lowers the overall current consumption to leakage levels.

To re-enter the Sleep state, the BLCK input must be restarted. A period of 1 ms (to allow for PLL stabilization) must occur before the processor can be considered to be in the Sleep State. Once in the Sleep state, the SLP# pin can be deasserted to re-enter the Stop-Grant state.

While in Deep Sleep state, the processor is incapable of responding to snoop transactions or latching interrupt signals. No transitions or assertions of signals are allowed on the system bus while the processor is in Deep Sleep state. Any transition on an input signal before the processor has returned to Stop-Grant state will result in unpredictable behavior. The processor has to stay in Deep Sleep mode for a minimum of 25us.

7.3 Thermal Monitor

The Thermal Monitor feature found in the Intel® Pentium® 4 processor with 512KB L2 cache allows system designers to design lower cost thermal solutions without compromising system integrity or reliability. By using a factory-tuned, precision on-die thermal sensor, and a fast acting thermal control circuit (TCC), the processor, without the aid of any additional software or hardware, can keep the processor’s die temperature within factory specifications under nearly all conditions. Thermal Monitor thus allows the processor and system thermal solutions to be designed much closer to the power envelopes of real applications, instead of being designed to the higher maximum processor power envelopes.

Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks. The processor clocks are modulated when the TCC is activated. Thermal Monitor uses two modes to activate the TCC: Automatic mode and On-Demand mode. **Automatic mode is required for the processor to operate within specifications and must first be enabled via BIOS.** Once automatic mode is enabled,

the TCC will activate only when the internal die temperature is very near the temperature limits of the processor. When the TCC is enabled, and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30-50%). Clocks will not be off for more than 3 µs when TCC is active. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. Once the temperature has returned to a non-critical level, and the hystersis timer has expired, modulation ceases and TCC goes inactive. Processor performance will decrease when the TCC is active, however, with a properly designed and characterized thermal solution, the TCC most likely will never be activated, or only will be activated briefly during the most power intensive applications.

For automatic mode, the 50% duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers or interrupt handling routines.

The TCC may also be activated via On-Demand mode. If bit 4 of the ACPI Thermal Monitor Control Register is written to a "1" the TCC will be activated immediately, independent of the processor temperature. When using On-Demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in On-Demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-Demand mode may be used at the same time Automatic mode is enabled, however, if the system tries to enable the TCC via On-Demand mode at the same time automatic mode is enabled AND a high temperature condition exists, the 50% duty cycle of the automatic mode will override the duty cycle selected by the On-Demand mode.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is at the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active. The temperature at which the thermal control circuit activates is not user configurable and is not software visible.

Besides the thermal sensor and TCC, the Thermal Monitor feature also includes one ACPI register, one performance counter register, three model specific registers (MSR), and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Thermal Monitor feature. Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

If automatic mode is disabled the processor will be operating out of specification. Regardless of enabling of the automatic or On-Demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 135 °C. At this point the system bus signal THERMTRIP# will go active and stay active until RESET# has been initiated. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) must be removed within the timeframe defined in Table 17.

7.3.1 Thermal Diode

The Intel® Pentium® 4 processor with 512KB L2 cache incorporates an on-die thermal diode. A thermal sensor located on the system board may monitor the die temperature of the Intel® Pentium® 4 processor with 512KB L2 cache for thermal management/long

term die temperature change purposes. Table 37 and Table 38 provide the diode parameter and interface specifications. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 37. Thermal Diode Parameters

Symbol	Min	Typ	Max	Unit	Notes
$I_{forward\ bias}$	5		450	uA	1
n_ideality	.9935	1.0126	1.0316		2, 3, 4
R_T		3.64		Ω	2, 3, 5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized at 75°C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, n, represents the deviation from ideal diode behavior as exemplified by the diode equation:

   $$I_{FW} = I_S * (e^{qV_D/nkT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_D = voltage across the diode, k = Boltzmann Constant, and T = absolute temperature (Kelvin).
5. The series resistance, R_T, is provided to allow for a more accurate measurement of the junction temperature. R_T, as defined, includes the pins of the processor but does not include any socket resistance or board trace resistance between the socket and the external remote diode thermal sensor. RT can be used by remote diode thermal sensors with automatic series resistance cancellation to calibrate out this error term. Another application is that a temperature offset can be manually calculated and programmed into an offset register in the remote diode thermal sensors as exemplified by the equation:

   $$T_{error} = [R_T * (N-1) * I_{FWmin}] / [nk/q * \ln N]$$

   where T_{error} = sensor temperature error, N = sensor current ratio, k = Boltzmann Constant, q = electronic charge.

Table 38. Thermal Diode Interface

Pin Name	Pin Number	Pin Description
THERMDA	B3	diode anode
THERMDC	C4	diode cathode

8.0 Debug Tools Specifications

Please refer to the *Pentium® 4 Processor Debug Port Design Guide* and the appropriate platform design guidelines for more detailed information regarding debug tools specifications, such as integration details.

8.1 Logic Analyzer Interface (LAI)

Intel® is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging systems. Tektronix* and Agilent* should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of Intel® Pentium® 4 processor with 512KB L2 cache systems, the LAI is critical in providing the ability to probe and capture system bus signals. There are two sets of considerations to keep in mind when designing a Intel®Pentium® 4 Processor system that can make use of an LAI: mechanical and electrical.

8.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the Intel® Pentium® 4 processor with 512KB L2 cache. The LAI pins plug into the socket, while the Intel® Pentium® 4 processor with 512KB L2 cache pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the Intel® Pentium® 4 processor with 512KB L2 cache and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the Intel® Pentium® 4 processor with 512KB L2 cache heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

8.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the system bus; therefore, it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.