

ATTENTION
OBSERVE PRECAUTIONS
FOR HANDLING
ELECTROSTATIC
SENSITIVE
DEVICES

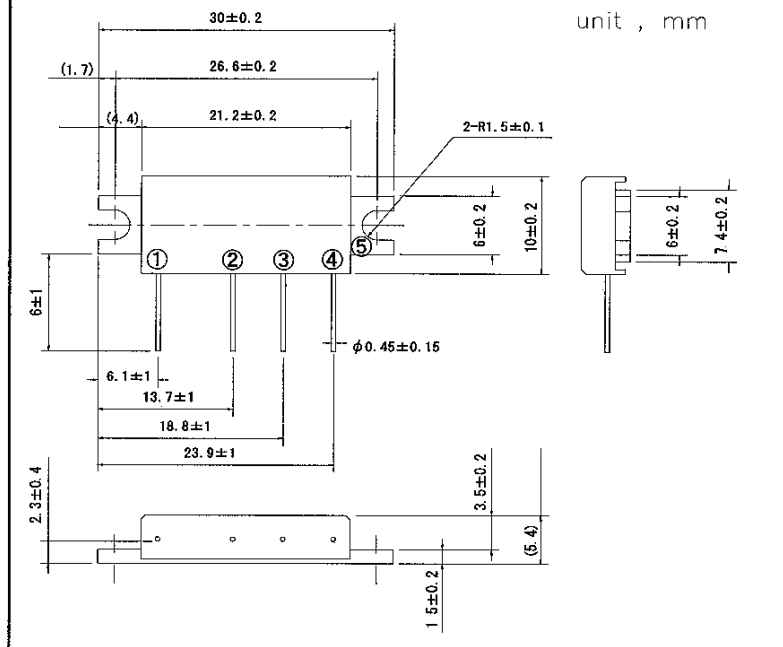
Revision date: 15th/Nov. '01

MITSUBISHI RF POWER MODULE

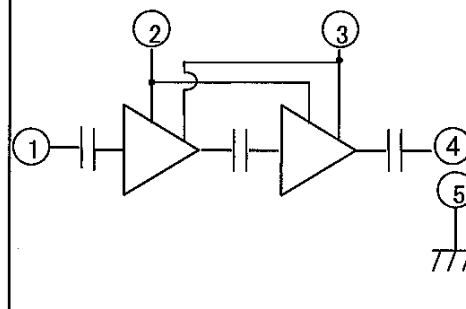
RA07M3340M

Silicon MOS FET Power Amplifier, 330-400MHz 7W PORTABLE RADIO

OUTLINE DRAWING



BLOCK DIAGRAM



PIN:

- 1 Pin :RF INPUT
- 2 V_{GG}:GATE BIAS SUPPLY
- 3 V_{DD}:DRAIN BIAS SUPPLY
- 4 P_o :RF OUTPUT
- 5 GND:FIN

MAXIMUM RATINGS (T_c=25deg.C UNLESS OTHERWISE NOTED)

SYMBOL	PARAMETER	CONDITIONS	RATINGS	UNIT
V _{DD}	SUPPLY VOLTAGE	V _{GG} <3.5V, Z _g =Z _l =50ohm	9.2	V
V _{GG}	GATE BIAS VOLTAGE	V _{DD} <7.2V, Pin=0mW, Z _g =Z _l =50ohm	4	V
P _{in}	INPUT POWER	f=330-400MHz, Z _g =Z _l =50ohm	70	mW
P _o	OUTPUT POWER	f=330-400MHz, Z _g =Z _l =50ohm	10	W
T _{C(OP)}	OPERATION CASE TEMPERATURE	f=330-400MHz, Z _g =Z _l =50ohm	-30 to +110	deg.C
T _{stg}	STORAGE TEMPERATURE		-40 to +110	deg.C

Note: Above parameters are guaranteed independently.

ELECTRICAL CHARACTERISTICS (T_c=25deg.C, Z_g=Z_l=50ohm UNLESS OTHERWISE NOTED)

SYMBOL	PARAMETER	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
f	FREQUENCY RANGE		330		400	MHz
P _o	OUTPUT POWER	V _{dd} =7.2V, V _{gg} =3.5V, Pin=50mW	7			W
E _t	TOTAL EFFICIENCY	P _o =6.5W, V _{dd} =7.2V, Pin=50mW, V _{gg} =adjust	40			%
2f _o	2nd HARMONIC				-25	dBc
VSWR _{in}	INPUT VSWR				4	-
	Stability	Z _g =50ohm, V _{dd} =4.0 - 9.2V, LOAD VSWR = 4:1, Pin=25 - 70mW, P _o <8W(V _{gg} Control)	No parasitic oscillation			
	LOAD VSWR TOLERANCE	V _{dd} =9.2V, Pin=50mW, P _o =7.0W(V _{gg} Control), Z _g =50ohm, LOAD VSWR = 20:1	No degradation or destroy			-

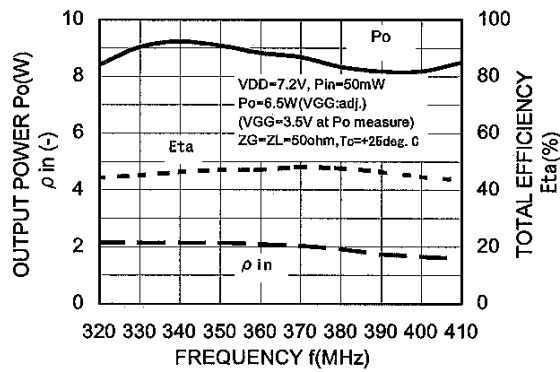
ABOVE PARAMETERS, RATINGS, LIMITS AND CONDITIONS ARE SUBJECT TO CHANGE .

Keep safety first in your circuit designs!

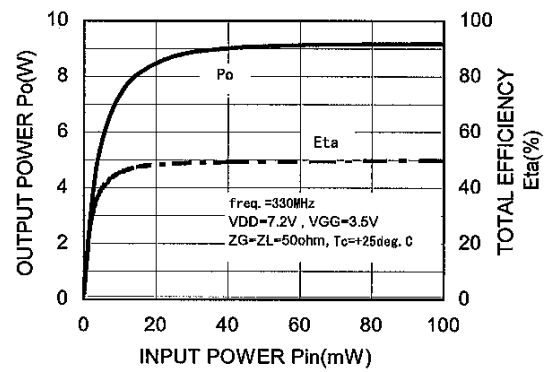
Mitsubishi Electric Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of non-flammable material or (iii) prevention against any malfunction or mishap.

TYPICAL PERFORMANCE DATA

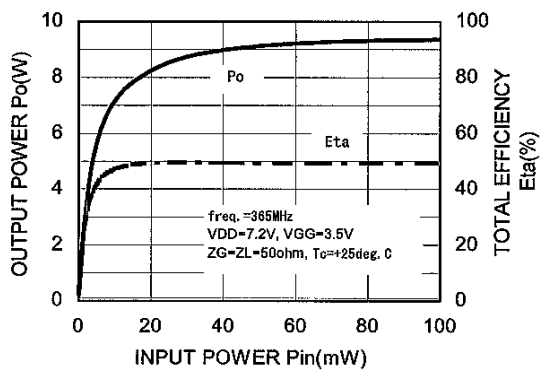
OUTPUT POWER, TOTAL EFFICIENCY, INPUT VSWR VS. FREQUENCY



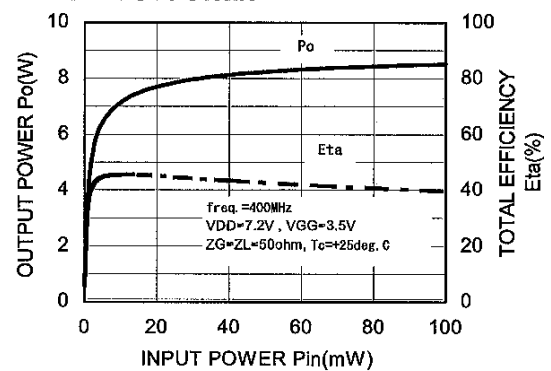
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



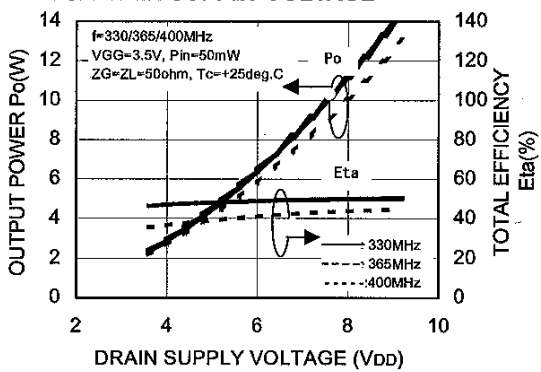
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



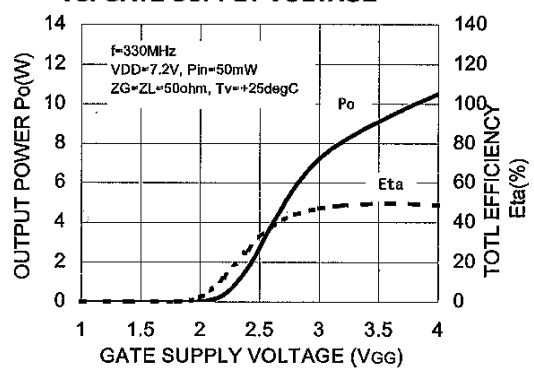
OUTPUT POWER, EFFICIENCY VS. INPUT POWER



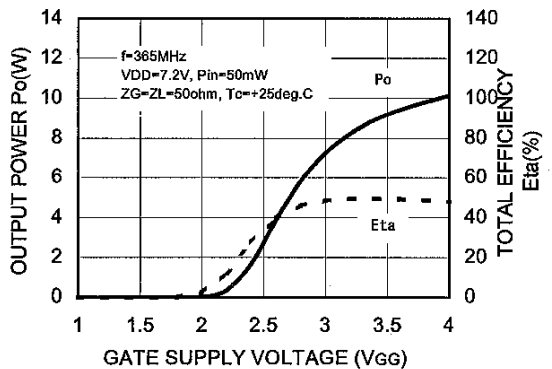
OUTPUT POWER, EFFICIENCY VS. DRAIN SUPPLY VOLTAGE



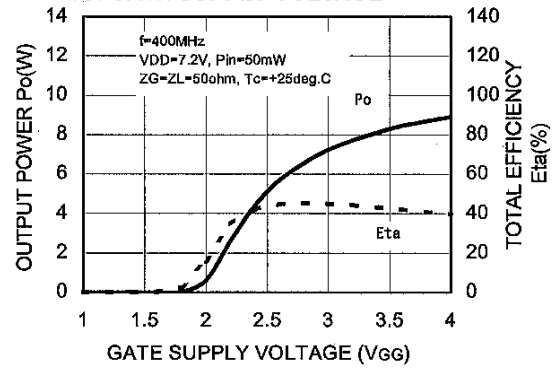
OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



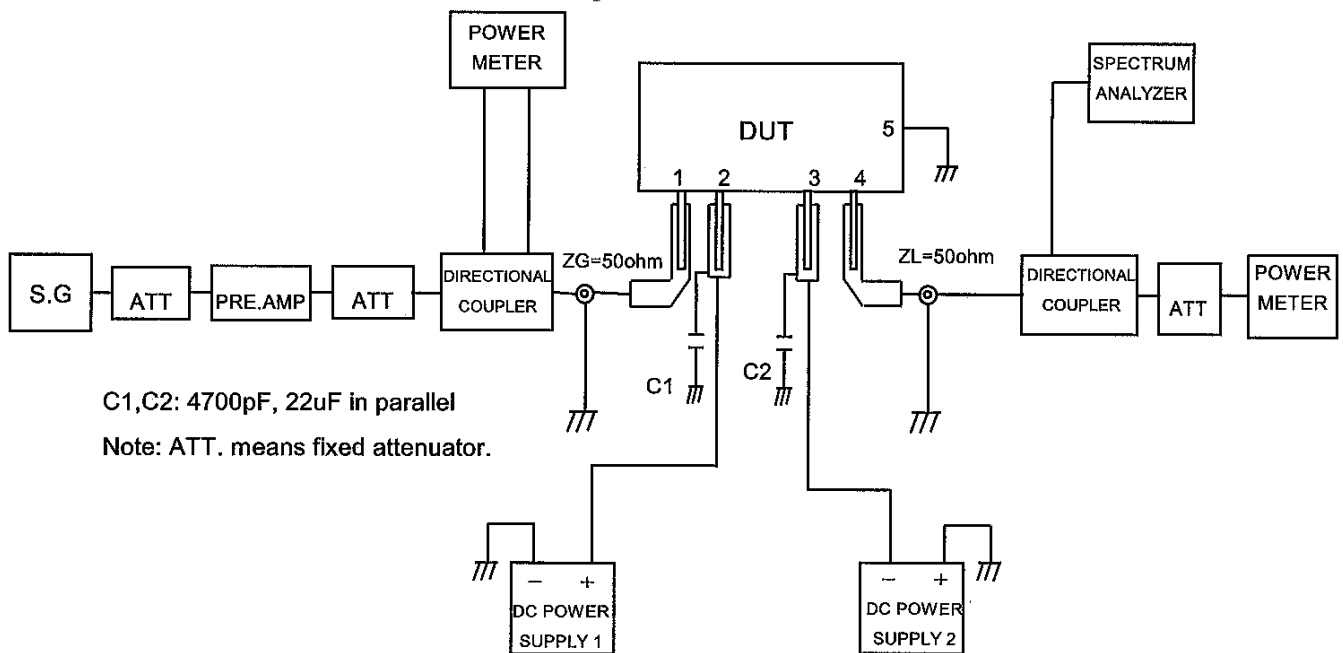
OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



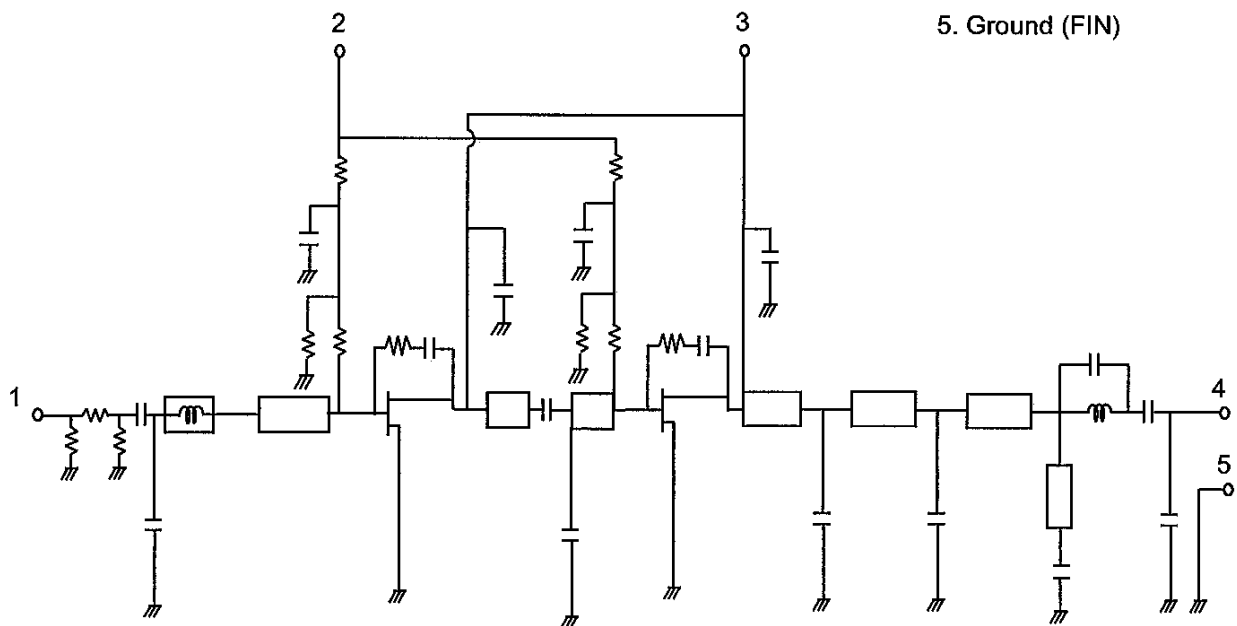
OUTPUT POWER, EFFICIENCY VS. GATE SUPPLY VOLTAGE



TEST BLOCK DIAGRAM



EQUIVALENT CIRCUIT



PINING

1. Input terminal
2. Vgg bias terminal
3. Vdd bias terminal
4. Output terminal
5. Ground (FIN)

RA07M3340M DESIGN CONSIDERATION OF HEAT RADIATION

A. Junction temperature

The condition at standard operation for each stage transistors are shown in Table 1.

Standard operation :

$$P_{out} = 7.0W, V_{dd} = 7.2V, P_{in} = 50mW,$$

$$\eta = 40 \% \text{ (min. rate)}$$

Table 1.

Stage	Vdd(V)	Idd(A)	Pin(W)	Pout(W)	Rth(j-c) (deg.C/W)
1st	7.20	0.55	0.05	2.0	4.50
Final	7.20	1.85	2.0	7.0	2.40

(1) Junction temperature of the 1st stage transistor

$$\begin{aligned} T_{j1} &= (V_{dd} \times I_{dd1} - P_{out1} + P_{in1}) \times R_{th1(j-c)} + T_{(case)} \\ &= (7.2 \times 0.55 - 2.0 + 0.05) \times 4.5 + T_{(case)} \\ &= 9.0 + T_{(case)} \text{ (deg.C)} \end{aligned}$$

(2) Junction temperature of the 2nd stage transistor

$$\begin{aligned} T_{j2} &= (V_{dd} \times I_{dd2} - P_{out2} + P_{in2}) \times R_{th2(j-c)} + T_{(case)} \\ &= (7.2 \times 1.85 - 7.0 + 2.0) \times 2.40 + T_{(case)} \\ &= 20.0 + T_{(case)} \text{ (deg.C)} \end{aligned}$$

B. Heat sink design

In thermal design of heat sink, keep the case temperature below 90 deg.C

at $P_{out} = 7.0W$ standard operation and ambient temperature 60 deg.C.

The thermal resistance R_{th} (case - air) of the heat sink to realize this :

$$\begin{aligned} R_{th} \text{ (case - air)} &= (T_{case} - T_{air}) / ((P_{out} / \eta) - P_{out} + P_{in}) \\ &= (90 - 60) / ((7.0 / 0.40) - 7.0 + 0.05) \\ &= 2.84 \text{ (deg.C / W)} \end{aligned}$$

Note : Including the contact thermal resistance between device and heat sink.

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistors become :

$$\begin{aligned} T_{j1} &= 99.0 \text{ (deg.C)} \\ T_{j2} &= 110.0 \text{ (deg.C)} \\ &\text{at } T_{(air)} = 60 \text{ deg.C, } T_{(case)} = 90 \text{ deg.C} \end{aligned}$$

Since the annual average of ambient temperature is 30 deg.C, junction temperature of each transistors become :

$$\begin{aligned} T_{j1} &= 69.0 \text{ (deg.C)} \\ T_{j2} &= 80.0 \text{ (deg.C)} \end{aligned}$$

As the maximum junction temperature of these incorporated transistors T_{jmax} are 175 deg.C, application under debated conditions is ensured.