

RMPA19000

18-22 GHz Power Amplifier MMIC

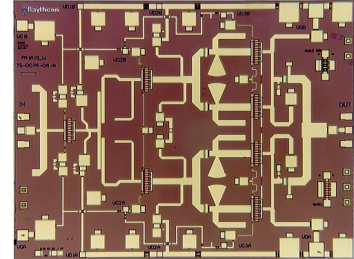
PRODUCT INFORMATION

Description

The Raytheon RMPA19000 is a high efficiency driver amplifier designed for use in point to point radio, point to multi-point communications and other millimeter wave applications. The RMPA19000 is a 3-stage GaAs MMIC amplifier utilizing Raytheon's advanced 0.15 μ m gate length Power PHEMT process and can be used in conjunction with other driver or power amplifiers to achieve the required total power output.

Features

- ◆ 28 dB small signal gain (typ.)
- ◆ 29 dBm saturated power out (typ.)
- ◆ Circuit contains individual source Vias
- ◆ Chip Size 4.45 mm x 3.50 mm

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Positive DC Voltage (+5 V Typical)	V _d	+ 6	Volts
Negative DC Voltage	V _g	- 2	Volts
Simultaneous (V _d - V _g)	V _{dg}	+ 8	Volts
Positive DC Current	I _D	1092	mA
RF Input Power (from 50 Ω source)	P _{IN}	+10	dBm
Operating Base plate Temperature	T _C	-30 to +85	°C
Storage Temperature Range	T _{Stg}	-55 to +125	°C
Thermal Resistance (Channel to Backside)	R _{jc}	16	°C/W

Electrical Characteristics

(At 25°C) 50 Ω system,
V_d=+5 V, Quiescent
current (I_{dq})=600 mA

Parameter	Min	Typ	Max	Unit
Frequency Range	18		22	GHz
Gate Supply Voltage (V _g) ¹		-0.2		V
Gain Small Signal at Pin=-5 dBm	22	26		dB
Gain Variation vs. Frequency		+/-1		dB
Power Output at 1 dB Compression		28		dBm
Power Output Saturated: (Pin=+5 dBm)	26	29		dBm
Drain Current at Pin=-5 dBm		600		mA

Parameter	Min	Typ	Max	Unit
Drain Current at P1 dB Compression		660		mA
Power Added Efficiency (PAE): at P1dB		15		%
OIP3		37		dBm
Input Return Loss (Pin=-5 dBm)		8		Db
Output Return Loss (Pin=-5 dBm)		10		dB

Note:

1. Typical range of the negative gate voltages is -0.9 to 0.0V to set typical I_{dq} of 600 mA.

Characteristic performance data and specifications are subject to change without notice.

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment for power devices should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC Ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist-grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typically 2 mils gap between the chip and the substrate material.

Figure 1
Functional
Block Diagram

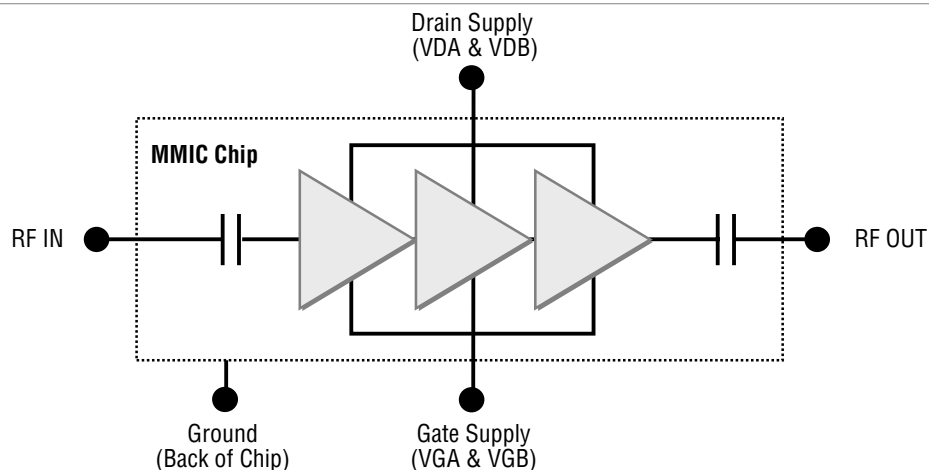
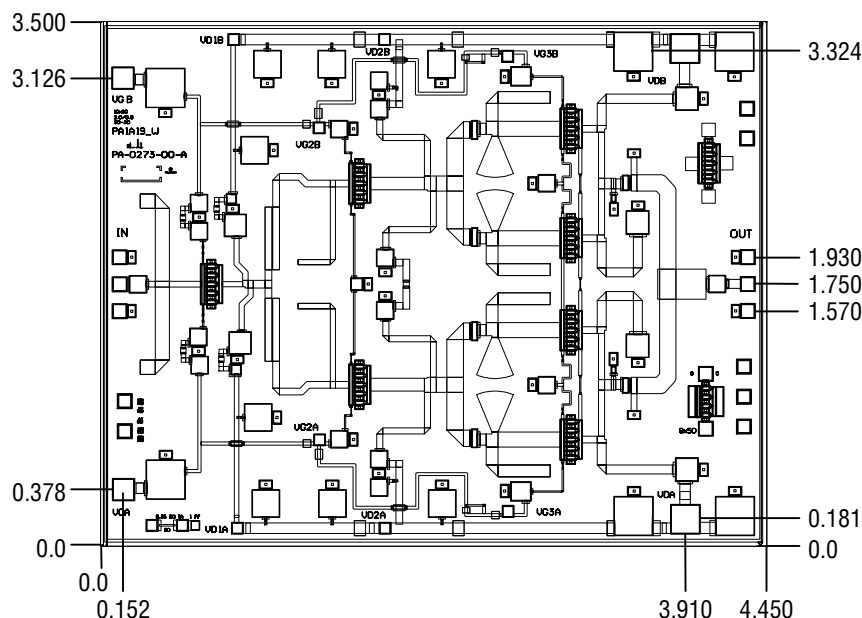


Figure 2
Chip Layout and Bond
Pad Locations

(Chip Size=4.450 mm
x 3.500 mm x 50 μ m.
Back of Chip is RF and
DC Ground)

Dimensions in mm



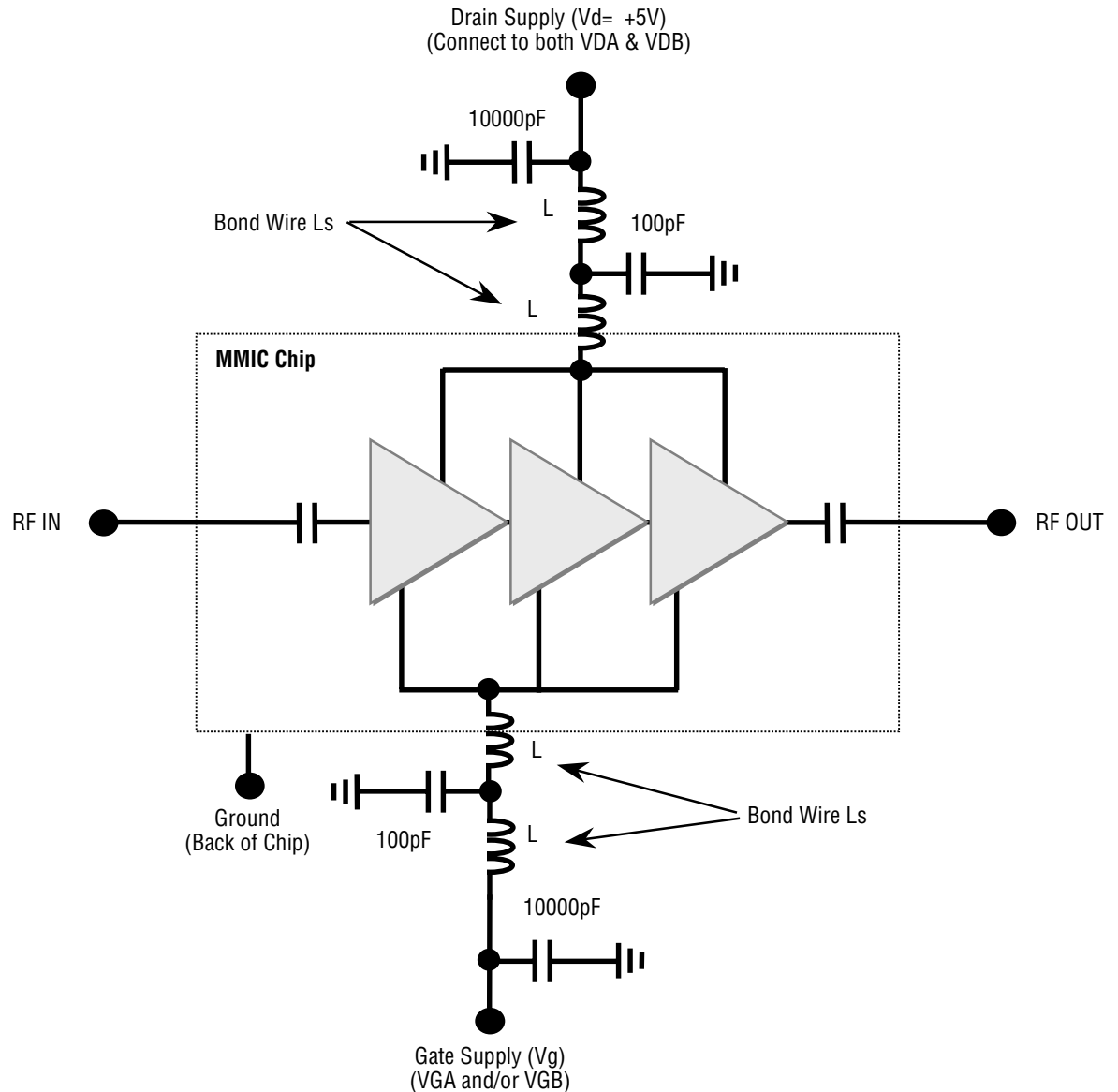
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Figure 3
Recommended
Application Schematic
Circuit Diagram



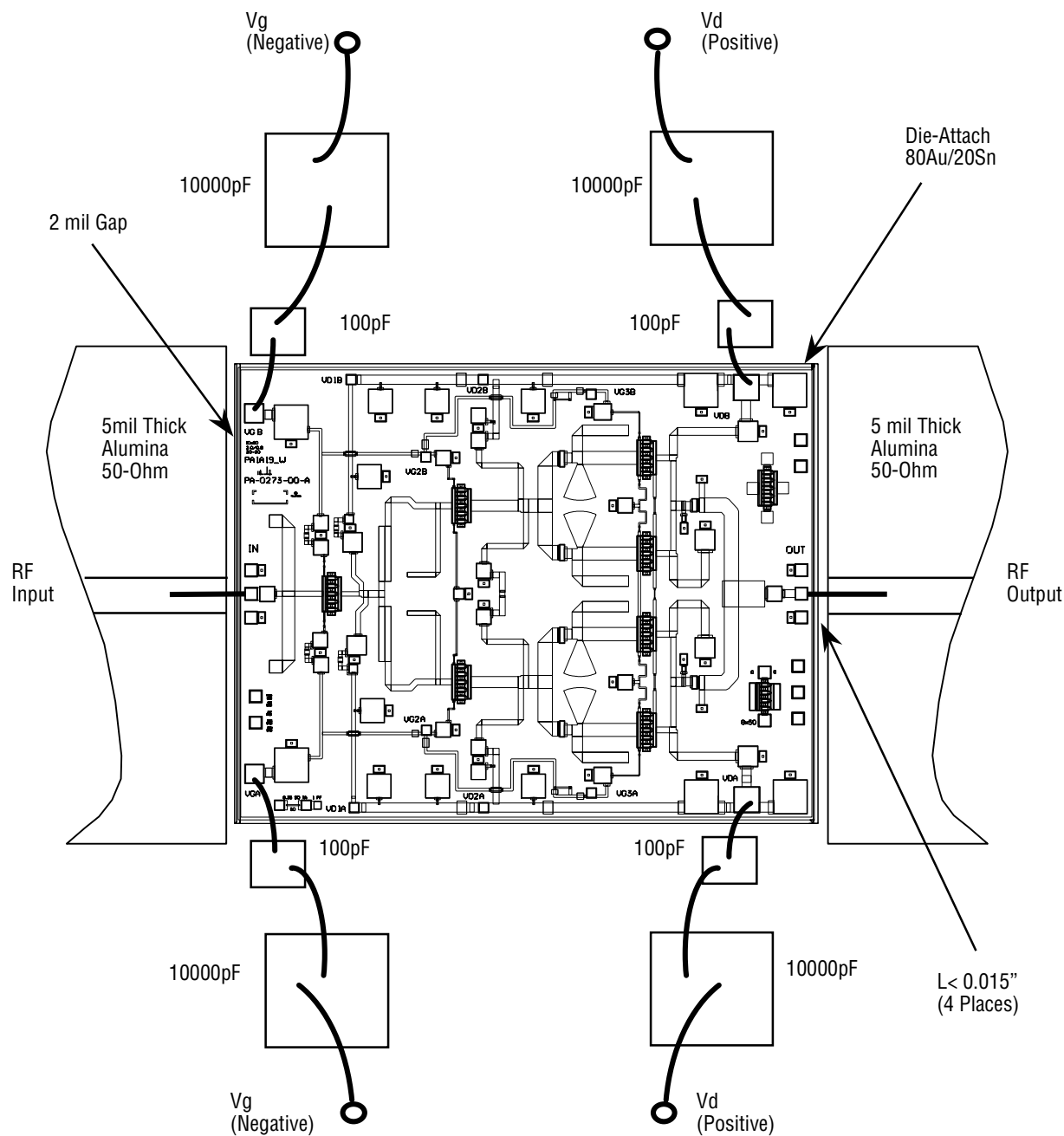
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Figure 4
Recommended
Assembly and
Bonding Diagram



Note:

Use 0.003" x 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief. Vd should be biased from 1 supply on both sides as shown. Vg can be biased from either or both sides from 1 supply.

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Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the ground of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5 V to V_g .

Step 3: Slowly apply positive drain bias supply voltage of +5 V to V_d .

Step 4: Adjust gate bias voltage to set the quiescent current of $I_{dq}=600$ mA.

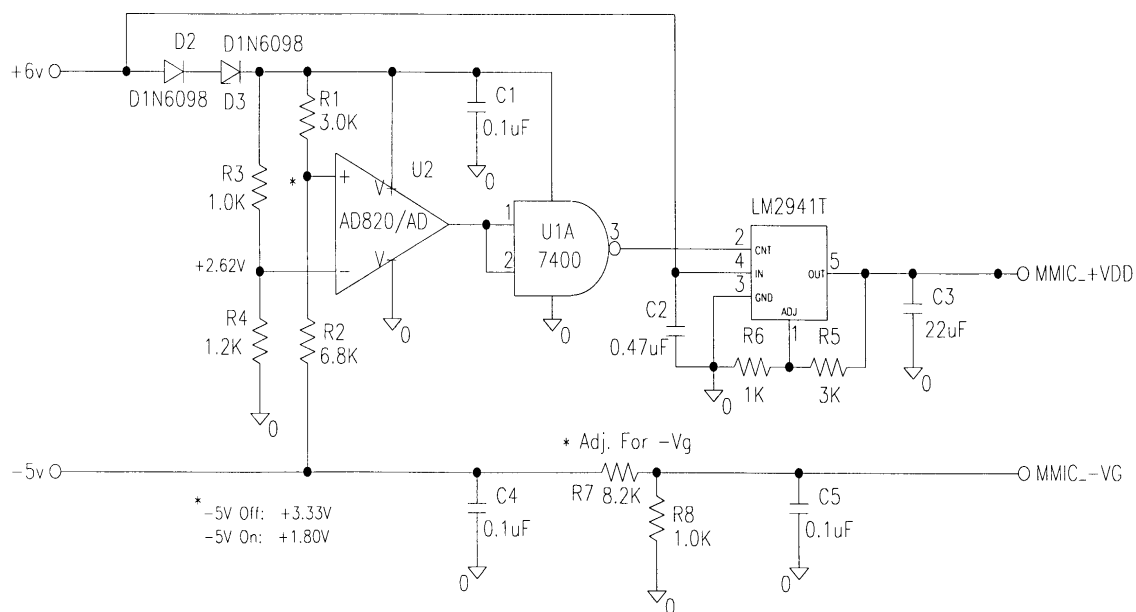
Step 5: After the bias condition is established, the RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

- (i) Turn off RF input power.
- (ii) Turn down and off drain voltage (V_d).
- (iii) Turn down and off gate bias voltage (V_g).

Note:

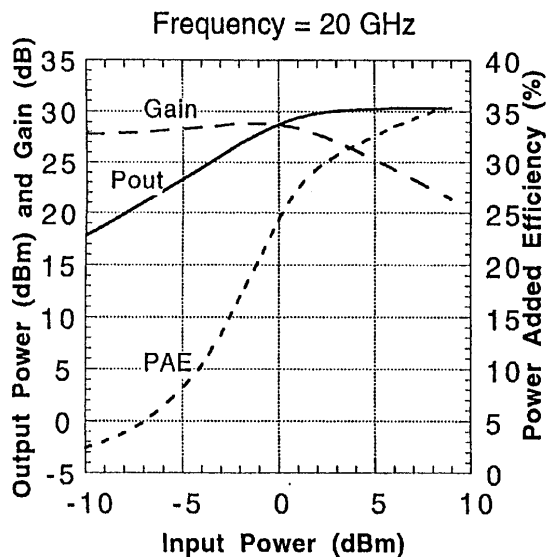
An example auto bias sequencing circuit to apply negative gate voltage and positive drain voltage for the above procedure is shown below.



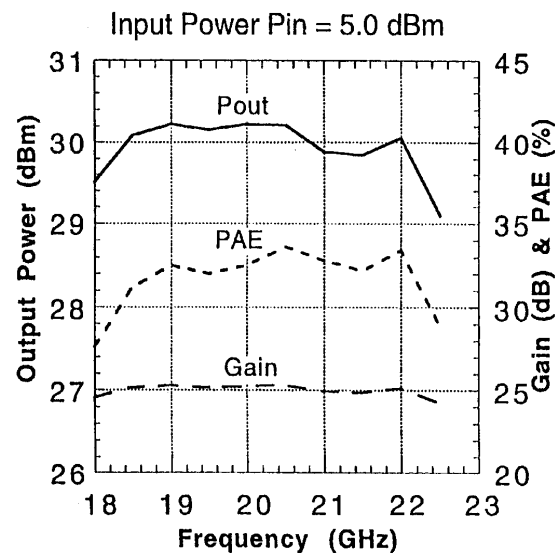
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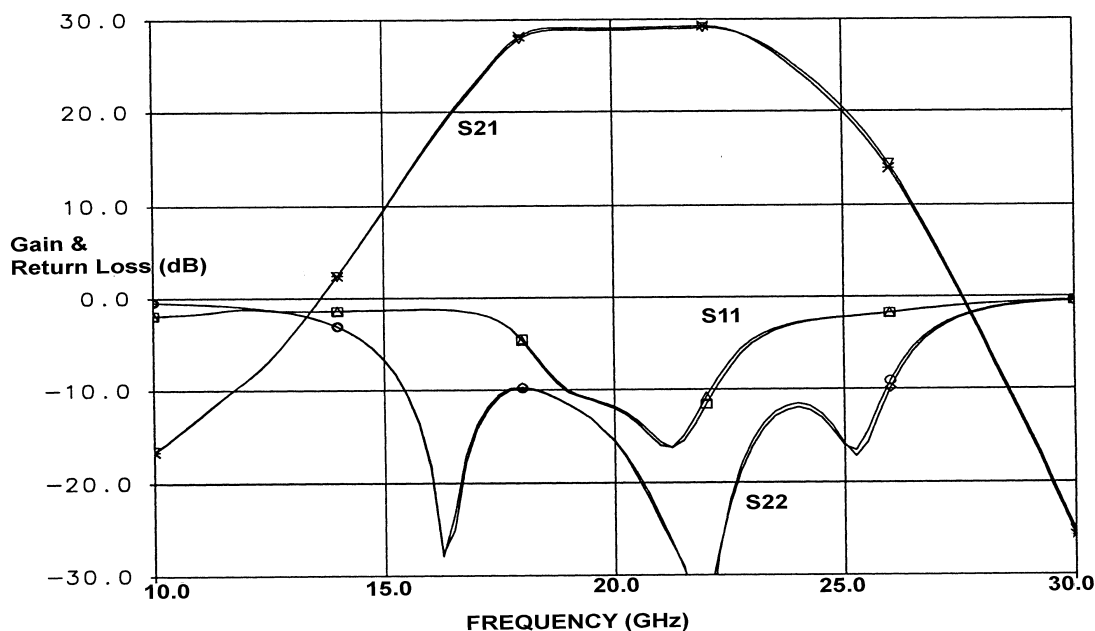
RMIPA19000 Gain, Power Out Vs. Power In
Bias $V_d=5$ V, $I_d=600$ mA, $T=25$ °C



RMIPA19000 Pout, PAE, Gain Vs. Freq
Bias $V_d=5$ V, $I_d=600$ mA, $T=25$ °C



RMIPA19000 S21, S11, S22 Mag Vs. Freq.
Bias $V_d=5$ V, $I_d=600$ mA, $T=25$ °C



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