Raytheon

RMBA09500-58

Cellular 2 Watt Linear GaAs MMIC Power Amplifier

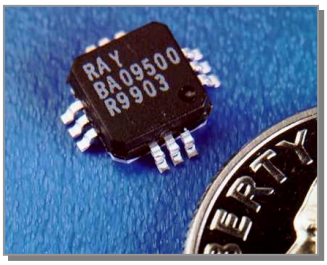
ADVANCED INFORMATION

Description

The RMBA09500 is a high power, highly linear Power Amplifier. The two stage circuit uses Raytheon's pHEMT process. It is designed for use as a driver stage for Cellular base stations, or as the output stage for Micro- and Pico-Cell base stations. The amplifier has been optimized for high linearity requirements for CDMA operation. The device is matched for 50 ohms input impedance.

Features

- 2 Watt Linear output power at 37 dBc ACPR1 for CDMA operation
- Small Signal Gain of > 30 dB
- Small outline SMD package



Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Typical	Max	Units
Drain Supply Voltage	V_{DD}			+10	V
Gate Supply Voltage	V_{GS}			-5	V
RF Input Power (50 ohm Source)	P_{RF}			+5	dBm
Case Operating Temperature	T_C	-30		+85	°C
Storage Temperature	T_S	-40		+100	°C

Electrical Characteristics[2]

Parameter	Min	Typ	Max	Unit
Frequency Range	869		894	MHz
Gain (small signal)		32		dB
Gain variation:				
Over frequency range		+/-1.5		dB
Over temperature range		+/-2.5		dB
Noise Figure		6		dB
Linear output power:				
for CDMA [3]	33			dBm
Saturated output power		38		dBm

Parameter	Min	Typ	Max	Unit
PAE		20		%
Input VSWR (50Ω)		2:1		
RF Input Power		+1		dBm
Drain Voltage (V_{DD})		7.0		Volts
Gate Voltage (V_{GS}) [4]		-3		Volts
Quiescent current				
(IDQ1, IDQ2)		150, 400		mA
Thermal Resistance				
(Channel to Case) Rjc		11		°C/W

Notes:

1. Not with RF power simultaneously applied.
2. 50 ohm system, V_{DD} = 7.0V, T = 25°C
3. 9 Channel Forward Link QPSK Source; 1.23 Mbps modulation rate. ACPR1 measured at 885 KHz offset at a value ≥ 37 dBc. CDMA Waveform measured using the ratio of the average power within the 1.23 MHz channel and within a 30 kHz bandwidth at an 885 MHz offset.
4. Gate Voltage can be adjusted to optimize the linearity of the amplifier for differing modulation systems. Default biasing is optimized for CDMA (Ref. Note 2).

Characteristic performance data and specifications are subject to change without notice.

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Andover, MA 01810

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Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

The following describes a procedure for evaluating the RMBA09500-58, a monolithic high efficiency power amplifier, in a surface mount package, designed for use as a driver stage for Cellular base stations, or as the final output stage for Micro- and Pico-Cell base stations. Figure 1 shows the package outline and the pin designations. Figure 2 shows the functional block diagram of the packaged product. It should be noted that RMBA09500-58 requires external passive components for DC bias and RF output matching circuits. A recommended schematic circuit is shown in Figure 3. The gate biases for the two stages of the amplifier may be set by simple resistive voltage dividers. Figure 4 shows a typical layout of an evaluation board, corresponding to the schematic circuits of figure 3. The following designations should be noted:

(1) Pin designations are as shown in figure 2.

(2) Vg1 and Vg2 are the Gate Voltages (negative) applied at the pins of the package

(3) Vgg1 and Vgg2 are the negative supply voltages at the evaluation board terminals

(4) Vd1 and Vd2 are the Drain Voltages (positive) applied at the pins of the package

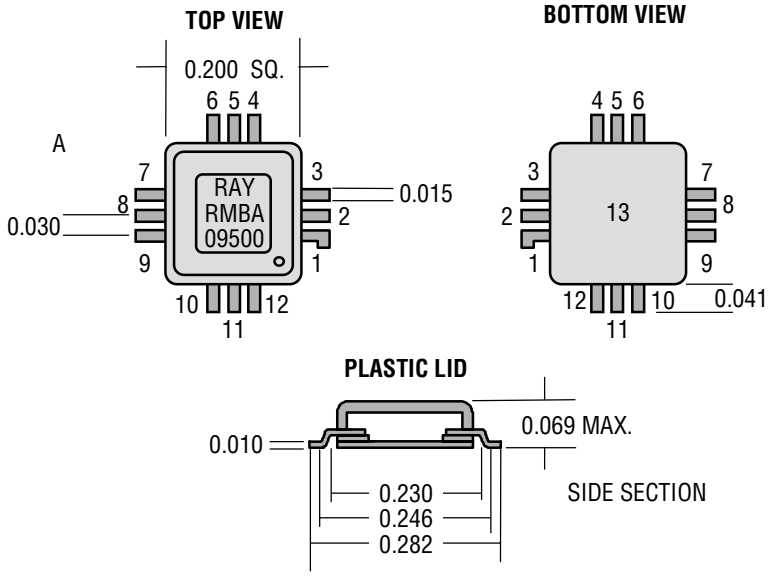
(5) Vdd1 and Vdd2 are the positive supply voltages at the evaluation board terminals

Note: The 2 terminals of Vdd1 and Vdd2 may be tied together.

The base of the package must be soldered on to a heat sink for proper operation.

Figure 1
Package Outline and Pin Designations

Dimensions in inches



Pin #	Description
1	RF Out & Vd2
2	RF Out & Vd2
3	RF Out & Vd2
4	AC Ground (g2)
5	GND
6	AC Ground (g1)
7	GND
8	RF Input
9	GND
10	Vd1
11	Vg2
12	Vg1
13	GND (METAL BASE)

Figure 2
Functional Block Diagram of Packaged Product

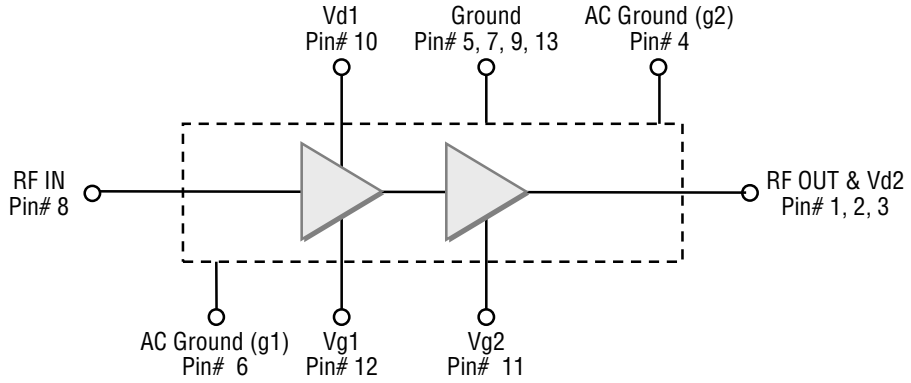


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Figure 3
Schematic of Application Circuit showing external components

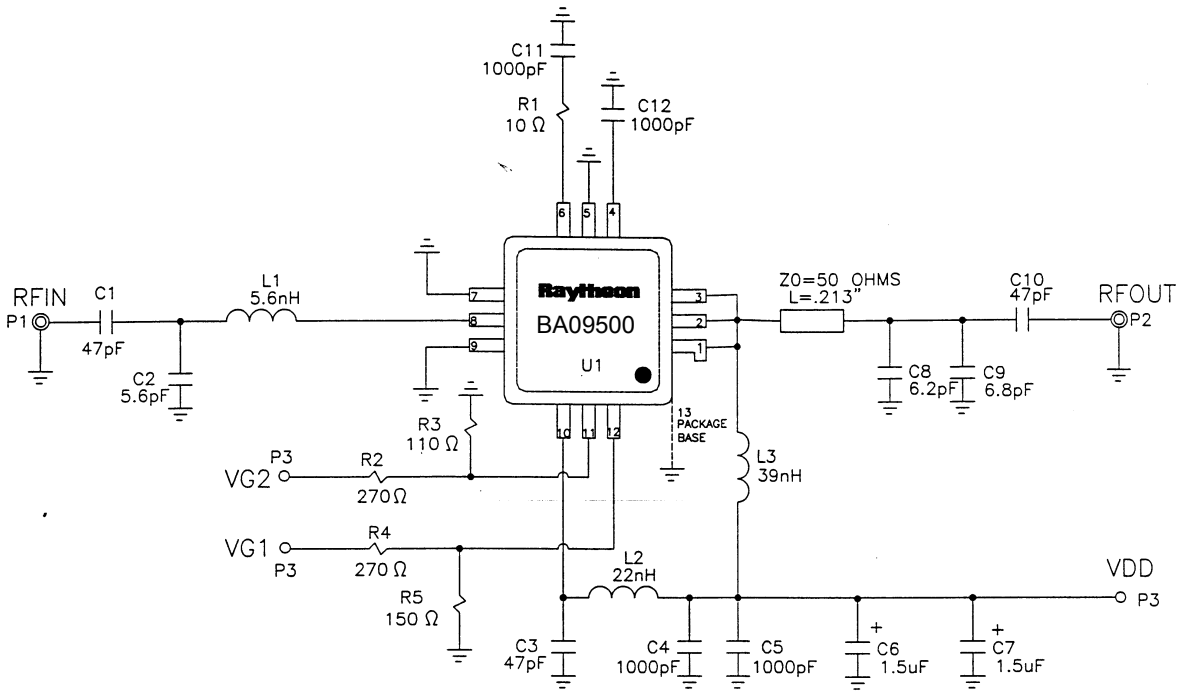
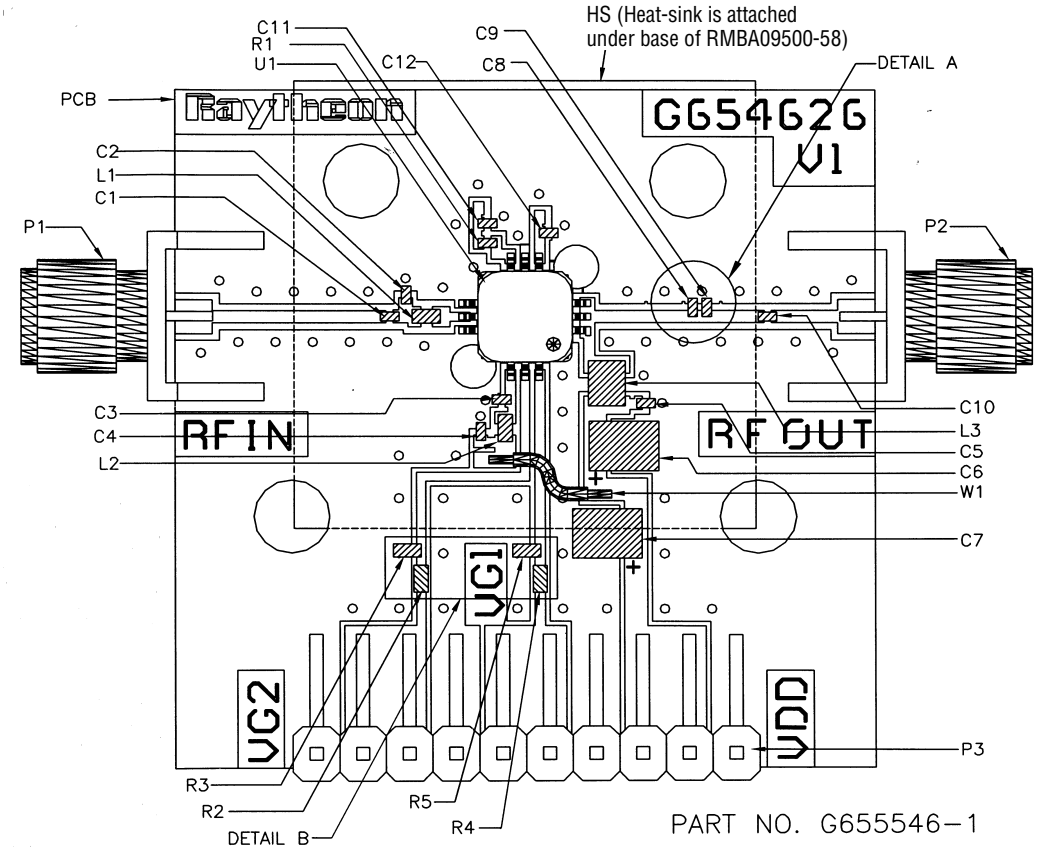


Figure 4
Layout of Test Evaluation Board (RMBA09500-58-TB)



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Test Procedure
for the evaluation board (RMBA09500-58-TB)

CAUTION: LOSS OF GATE VOLTAGES (VG1, VG2) WHILE CORRESPONDING DRAIN VOLTAGES (Vdd) ARE PRESENT CAN DAMAGE THE AMPLIFIER.

The following sequence must be followed to properly test the amplifier. (It is necessary to add a fan to provide air cooling across the heat sink of RMBA09500.) Note: Vdd1, 2 are tied together.

Step 1: Turn off RF input power.

Step 2: Use GND terminal of the evaluation board for the ground of the DC supplies. Slowly apply gate supply voltages as specified on results sheet supplied with test board to the board terminals Vgg1 and Vgg2.

Step 3: Slowly apply drain supply voltages of +7.0 V to the board terminals Vdd1, 2. Adjust Vgg to set the total quiescent current Idq1 and Idq2 (with no RF applied) Idq as per supplied result sheet. Gate supply voltages (Vgg i.e., Vgg1, Vgg2) may be adjusted, only if quiescent current (Idq1 and Idq2) values desired are different from those noted on the data summary supplied with product samples.

Step 4: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band and appropriate power level.

Step 5: Follow turn-off sequence of:

(i) Turn off RF Input Power

(ii) Turn down and off drain voltages Vdd1, 2.

(iii) Turn down and off gate voltages Vgg1 and Vgg2.

Parts List
for Test Evaluation Board (RMBA09500-58-TB, G654188/G654942)

Part	Value	EIA Size	Vendor(s)
C1,C3,C10	47 pF	0402	Murata, GRM36COG470J050
C2	5.6 pF	0402	Murata, GRM36COG5R6B050
C8	6.2 pF	0402	Murata, GRM36COG6R2B050
C9	6.8 pF	0402	Murata, GRM36COG6R8B050
C4,C5,C11,C12	1000 pF	0402	Murata, GRM36X7R102K050
C6,C7	1.5 uF	3528	Kemet (T494B155K020AS)
L1	5.6 nH	0603	Toko, LL1608-FH5N6S
L2	22 nH	0603	Toko, LL608-FH22NK
L3	39 nH	1008	Coilcraft, 1008HS-390TKBC
R1	10 Ohm	0402	IMS, RCI-0402-10R0J
W1	26AWG (0.015” dia) Wire		Alpha, 2853/1
U1	RMBA09500-58, 3.5V PA		Raytheon, G654257
P3	Right angle Pin Header		3M (2340-5211TN)
P1,P2	SMA Connectors		Johnson Components (142-0701-841)
Board	FR4		Raytheon Dwg# G654626, V1
R2, R4	270 ohm	0402	IMS RCI 0402 2700J
R3	110 ohm	0402	IMS RCI 0402 1100J
R5	150 ohm	0402	IMS RCI 0402 1500J

Recommendations
for Heat-Sinking the RMBA09500-58

Use SN92 solder to attach the device to a small copper pedestal at 185°C for 10 seconds. The copper pedestal should be flush with the top surface of the PWB and be soldered to the rear side of the PWB again using SN92 at 185°C with a sufficient flange to allow attachment of the pedestal, PWB and MMIC to a suitable heat-sink. This operation will assure that the total thermal resistance of the MMIC to the heat-sink is 13°C/watt and the junction temperature is below 150°C at a case temperature of 85°C.

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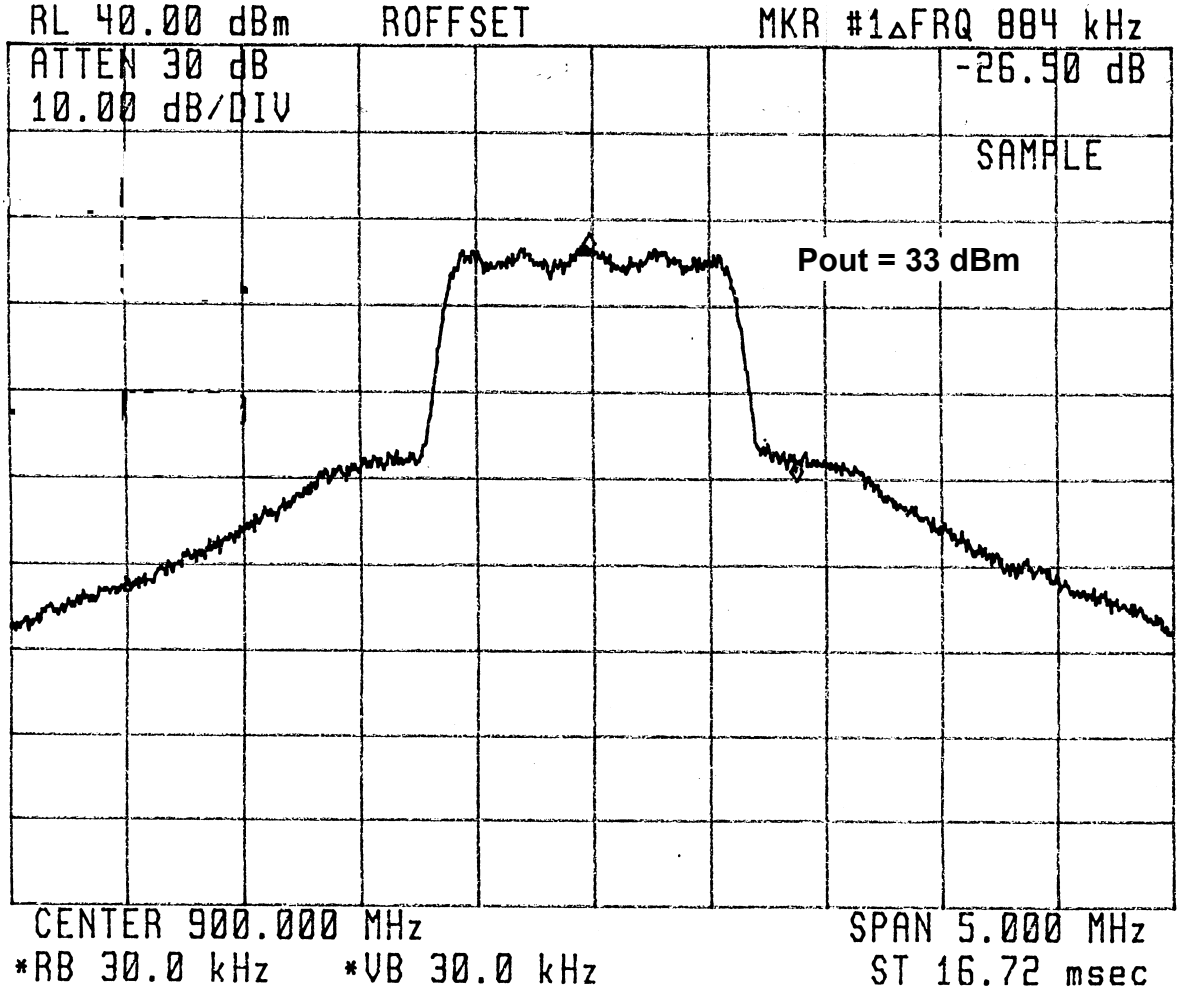
Performance Data

CDMA: 9 Channel Forward Link



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