I²CBus SERIAL INTERFACE REAL TIME CLOCK

RS5C372A

APPLICATION MANUAL

RICOH

ELECTRONIC DEVICES DIVISION

NO.EA-044-9803

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June 1995

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CONTENTS

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OUTLINE

The RS5C372A is a CMOS type real-time clock which is connected to the CPU via 2-wires and capable of serial transmission of clock and calendar data to the CPU.

The RS5C372A can generate various periodic interrupt clock pulses lasting for long period (one month), and alarm interrupt can be made by days of the week, hours, and minutes by two incorporated systems. Since an oscillation circuit is driven at a constant voltage, it undergoes fluctuations of few voltage and consequently offers low current consumption (TYP. 0.5µA at 3V). It also provides an oscillator halt sensing function applicable for data validation at power-on and other occasions and 32kHz clock output for an external micro computer. The product also incorporates a time trimming circuit that adjusts the clock with higher precision by adjusting any errors in crystal oscillator frequencies based on signals from the CPU. The crystal oscillator may be selected from 32.768kHz or 32.000kHz types. Integrated into an ultra compact and ultra thin 8 pin SSOP package, the RS5C372A is the optimum choice for equipment requiring small sized and low power consuming products.

FEATURES

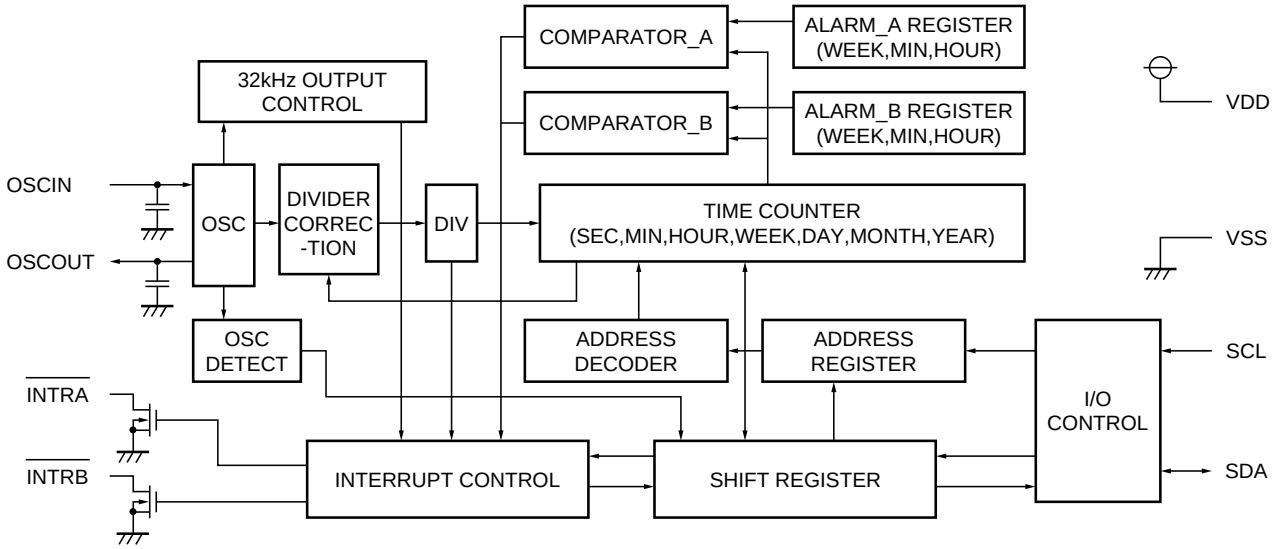
- Time keeping voltage: 1.45V to 6.0V
- Lowest supply current: 0.5µA TYP. (0.9µA MAX.) : 3V (25˚C)
  (1.0µA MAX.) : 3V (–40 to +85˚C)
- Connected to the CPU via only 2-wires (I²CBus Interface, MAX.400kHz, address 7bit)
- A clock counter (counting hours, minutes, and seconds) and a calendar counter (counting leap years, years, months, days, and days of the week) in BCD codes
- Interrupt to the CPU (period of one month to one second, interrupt flag, interrupt halt function) ($\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$)
- Two systems of alarm functions (days of the week, hours, and minutes) ($\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$)
- Oscillation halt sensing to judge internal data validity
- Clock output of 32.768kHz (32.000kHz) (output controllable via a register)
- Second digit adjustment by ±30 seconds
- Automatic leap year recognition up to the year 2099
- 12-hour or 24-hour time display selectable
- Oscillation stabilizing capacity (C_G, C_D) incorporated
- High precision time trimming circuit
- Oscillator of 32.768kHz or 32.000kHz may be used
- CMOS logic
- Package: 8pin SSOP

Note

· I²CBus is a trademark of PHILIPS ELECTRONICS N.V.

· Purchase of I²C components of Ricoh Company, Ltd. conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system comforms to the I²C Standard Specification as defined by Philips.

BLOCK DIAGRAM



APPLICATIONS

- Communication devices (multi function phone, portable phone, PHS or pager)
- OA devices (fax, portable fax)
- Computer (desk-top and mobile PC, portable word-processor, PDA, electric note or video game)
- AV components (portable audio unit, video camera,camera, digital camera or remote controller)
- Home appliances (rice cooker, electric oven)
- Other (car navigation system, multi-function watch)

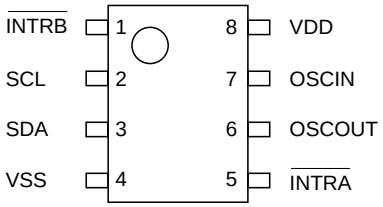
SELECTION GUIDE

One of two RS5C372As can be selected based on IC direction on taping. (E2 is standard.)

Part Number : RS5C372A-E1, RS5C372A-E2

PIN CONFIGURATION

• 8pin SSOP (0.65mm pitch)



PIN DESCRIPTIONS

Pin No.	Symbol	Name	Description
2	SCL	Serial clock line	This pin is used to input shift clock pulses to synchronize data input/output to and from the SDA pin with this clock. Up to 6V beyond V_{DD} may be input.
3	SDA	Serial data line	This pin inputs and outputs written or read data in synchronization with shift clock pulses from the SCL pin. Up to 6V beyond V_{DD} may be input. This pin functions as an Nch open drain output.
5	$\overline{\text{INTRA}}$	Interrupt output A	This pin outputs periodic interrupt pulses and alarm interrupt (ALARM_A, ALARM_B) to the CPU. This pin is off when power is activated from 0V. This pin functions as an Nch open drain output.
1	$\overline{\text{INTRB}}$	Interrupt output B	This pin outputs 32.768kHz clock pulses (when 32.768kHz crystal is used), periodic interrupt pulses to the CPU or alarm interrupt (ALARM_B). It outputs 32.768kHz when power source is activated from 0V. This pin functions as an Nch open drain output.
7 6	OSCIN OSCOUT	Oscillator circuit input/output	These pins configure an oscillator circuit by connecting a 32.768kHz or 32.000kHz crystal oscillator between the OSCIN–OSCOUT pins. (Any other oscillator circuit components are built into the RS5C372A.)
8 4	VDD VSS	Positive power supply input Negative power supply input	The V_{DD} pin is connected to the positive power supply and Vss to the ground.

ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Symbol	Item	Conditions	Ratings	Unit
V_{DD}	Supply voltage		–0.3 to +7.0	V
V_I	Input voltage	SCL, SDA	–0.3 to +7.0	V
V_{O1}	Output voltage 1	SDA	–0.3 to +7.0	V
V_{O2}	Output voltage 2	$\overline{\text{INTRA}}$, $\overline{\text{INTRB}}$	–0.3 to +12	
P_D	Power dissipation	T_{opt}=25˚C	300	mW
Topt	Operating temperature		–40 to +85	˚C
Tstg	Storage temperature		–55 to +125	˚C

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are threshold limit values that must not be exceeded even for an instant under any conditions. Moreover, such values for any two items must not be reached simultaneously. Operation above these absolute maximum ratings may cause degradation or permanent damage to the device. These are stress ratings only and do not necessarily imply functional operation below these limits.

RECOMMENDED OPERATING CONDITIONS

(Vss=0V, Topt=–40 to +85˚C)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{DD}	Supply voltage		2.0		6.0	V
V_{CLK}	Time keeping voltage		1.45		6.0	V
F_{XT}	Oscillation frequency			32.768 or 32.000		kHz
V_{PUP1}	Pull-up voltage 1	SCL, SDA			6.0	V
V_{PUP2}	Pull-up voltage 2	$\overline{INTRA}$, $\overline{INTRB}$			10.0	V

DC CHARACTERISTICS

Unless otherwise specified: Vss=0V, V_{DD}=3V, Topt=–40 to +85˚C, Oscillation frequency=32.768kHz, or 32.000kHz(R_1=30kΩ)

Symbol	Item	Pin name	Conditions	MIN.	TYP.	MAX.	Unit
V_{IH}	"H" input voltage	SCL, SDA		0.8V_{DD}		6.0	V
V_{IL}	"L" input voltage	SCL, SDA		–0.3		0.2V_{DD}	V
I_{OL1}	Output current	$\overline{INTRA}$, $\overline{INTRB}$	V_{OL1}=0.4V	1			mA
I_{OL2}		SDA	V_{OL2}=0.6V	6			mA
I_{ILK}	Input leakage current	SCL	V_I=6V or Vss V_{DD}=6V	–1		1	µA
I_{OZ}	Output off state leakage current	SDA, $\overline{INTRA}$, $\overline{INTRB}$	V_O=6V or Vss V_{DD}=6V	–1		1	µA
I_{DD1}	Standby current	VDD	V_{DD}=3V, Topt=25˚C SCL, SDA=3V Output=OPEN*1		0.5	0.9	µA
I_{DD2}		VDD	V_{DD}=3V, Topt=–40 to +85˚C SCL, SDA=3V Output=OPEN*1			1.0	µA
I_{DD3}		VDD	V_{DD}=6V SCL, SDA=6V Output=Open*1		0.8	2.0	µA
C_G	Internal oscillation capacitance 1	OSCIN			10		pF
C_D	Internal oscillation capacitance 2	OSCOUT			10		pF

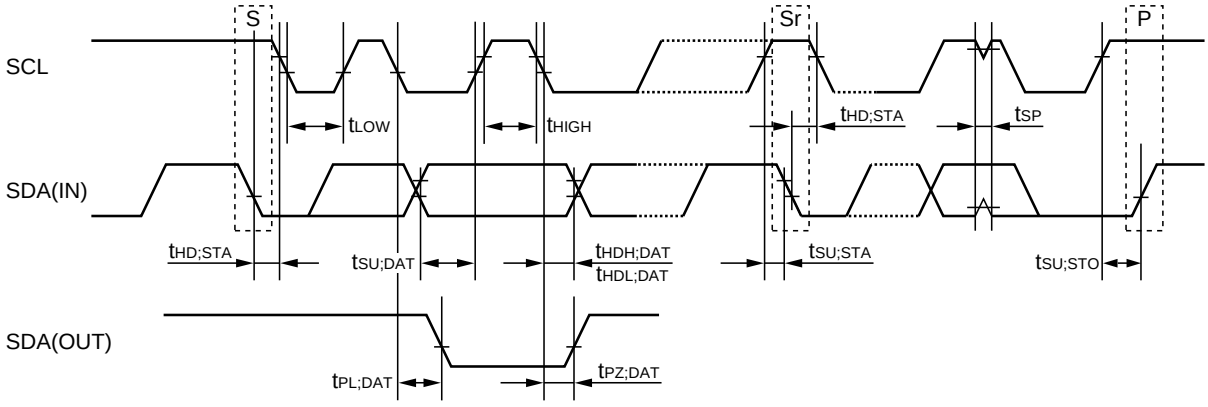
*1) The mode outputs no clock pulses when output is open (output off state).
For consumption current (output: no load) when 32kHz pulses are output from $\overline{INTRB}$, see "6. Typical Characteristic Measurements"

AC CHARACTERISTICS

• V_{DD}≥2.0V (supports standard mode I²CBus)

Unless otherwise specified : V_{SS}=0V, Topt=–40 to +85°C, Crystal=32.768kHz or 32.000kHz
I/O conditions: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, V_{OL}=0.2×V_{DD}, C_L=50pF

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
f_{SCL}	SCL clock frequency		0		100	kHz
t_{LOW}	SCL clock "L" time		4.7			µs
t_{HIGH}	SCL clock "H" time		4.0			µs
$t_{HD;STA}$	Start condition hold time		4.0			µs
$t_{SU;STO}$	Stop condition setup time		4.0			µs
$t_{SU;STA}$	Start condition setup time		4.7			µs
$t_{SU;DAT}$	Data setup time		250			ns
$t_{HDH;DAT}$	"H" data hold time		0			ns
$t_{HDL;DAT}$	"L" data hold time		35			ns
$t_{PL;DAT}$	SDA "L" stable time after falling of SCL				2.0	µs
$t_{PZ;DAT}$	SDA off stable time after falling of SCL				2.0	µs
t_R	Rising time of SCL and SDA (input)				1000	ns
t_F	Falling time of SCL and SDA (input)				300	ns
t_{SP}	Spike width that can be removed with input filter				50	ns



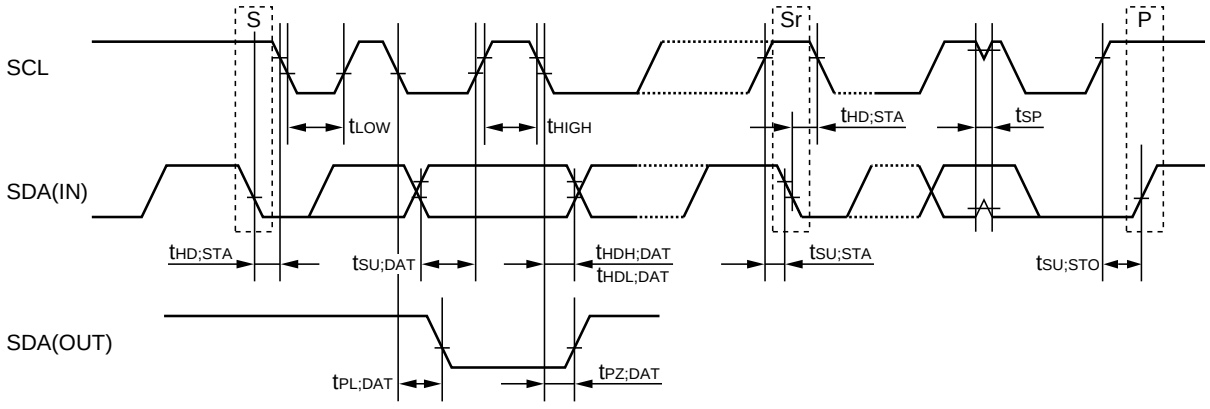
S Start condition
P Stop condition
Sr Repeated start condition

*) For detailed information refer to "OPERATION: 1.2 Transmission System of I²CBus."

• V_{DD}≥2.5V (supports fast mode I²CBus)

Unless otherwise specified : V_{SS}=0V, Topt=–40 to +85°C, Crystal=32.768kHz or 32.000kHz
I/O conditions: V_{IH}=0.8×V_{DD}, V_{IL}=0.2×V_{DD}, V_{OL}=0.2×V_{DD}, C_L=50pF

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
f_{SCL}	SCL clock frequency		0		400	kHz
t_{LOW}	SCL clock "L" time		1.3			µs
t_{HIGH}	SCL clock "H" time		0.6			µs
$t_{HD\ ;\ STA}$	Start condition hold time		0.6			µs
$t_{SU\ ;\ STO}$	Stop condition setup time		0.6			µs
$t_{SU\ ;\ STA}$	Start condition setup time		0.6			µs
$t_{SU\ ;\ DAT}$	Data setup time		100			ns
$t_{HDH\ ;\ DAT}$	"H" data hold time		0			ns
$t_{HDL\ ;\ DAT}$	"L" data hold time		35			ns
$t_{PL\ ;\ DAT}$	SDA "L" stable time after falling of SCL				0.9	µs
$t_{PZ\ ;\ DAT}$	SDA off stable time after falling of SCL				0.9	µs
t_R	Rising time of SCL and SDA (input)				300	ns
t_F	Falling time of SCL and SDA (input)				300	ns
t_{SP}	Spike width that can be removed with input filter				50	ns



S Start condition
P Stop condition
Sr Repeated start condition

*) For detailed information refer to "OPERATION: 1.2 Transmission System of I²CBus."

OUTLINE DESCRIPTION

1. Interfacing with the CPU

The RS5C372A reads/writes data over I²CBus interface via 2-wires: SDA (data) and SCL (clock). Since the output of the I/O pin of SDA is open drain, data interfacing with a CPU with different supply voltage is possible by applying pull-up resistor on the circuit board. The maximum clock frequency of 400kHz of SCL enables data transfer in I²CBus fast mode.

2. Clock function

The clock function of the RS5C372A allows write/read data from lower two digits of the dominical year to seconds to and from the CPU. When lower two digits of the dominical year are multiples of 4, the year is recognized as a leap year automatically. Up to the year 2099 leap years will be automatically recognized.

*) The year 2000 is a leap year while the year 2100 is not.

3. Alarm function

The RS5C372A has an alarm function that outputs an interrupt signal from $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ output pins to the CPU when the day of the week, hour or minute corresponds to the setting. These two systems of alarms (ALARM_A, ALARM_B), each may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for each day of the week, thus allowing outputting alarm everyday or on a specific day of the week.
The ALARM_A is output from the $\overline{\text{INTRA}}$ pin while the ALARM_B is output from either the $\overline{\text{INTRA}}$ or the $\overline{\text{INTRB}}$ pins. Polling is possible separately for each alarm system.

4. High precision time trimming function

The RS5C372A has an internal oscillation circuit capacitance C_G and C_D so that an oscillation circuit may be configured simply by externally connecting a crystal. Either 32.768kHz or 32.000kHz may be selected as a crystal oscillator by setting the internal register appropriately. The RS5C372A incorporates a time trimming circuit that adjusts gain or loss of the clock from the CPU up to approx. ±189ppm (±194ppm when 32.000kHz crystal is used) by approximately 3ppm steps to correct discrepancy in oscillation frequency. (Error after correction: ±1.5ppm: 25°C)
Thus by adjusting frequencies for each system,

- Clock display is possible at much higher precision than conventional real-time clock while using a crystal with broader fluctuation in precision.
- Even seasonal frequency fluctuation may be corrected by adjusting seasonal clock error.
- For those systems that have temperature detection precision of clock function may be increased by correcting clock error according to temperature fluctuations.

5. Oscillation halt sensing

The oscillation halt sensing function uses a register to store oscillation halt information. This function may be used to determine if the RS5C372A supply power has been booted from 0V and if it has been backed up. This function is useful for determining if clock data is valid or invalid.

6. Periodic interrupt

The RS5C372A can output periodic interrupt pulses in addition to alarm function from the $\overline{\text{INTRA}}$ and $\overline{\text{INTRB}}$ pins. This frequency may be selected from 2Hz (every 0.5 seconds), 1Hz (every second), 1/60Hz (every minute), 1/3600Hz (every hour) and monthly (1st of month).

Output wave form for periodic interrupt may be selected from regular pulse waveform (2Hz and 1Hz) and waveforms (every second, every minute, every hour and every month) that are appropriate for CPU level interrupt. Outputs may be selected either $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$. The RS5C372A has polling function that monitors pin status in the register.

7. 32kHz clock output

The RS5C372A may output oscillation frequency from the $\overline{\text{INTRB}}$ pin. This clock output is set for output by default, which is set to on or off by setting the register.

Note

The year-digit counter of RS5C372A counts only lower two digits of a year and no counter is supplied for upper two digits. When you are going to use this product in a system that must cope with “2000 year problem” which shall be corrected by software.

FUNCTIONAL DESCRIPTIONS

1. Allocation of Internal Addresses

	Internal address				Contents	Data*1							
	A_3	A_2	A_1	A_0		D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	Second counter	—*2	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1
1	0	0	0	1	Minute counter	—	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1
2	0	0	1	0	Hour counter	—	—	H_{20} $P/\overline{A}$	H_{10}	H_8	H_4	H_2	H_1
3	0	0	1	1	Day of the week counter	—	—	—	—	—	W_4	W_2	W_1
4	0	1	0	0	Day counter	—	—	D_{20}	D_{10}	D_8	D_4	D_2	D_1
5	0	1	0	1	Month counter	—	—	—	MO_{10}	MO_8	MO_4	MO_2	MO_1
6	0	1	1	0	Year counter	Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1
7	0	1	1	1	Time trimming register	$\overline{XSL}$	F_6	F_5	F_4	F_3	F_2	F_1	F_0
8	1	0	0	0	Alarm_A (minute register)	—	AM_{40}	AM_{20}	AM_{10}	AM_8	AM_4	AM_2	AM_1
9	1	0	0	1	Alarm_A (hour register)	—	—	AH_{20} $AP/\overline{A}$	AH_{10}	AH_8	AH_4	AH_2	AH_1
A	1	0	1	0	Alarm_A (day of the week register)	—	AW_6	AW_5	AW_4	AW_3	AW_2	AW_1	AW_0
B	1	0	1	1	Alarm_B (minute register)	—	BM_{40}	BM_{20}	BM_{10}	BM_8	BM_4	BM_2	BM_1
C	1	1	0	0	Alarm_B (hour register)	—	—	BH_{20} $BP/\overline{A}$	BH_{10}	BH_8	BH_4	BH_2	BH_1
D	1	1	0	1	Alarm_B (day of the week register)	—	BW_6	BW_5	BW_4	BW_3	BW_2	BW_1	BW_0
E	1	1	1	0	Control register 1	AALE	BALE	SL_2	SL_1	TEST	CT_2	CT_1	CT_0
F	1	1	1	1	Control register 2	—	—	$\overline{12}/24$	ADJ*3 XSTP*4	$\overline{CLEN}$	CTFG	AAFG	BAFG

*1) All the listed data can be read and written except for ADJ/XSTP.
*2) The "–" mark indicates data which can be read only and set to "0" when read.
*3) The ADJ/XSTP bit of the control register2 is set to ADJ for write and XSTP for read operation. The XSTP bit is set to "0" by writing data into the control register2 for normal oscillation.
*4) When XSTP is set to "1", the $\overline{XSL}$, F_6 to F_0, CT_2 to CT_0, AALE, BALE, SL_2, SL_1, $\overline{CLEN}$ and TEST bits are reset to "0".

2. Registers

2.1 Control Register 1 (at internal address Eh)

D7	D6	D5	D4	D3	D2	D1	D0	
AALE	BALE	SL_2	SL_1	TEST	CT_2	CT_1	CT_0	(For write operation)
AALE	BALE	SL_2	SL_1	TEST	CT_2	CT_1	CT_0	(For read operation)
0	0	0	0	0	0	0	0	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.1-1 AALE, BALE

Alarm_A, Alarm_B enable bits

AALE, BALE	Description	
0	Alarm_A (Alarm_B) Correspondence action invalid	(Default)
1	Alarm_A (Alarm_B) Correspondence action valid	

2.1-2 SL2, SL1

Interrupt output select bits

SL2	SL1	Description	
0	0	Outputs Alarm_A, Alarm_B, INT to the $\overline{\text{INTRA}}$. Outputs 32k clock pulses to the $\overline{\text{INTRB}}$.	(Default)
0	1	Outputs Alarm_A, INT to the $\overline{\text{INTRA}}$. Outputs 32k clock pulses, Alarm_B to the $\overline{\text{INTRB}}$.	
1	0	Outputs Alarm_A, Alarm_B to the $\overline{\text{INTRA}}$. Outputs 32k clock pulses, INT to the $\overline{\text{INTRB}}$.	
1	1	Outputs Alarm_A to the $\overline{\text{INTRA}}$. Outputs 32k clock pulses, Alarm_B, INT to the $\overline{\text{INTRB}}$.	

By setting SL1 and SL2 bits, two alarm pulses (Alarm_A and alarm_B), periodic interrupt output (INT), 32k clock pulses may be output to the $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ pins selectively.

2.1-3 TEST

Test bit

TEST	Description	
0	Ordinary operation mode	(Default)
1	Test mode	

The test bit is used for IC test. Set the TEST bit to 0 in ordinary operation.

2.1-4 CT2, CT1, CT0

Periodic interrupt cycle select bit

CT2	CT1	CT0	Description		
			Wave form mode	Cycle and falling timing	
0	0	0	—	off (“H”)	(Default)
0	0	1	—	Fixed at “L”	
0	1	0	Pulse mode	2Hz (Duty50%)	
0	1	1	Pulse mode	1Hz (Duty50%)	
1	0	0	Level mode	Every second (synchronized with second count up)	
1	0	1	Level mode	Every minute (00 second of every minute)	
1	1	0	Level mode	Every hour (00 minute(s) 00 second(s) of every hour)	
1	1	1	Level mode	Every month (the 1st day 00 A.M. 00 minute(s) 00 second(s) of every month)	

1) Pulse mode : Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds see the diagram below.

*) When 32.000kHz crystal is used,
In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternately.
Duty cycle for 1Hz clock pulses becomes 50.4% (“L” duration is 0.496s while “H” duration is 0.504s).

2) Level mode : One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output.

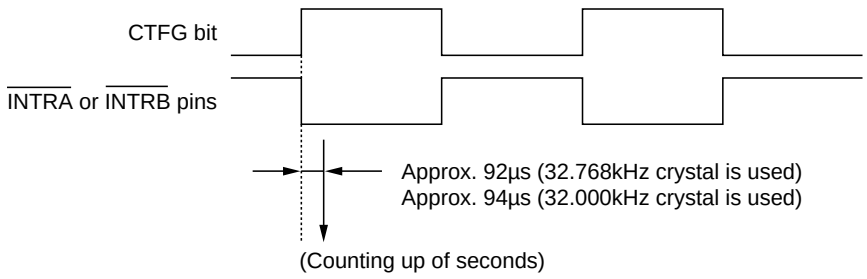
3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.

Pulse mode : “L” duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)
For example, Duty will be 50±0.3784% (or 50±0.3875% when 32.000kHz crystal is used) at 1Hz.

Level mode : Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)

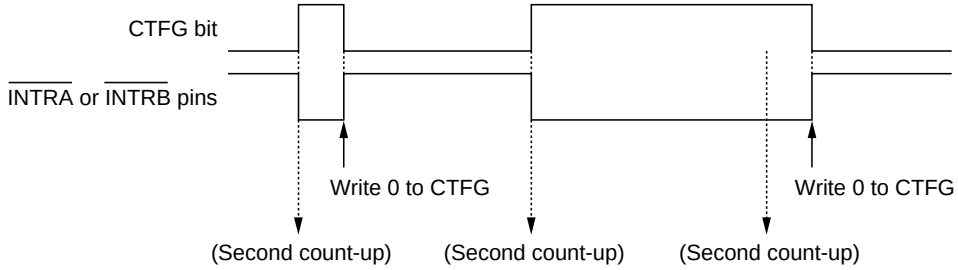
Relation Between Mode Waveforms and CTFG Bit

• Pulse mode



*) Since counting up of seconds and the falling edge has a time lag of approx. 92µs (at 32.768kHz) (approx. 94µs when 32.000kHz crystal is used), time with apparently approx. one second of delay from time of the real-time clock may be read when time is read in synchronization with the falling edge of output.

• Level mode



2.2 Control Register 2 (at internal address Fh)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	$\overline{12}$/24	ADJ	$\overline{CLEN}$	CTFG	AAFG	BAFG	(For write operation)
0	0	$\overline{12}$/24	XSTP	$\overline{CLEN}$	CTFG	AAFG	BAFG	(For read operation)
0	0	Undefined	1	0	0	0	0	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.2-1 $\overline{12}$/24

$\overline{12}$/24-hour Time Display System Selection bit

$\overline{12}$/24	Description
0	12-hour time display system (separate for mornings and afternoons)
1	24-hour time display system

Being set this bit at "0" indicates 12-hour display system while "1" indicates 24-hour system.

Time Display Digit Table

24-hour time display system	12-hour time display system	24-hour time display system	12-hour time display system
00	12 (AM12)	12	32 (PM12)
01	01 (AM 1)	13	21 (PM 1)
02	02 (AM 2)	14	22 (PM 2)
03	03 (AM 3)	15	23 (PM 3)
04	04 (AM 4)	16	24 (PM 4)
05	05 (AM 5)	17	25 (PM 5)
06	06 (AM 6)	18	26 (PM 6)
07	07 (AM 7)	19	27 (PM 7)
08	08 (AM 8)	20	28 (PM 8)
09	09 (AM 9)	21	29 (PM 9)
10	10 (AM10)	22	30 (PM10)
11	11 (AM11)	23	31 (PM11)

*) Either the 12-hour or 24-hour time display system should be selected before writing time data.

2.2-2 ADJ

±30 Second Adjust Bit

ADJ	Description
0	Ordinary operation
1	Second digit adjustment

· The following operations are performed by setting the second ADJ bit to 1.
  1) For second digits ranging from "00" to "29" seconds:
     Time counters smaller than seconds are reset and second digits are set to "00".
  2) For second digits ranging from "30" to "59" seconds:
     Time counters smaller than seconds are reset and second digits are set to "00". Minute digits are incremented by 1.
· Second digits are adjusted within 122µs (within 125µs: when 32.000kHz crystal is used) from writing operation to ADJ.
· The ADJ bit is for write only and allows no read operation.

2.2-3 XSTP

Oscillator Halt Sensing Bit

XSTP	Description	
0	Ordinary oscillation	
1	Oscillator halt sensing	(Default)

The XSTP bit senses the oscillator halt.
· When oscillation is halted after initial power on from 0V or drop in supply voltage the bit is set to "1" and which remains to be "1" after it is restarted. This bit may be used to judge validity of clock and calendar count data after power on or supply voltage drop.
· When this bit is set to "1", $\overline{XSL}$, F_6 to F_0, CT_2, CT_1, CT_0, AALE, BALE, SL_2, SL_1, $\overline{CLEN}$ and TEST bits are reset to "0". $\overline{INTRA}$ will stop output and the $\overline{INTRB}$ will output 32kHz clock pulses.
· The XSTP bit is set to "0" by setting the control register 2 (address Fh) during ordinary oscillation.

2.2-4 $\overline{CLEN}$

32kHz Clock Output Bit

$\overline{CLEN}$	Description	
0	32kHz clock output enabled	(Default)
1	32kHz clock output disabled	

By setting this bit to "0", output of clock pulses of the same frequency as the crystal oscillator is enabled.

2.2-5 CTFG

Periodic Interrupt Flag Bit

CTFG	Description	
0	Periodic interrupt output=OFF (“H”)	(Default)
1	Periodic interrupt output=ON (“L”)	

This bit is set to “1” when periodic interrupt pulses are output ($\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$=“L”).
The CTFG bit may be set only to “0” in the interrupt level mode. Setting this bit to “0” sets either the $\overline{\text{INTRA}}$ or the $\overline{\text{INTRB}}$ to OFF (“H”). When this bit is set to “1” nothing happens.

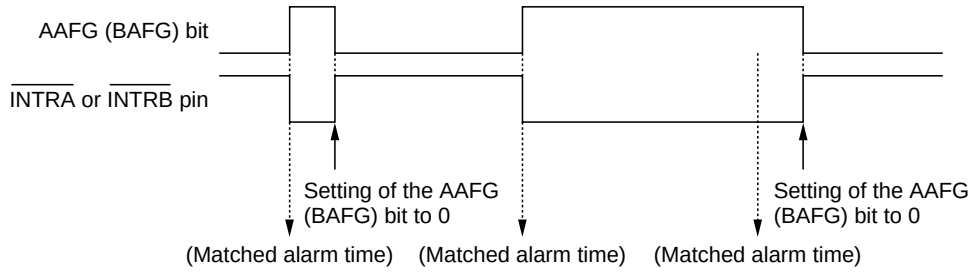
2.2-6 AAFG, BAFG

Alarm_A (Alarm_B) Flag Bit

AAFG, BAFG	Description	
0	Unmatched alarm register with clock counter	(Default)
1	Matched alarm register with clock counter	

- The alarm interruption is enabled only when the AALE, BALE bits are set to “1”. This bit turns to “1” when matched time is sensed for each alarm.
- The AAFG, BAFG bit may be set only to “0”. Setting this bit to “0” sets either the $\overline{\text{INTRA}}$ or the $\overline{\text{INTRB}}$ to the “H”. When this bit is set to “1” nothing happens.
- When the AALE, BALE bit is set to “0”, alarm operation is disabled and “0” is read from the AAFG, BAFG bit.

Output Relationships Between the ALFG Bit and $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$



2.3 Clock Counter (at internal address 0-2h)

· Time digit display (in BCD code)

Second digits : Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.

Minute digits : Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.

Hour digits : See descriptions on the $\overline{12}/24$ bit (Section 2.2-1).

Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

· Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

2.3-1 Second digit register (at internal address 0h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For write operation)
0	S_{40}	S_{20}	S_{10}	S_8	S_4	S_2	S_1	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.3-2 Minute digit register (at internal address 1h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For write operation)
0	M_{40}	M_{20}	M_{10}	M_8	M_4	M_2	M_1	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.3-3 Hour digit register (at internal address 2h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	$P/\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For write operation)
0	0	$P/\overline{A}$ or H_{20}	H_{10}	H_8	H_4	H_2	H_1	(For read operation)
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.4 Day-of-the-week Counter (at internal address 3h)

- Day-of-the-week digits are incremented by 1 when carried to 1-day digits.
- Day-of-the-week digits display (incremented in septimal notation):
  $(W_4, W_2, W_1)=(0,0,0)\rightarrow(0,0,1)\rightarrow\cdots\rightarrow(1,1,0)\rightarrow(0,0,0)$
- The relation between days of the week and day-of-the-week digits is user changeable (e.g. Sunday=0,0,0).
- The (W_4, W_2, W_1) should not be set to (1, 1, 1).

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	—	—	—	W_4	W_2	W_1	(For write operation)
0	0	0	0	0	W_4	W_2	W_1	(For read operation)
0	0	0	0	0	Undefined	Undefined	Undefined	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.5 Calendar Counter (at internal address 4 to 6h)

- The automatic calendar function provides the following calendar digit displays in BCD code.

  Day digits : Range from 1 to 31 (for January, March, May, July, August, October, and December).
  Range from 1 to 30 (for April, June, September, and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.

  Month digits : Range from 1 to 12 and carried to year digits when cycled to 1.

  Year digits : Range from 00 to 99 and 00, 04, 08,..., 92, and 96 are counted as leap years.

- Any registered imaginary time should be replaced with correct time as carrying to such registered imaginary time digits from lower-order ones cause the clock counter malfunction.

2.5-1 Day digit register (at internal address 4h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For write operation)
0	0	D_{20}	D_{10}	D_8	D_4	D_2	D_1	(For read operation)
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.5-2 Month digit register (at internal address 5h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	—	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For write operation)
0	0	0	MO_{10}	MO_8	MO_4	MO_2	MO_1	(For read operation)
0	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.5-3 Year digit register (at internal address 6h)

D7	D6	D5	D4	D3	D2	D1	D0	
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For write operation)
Y_{80}	Y_{40}	Y_{20}	Y_{10}	Y_8	Y_4	Y_2	Y_1	(For read operation)
Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.6 Time Trimming Register (at internal address 7h)

D7	D6	D5	D4	D3	D2	D1	D0	
$\overline{XSL}$	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For write operation)
$\overline{XSL}$	F_6	F_5	F_4	F_3	F_2	F_1	F_0	(For read operation)
0	0	0	0	0	0	0	0	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

2.6-1 $\overline{XSL}$ bit

The $\overline{XSL}$ bit is used to select a crystal oscillator.

Set the $\overline{XSL}$ to "0" (default) to use 32.768kHz.

Set the $\overline{XSL}$ to "1" to use 32.000kHz.

2.6-2 F_6 to F_0

The time trimming circuit adjust one second count based on this register readings when second digit is 00, 20, or 40 seconds. Normally, counting up to seconds is made once per 32,768 of clock pulse (or 32,000 when 32.000kHz crystal is used) generated by the oscillator. Setting data to this register activates the time trimming circuit.

Register counts will be incremented as $((F_5, F_4, F_3, F_2, F_1, F_0)-1)\times 2$ when F_6 is set to "0".
Register counts will be decremented as $((\overline{F_5}, \overline{F_4}, \overline{F_3}, \overline{F_2}, \overline{F_1}, \overline{F_0})+1)\times 2$ when F_6 is set to "1".
Counts will not change when $(F_6, F_5, F_4, F_3, F_2, F_1, F_0)$ are set to $(*, 0, 0, 0, 0, 0, *)$.

For example, when 32.768kHz crystal is used.

When $(F_6, F_5, F_4, F_3, F_2, F_1, F_0)$ are set to (0, 0, 0, 0, 1, 1, 1), counts will change as: $32{,}768+(7-1)\times 2=32{,}780$ (clock will be delayed) when second digit is 00, 20, or 40.

When $(F_6, F_5, F_4, F_3, F_2, F_1, F_0)$ are set to (0, 0, 0, 0, 0, 0, 1), counts will remain 32,768 without changing when second digit is 00, 20, or 40.

When $(F_6, F_5, F_4, F_3, F_2, F_1, F_0)$ are set to (1, 1, 1, 1, 1, 1, 0), counts will change as: $32{,}768+(-2)\times 2=32{,}764$ (clock will be advanced) when second digit is 00, 20, or 40.

Adding 2 clock pulses every 20 seconds: $2/(32{,}768\times 20)=3.051$ppm (or 3.125ppm when 32.000kHz crystal is used), delays the clock by approx. 3ppm. Likewise, decrementing 2 clock pulses advances the clock by 3ppm. Thus the clock may be adjusted to the precision of ±1.5ppm. Note that the time trimming function only adjust clock timing and oscillation frequency and 32kHz clock output is not adjusted.

2.7 Alarm_A, Alarm_B Register (Alarm_A: internal address 8 to Ah; Alarm_B: internal address B to Dh)

2.7-1 Alarm_A minute register (internal address 8h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	AM_{40}	AM_{20}	AM_{10}	AM_{8}	AM_{4}	AM_{2}	AM_{1}	(For write operation)
0	AM_{40}	AM_{20}	AM_{10}	AM_{8}	AM_{4}	AM_{2}	AM_{1}	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.7-2 Alarm_B minute register (internal address Bh)

D7	D6	D5	D4	D3	D2	D1	D0	
—	BM_{40}	BM_{20}	BM_{10}	BM_{8}	BM_{4}	BM_{2}	BM_{1}	(For write operation)
0	BM_{40}	BM_{20}	BM_{10}	BM_{8}	BM_{4}	BM_{2}	BM_{1}	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.7-3 Alarm_A hour register (internal address 9h)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	AH_{20}, AP/$\overline{A}$	AH_{10}	AH_{8}	AH_{4}	AH_{2}	AH_{1}	(For write operation)
0	0	AH_{20}, AP/$\overline{A}$	AH_{10}	AH_{8}	AH_{4}	AH_{2}	AH_{1}	(For read operation)
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.7-4 Alarm_B hour register (internal address Ch)

D7	D6	D5	D4	D3	D2	D1	D0	
—	—	BH_{20}, AP/$\overline{A}$	BH_{10}	BH_{8}	BH_{4}	BH_{2}	BH_{1}	(For write operation)
0	0	BH_{20}, AP/$\overline{A}$	BH_{10}	BH_{8}	BH_{4}	BH_{2}	BH_{1}	(For read operation)
0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.7-5 Alarm_A day-of-the-week register (internal address Ah)

D7	D6	D5	D4	D3	D2	D1	D0	
—	AW_{6}	AW_{5}	AW_{4}	AW_{3}	AW_{2}	AW_{1}	AW_{0}	(For write operation)
0	AW_{6}	AW_{5}	AW_{4}	AW_{3}	AW_{2}	AW_{1}	AW_{0}	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

2.7-6 Alarm_B day-of-the-week register (internal address Dh)

D7	D6	D5	D4	D3	D2	D1	D0	
—	BW_6	BW_5	BW_4	BW_3	BW_2	BW_1	BW_0	(For write operation)
0	BW_6	BW_5	BW_4	BW_3	BW_2	BW_1	BW_0	(For read operation)
0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Default*

*) The default means read value when XSTP bit is set to "1" by starting up from 0V, or supply voltage drop, etc.

- Alarm_A, Alarm_B hour register D5 is set to 0 for AM and 1 for PM in the 12-hour display system at AP/$\overline{A}$. The register D5 indicates 10 digit of hour digit in 24-hour display system at AH_{20}.
- To activate alarm operation, any imaginary alarm time setting should not be left to avoid unmatching.
- In hour digit display midnight is set to 12, noon is set to 32 in 12-hour display system. (See section 2.2-1)
- AW_0 to AW_6 correspond to the day-of-the-week counter (W_4, W_2, W_1) being set at (0, 0, 0) to (1, 1, 0).
- No alarm pulses are output when all of AW_0 to AW_6 are set to "0".

Example of Alarm Time Settings

Alarm Time Settings	Day-of-the-week							12-hour system				24-hour system			
	Sun. AW_0	Mon. AW_1	Tue. AW_2	Wed. AW_3	Thu. AW_4	Fri. AW_5	Sat. AW_6	10-hour	1-hour	10-min	1-min	10-hour	1-hour	10-min	1-min
00:00 AM every day	1	1	1	1	1	1	1	1	2	0	0	0	0	0	0
01:30 AM every day	1	1	1	1	1	1	1	0	1	3	0	0	1	3	0
11:59 AM every day	1	1	1	1	1	1	1	1	1	5	9	1	1	5	9
00:00 PM on Monday through Friday	0	1	1	1	1	1	0	3	2	0	0	1	2	0	0
01:30 PM on Sunday	1	0	0	0	0	0	0	2	1	3	0	1	3	3	0
11:59 PM on Monday, Wednesday, and Friday	0	1	0	1	0	1	0	3	1	5	9	2	3	5	9

Designation of days of the week and AW_0 to AW_6 in the above table is an example.

OPERATION

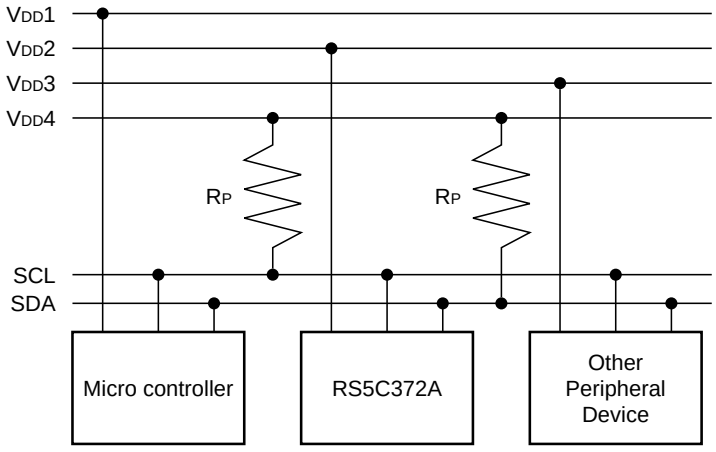
1. Interfacing with the CPU

The RS5C372A employs the I²CBus system to be connected to the CPU via 2-wires. Connection and transfer system of I²CBus are described in the following sections.

Note
I²CBus is a trademark of PHILIPS ELECTRONICS N.V.

1.1 Connection of I²CBus

2-wires, SCL and SDA which are connected to I²CBus are used for transmit clock pulses and data respectively.
All ICs that are connected to these lines are designed that will be not be clamped when a voltage beyond supply voltage is applied to input or output pins. Open drain pins are used for output. This construction allows communication of signals between ICs with different supply voltages by adding a pull-up resistor to each signal line as shown in the figure below. Each IC is designed not to affect SCL and SDA signal lines when power to each of these is turned off separately.



*) For data interface, the following conditions must be met:
$V_{DD4} \geq V_{DD1}$
$V_{DD4} \geq V_{DD2}$
$V_{DD4} \geq V_{DD3}$

*) When the master is one, the micro controller is ready for driving SCL to "H" and R_P of SCL may not be required.

Cautions on Determining R_P Resistance

(1) Voltage drop at R_P due to sum of input current or output current at off conditions on each IC pin connected to the I²CBus shall be adequately small.
(2) Rising time of each signal shall be kept short even when all capacity of the bus is driven.
(3) Current consumed in I²CBus is small compared to the consumption current permitted for the entire system.

When all ICs connected to I²CBus are CMOS type, condition (1) may usually be ignored since input current and off state output current is extremely small for the many CMOS type ICs.
Thus the maximum resistance of R_P may be determined based on (2) while the minimum on (3) in most cases.

In actual cases a resistor may be place between the bus and input/output pins of each IC to improve noise margins in which case the R_P minimum value may be determined by the resistance.

Consumption current in the bus to review (3) above may be expressed by the formula below:

$$\text{Bus consumption current} \fallingdotseq \frac{(\text{Sum of input current and off state output current of all devices in stand-by mode}) \times \text{Bus stand-by duration}}{\text{Bus stand-by duration} + \text{bus operation duration}} + \frac{\text{Supply voltage} \times \text{bus operation duration} \times 2}{R_P \text{ resistance} \times 2 \times (\text{bus stand-by duration} + \text{bus operation duration})} + \text{supply voltage} \times \text{bus capacity} \times \text{charging/discharging times per unit time}$$

Operation of "× 2" in the second member denominator in the above formula is derived from assumption that "L" duration of SDA and SCL pins are the half of bus operation duration. "× 2" in the numerator of the same member is because there are two pins of SDA and SCL. The third member, (charging/discharging times per unit time) means number of transition from "H" to "L" of the signal line.

Calculation example is shown below:

Pull-up resistor (R_P)=10kΩ, Bus capacity=50pF (both for SCL and SDA), V_{DD}=3V
In as system with sum of input current and off state output current of each pin=0.1μA, I²CBus is used for 10ms every second while the rest of 990ms is in the stand-by mode. In this mode number of transitions of the SCL pin from "H" to "L" state is 100 while SDA 50, every second.

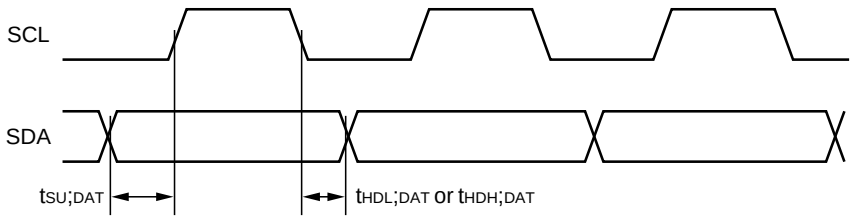
$$\text{Bus consumption current} \fallingdotseq \frac{0.1\mu A \times 990ms}{990ms + 10ms} + \frac{3V \times 10ms \times 2}{10k\Omega \times 2 \times (990ms + 10ms)} + 3V \times 50pF \times (100 + 50) = 0.099\mu A + 3.0\mu A + 0.0225\mu A = 3.12\mu A$$

Generally, the second member of the above formula is larger enough than the first and the third members, bus consumption current may be determined by the second member in many cases.

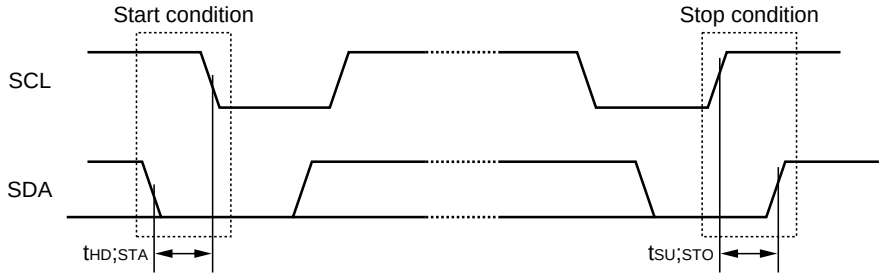
1.2 Transmission System of I²CBus

1.2-1 Start and stop conditions

In I²CBus, SDA must be kept at a certain state while SCL is at the "H" state as shown below during data transmission.



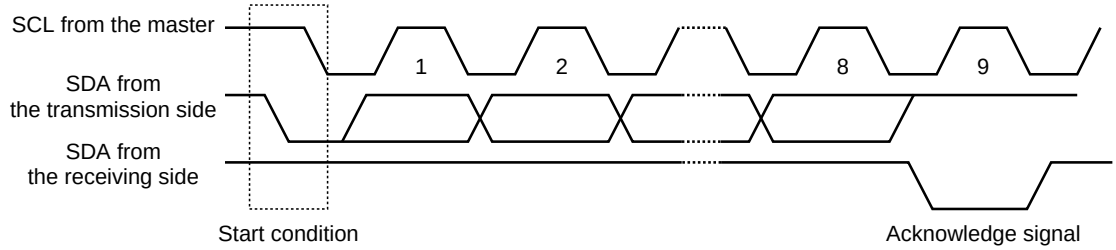
The SCL and SDA pins are at the "H" level when no data transmission is made. Changing the SDA from "H" to "L" when the SCL and the SDA are "H" activates the start condition and access is started. Changing the SDA from "L" to "H" when the SCL is "H" activates stop condition and accessing stopped. Generation of start and stop conditions are always made by the master (see the figure below).



1.2-2 Data transmission and its acknowledge

After start condition is entered, data is transmitted by 1byte (8bits). Any bytes of data may be serially transmitted. The receiving side will send an acknowledge signal to the transmission side each time 8bit data is transmitted.

The acknowledge signal is sent immediately after falling to "L" of SCL8bit clock pulses of data transmission, by releasing the SDA by the transmission side that has asserted the bus at that time and by turning the SDA to "L" by the receiving side. When transmission of 1byte data next to preceding 1byte of data is received the receiving side releases the SDA pin at falling edge of the SCL9bit of clock pulses or when the receiving side switches to the transmission side it starts data transmission. When the master is the receiving side, it generates no acknowledge signal after the last 1byte of data from the slave to tell the transmitter that data transmission has completed when the slave side (transmission side) continues to release the SDA pin so that the master will be able to generate stop condition.

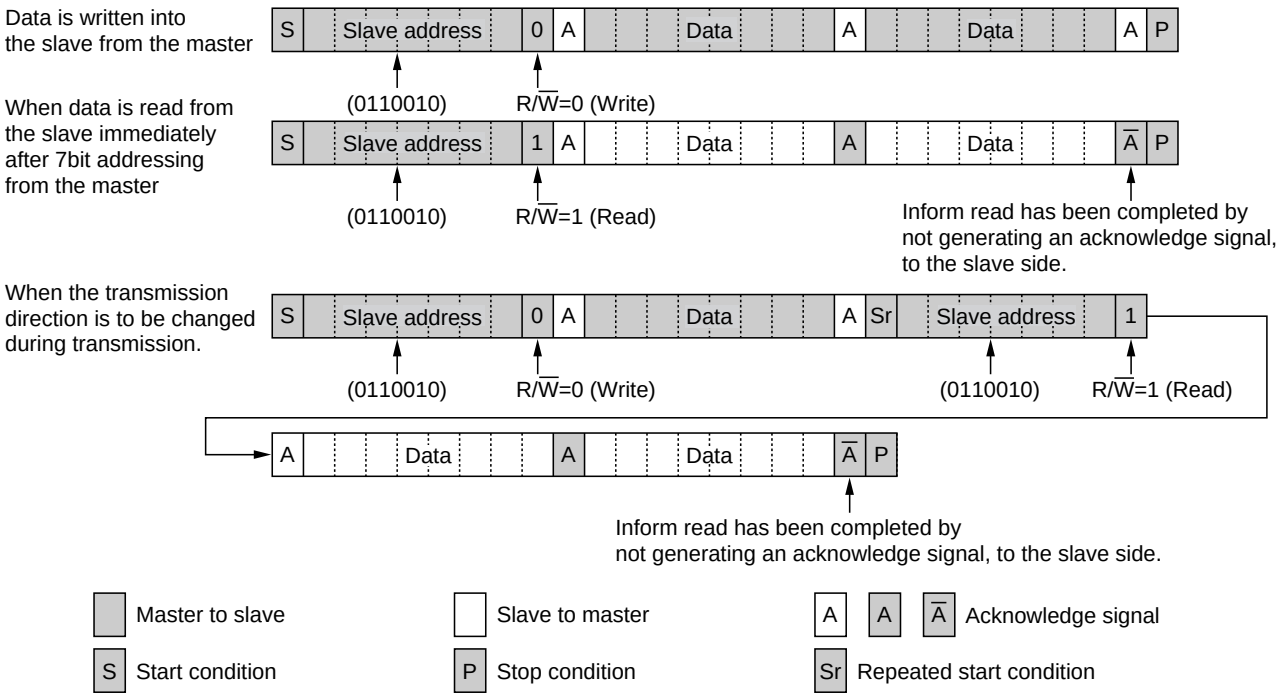


1.2-3 Data transmission format in I²CBus

I²CBus generates no CE signals. In place of it each device has a 7bit slave address allocated. The first 1byte is allocated to this 7bit of slave address and to the command (R/$\overline{W}$) for which data transmission direction is designated by the data transmission thereafter. 7bit address is sequentially transmitted from the MSB and 2 and after bytes are read, when 8bit is "H" and write when "L".

The slave address of the RS5C372A is specified at (0110010).

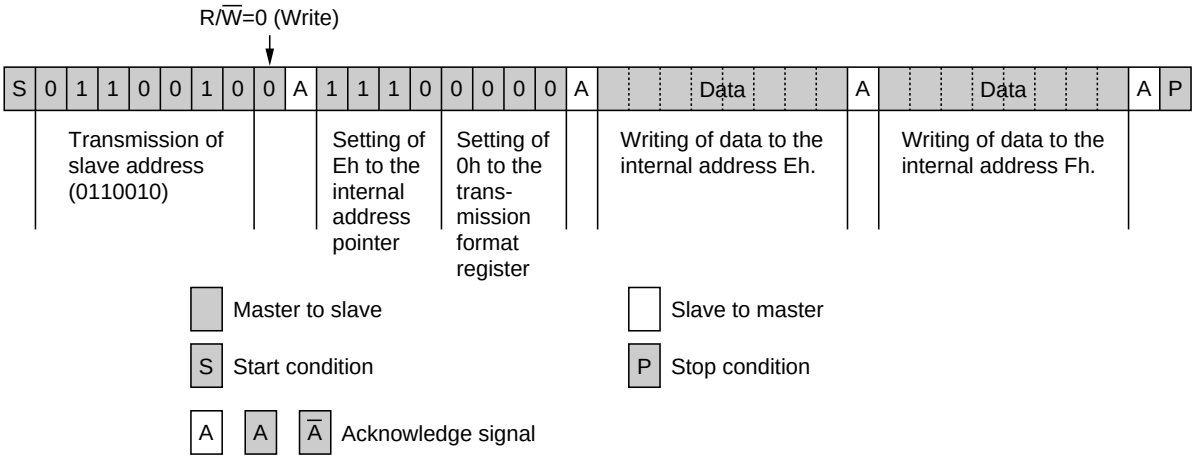
At the end of data transmission/receiving stop condition is generated to complete transmission. However, if start condition is generated without generating stop condition, repeated start condition is met and transmission/receiving data may be continued by setting the slave address again. Use this procedures when the transmission direction needs to be changed during one transmission.



1.2-4 Data transmission write format in the RS5C372A

Although the I²CBus standard defines a transmission format for the slave address allocated for each IC, transmission method of address information in IC is not defined. The RS5C372A transmits data the internal address pointer (4bit) and the transmission format register (4bit) at the 1byte next to one which transmitted a slave address and a write command. For write operation only one transmission format is available and (0000) is set to the transmission format register. The 3byte transmits data to the address specified by the internal address pointer written to the 2byte. Internal address pointer settings are automatically incremented for 4byte and after. Note that when the internal address pointer is Fh, it will change to 0h on transmitting the next byte.

Example of data writing (When writing to internal address Eh to Fh)

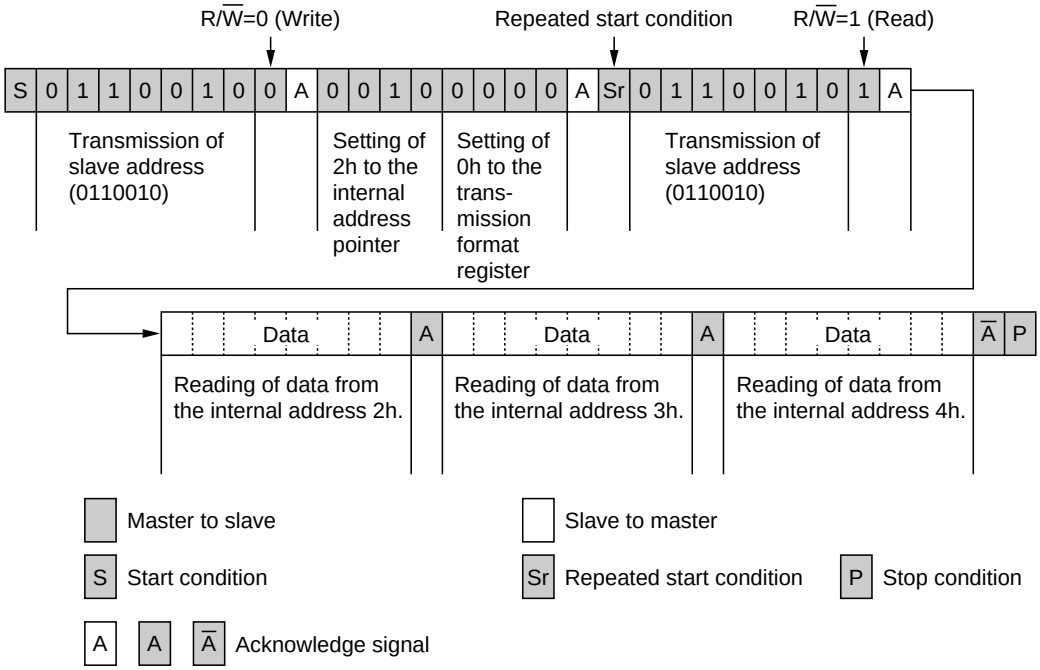


1.2-5 Data transmission read format of the RS5C372A

The RS5C372A allows the following three readout methods of data from an internal register.

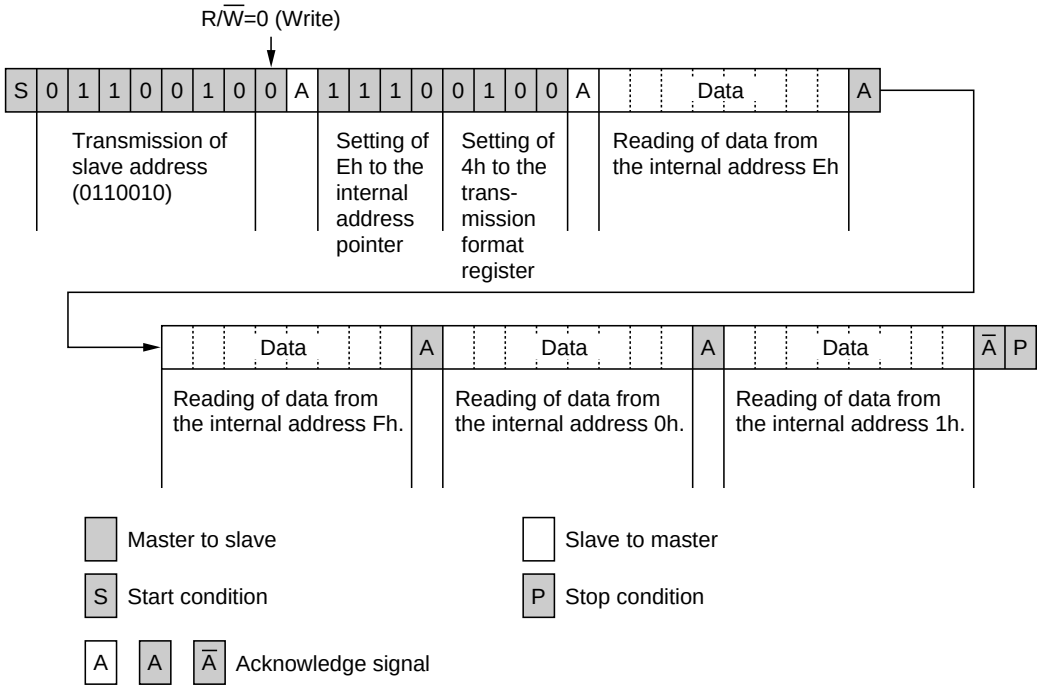
1) The first method to reading data from the internal register is to specify an internal address by setting the internal address pointer and the transmission format register described 1.2-4, generate the repeated start condition (see section 1.2-3) to change the data transmission direction to perform reading. The internal address pointer is set to Fh when the stop condition is met. Therefore, this method of reading allows no insertion of the stop condition before the repeated start condition. Set 0h to the transmission format register.

Example 1 of data read (when data is read from 2h to 4h)



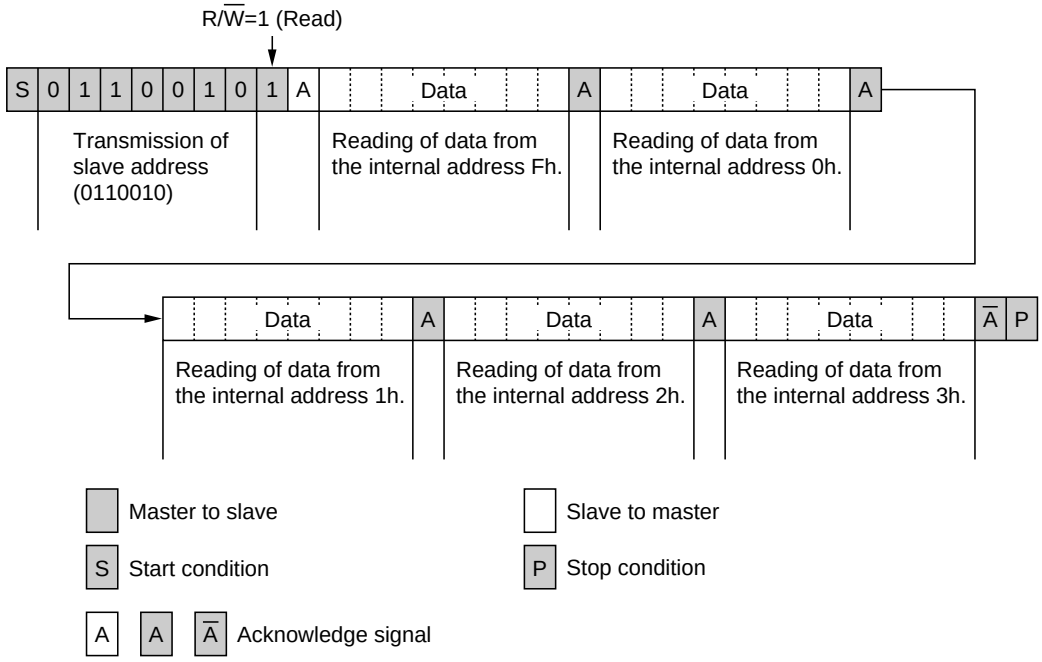
2) The second method to reading data from the internal register is to start reading immediately after writing to the internal address pointer and the transmission format register. Although this method is not based on the I²CBus standard in a strict sense it still effective to shorten read time to ease load to the master. Set 4h to the transmission format register when this method is used.

Example 2 of data read (when data is read from internal addresses Eh to 1h).



3) The third method to reading data from the internal register is to start reading immediately after writing to the slave address and the R/$\overline{W}$ bit. Since the internal address pointer is set to Fh by default as described in 1), this method is only effective when reading is started from the internal address Fh.

Example 3 of data read (when data is read from internal addresses Fh to 3h).



1.2-6 Data transmission under special condition

The RS5C372A holds the clock tentatively for duration from start condition to stop condition to avoid invalid read or write clock on carrying clock. When clock is carried during this period, which will be adjusted within approx. 61µs from stop condition. To prevent invalid read or write clock shall be made during one transmission operation (from start condition to stop condition). When 0.5 to 1.0 second elapses after start condition any access to the RS5C372A is automatically released to release tentative hold of the clock, set Fh to the address pointer, and access from the CPU is forced to be terminated (the same action as made stop condition is received: automatic resume function from the I²CBus interface). Therefore, one access must be completed within 0.5 seconds. The automatic resume function prevents delay in clock even if the SCL is stopped from sudden failure of the system during clock read operation.

Also a second start condition after the first condition and before the stop condition is regarded as the "repeated start condition." Therefore, when 0.5 to 1.0 seconds passed after the first start condition, access to the RS5C372A is automatically released.

If access is tried after automatic resume function is activated, no acknowledge signal will be output for writing while FFh will be output for reading.

Access to the Real-time Clock

1) No stop condition shall be generated until clock read/write is started and completed.
2) One cycle read/write operation shall be completed within 0.5 seconds.

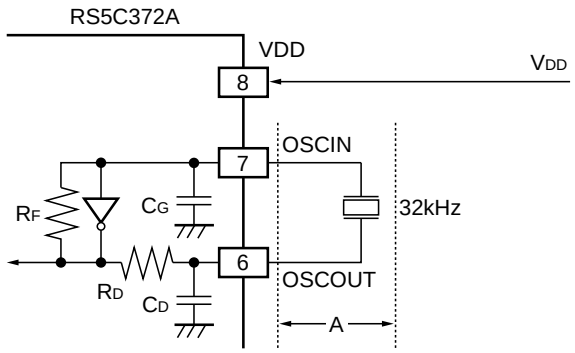
The user shall always be able to access the real-time clock as long as these two conditions are met.

Bad example of reading from seconds to hours (invalid read)
(Start condition) → (Read of seconds) → (Read of minutes) → (Stop condition) → (Start condition) → (Read of hour) → (Stop condition)

Assuming read was started at 05:59:59 P.M. and while reading seconds and minutes the time advanced to 06:00:00 P.M. At this time second digit is hold so the read as 05:59:59. Then the RS5C372A confirms (Stop condition) and carries second digit being hold and the time changes to 06:00:00 P.M. Then, when the hour digit is read, it changes to 6. The wrong results of 06:59:59 will be read.

2. Configuration of Oscillating Circuit and Time Trimming

2.1 Configuration of Oscillating Circuit



Typical external device:
X'tal: 32.768kHz or 32.000kHz
(R_I=30kΩ TYP.)
(C_L=6pF to 8pF)

Typical values of internal devices:
R_F=15MΩ TYP.
R_D=60kΩ TYP.
C_G, C_D=10pF TYP.

The oscillation circuit is driven at a constant voltage of about 1.2V relative to the Vss level.
Consequently, it generates a wave form having a peak-to-peak amplitude of about 1.2V on the positive side of the Vss level.

Considerations on Crystal Oscillator

Basic characteristics of a crystal oscillator includes R_I (equivalent series resistance: ease of oscillation) and C_L (load capacitance: rank of center frequency). R_I=TYP. of 30kΩ, C_L=6 to 8pF is recommended for the RS5C372A. Confirm recommended values to the manufacturer of the crystal oscillator used.

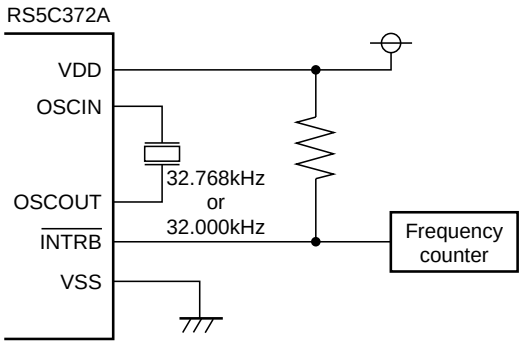
Considerations in Mounting Components Surrounding Oscillating Circuit

1) Mount the crystal oscillators in the closest possible position to the IC.
2) Avoid laying any signal or power line close to the oscillation circuit (particularly in the area marked with "← A →" in the above figure).
3) Apply the highest possible insulation resistance between the OSCIN or OSCOUT pin and the PCB.
4) Avoid using any long parallel line to wire the OSCIN and OSCOUT pin.
5) Take extreme care not to cause condensation, which leads to various problems such as oscillation halt.

Other Relevant Considerations

1) When applying an external input of clock pulses (32.768kHz or 32.000kHz) to the OSCIN pin:
   DC coupling : Prohibited due to mismatching of input levels.
   AC coupling : Permissible except that unpredictable results may occur in oscillator halt sensing due to possible sensing errors caused by noises, etc.
2) Avoid using the oscillator output of the RS5C372A (from the OSCOUT pin) to drive any other IC for the purpose of ensuring stable oscillation.

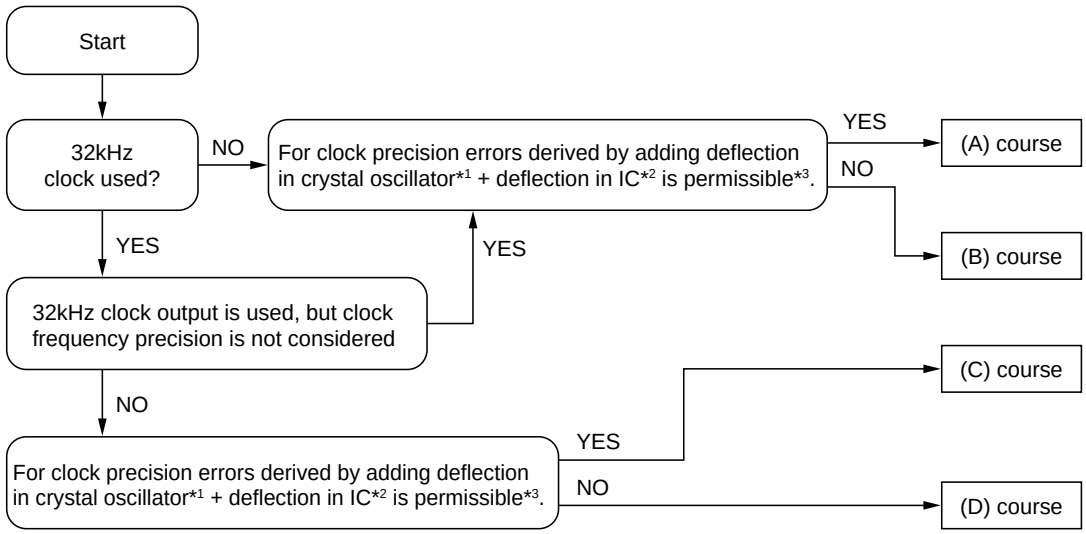
2.2 Measurement of Oscillation Frequency



∗1) Clock pulse of 32.768kHz or 32.000kHz is output from the $\overline{\text{INTRB}}$ output pin on powering on (XSTP is set to 1).
∗2) Use a frequency counter having at least 6 digits (7digits or more recommended).
∗3) Pull-up the $\overline{\text{INTRB}}$ output pin to V_{DD}.

2.3 Oscillation Frequency Adjustment

Adjustment amount of oscillation frequency may differ dependent on how the RS5C372A is used or how much clock error is permissible in the system it is installed. Use the flow chart shown below find an optimal oscillation frequency adjustment method.



∗1) In general crystal oscillators are classified by their central frequency of C_L (load capacitance) and available further grouped in several ranks as ±10, ±20 and ±50ppm of fluctuations in precision.
∗2) Fluctuations in frequency due to the IC used is generally from ±5 to 10ppm at a room temperature.
∗3) Clock precision here is at a room temperature and is subjected to change due to temperature characteristics of the crystal itself.

(A) course
Adjustment of clock is not made for IC (no adjustment) and any C_L value may be used for the crystal oscillator. Precision fluctuations of a crystal oscillator may be selected as long as clock precision allows. Obtain the central frequency as described in section 2.2 using several crystal oscillator and ICs, determine an adjustment value as described in "2.4 Time Trimming Circuit" which shall be set to the RS5C372A.

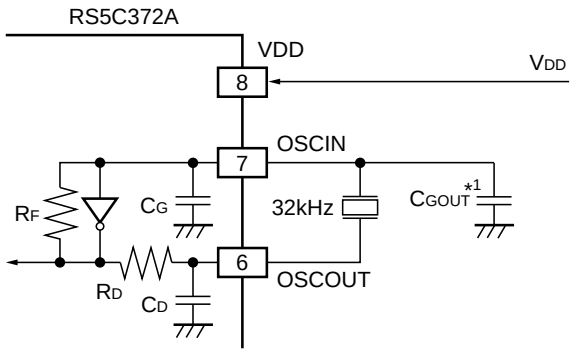
(B) course
To keep clock precision within the range of (fluctuation in crys-tal oscillator + fluctuation in IC), clock shall be adjustment is required for each IC. On adjusting procedures see "2.4 Time Trimming Circuit." Available selection range for the frequency precision fluctuations and C_L (load capacitance) for a crystal oscillator may be widened by adjusting clock frequency. Obtain the central frequency as described in section 2.2 using the crystal oscillator and IC to be used, determine if an adjustment is possible or not using the clock adjustment circuit, perform adjustment for each IC using the clock adjustment circuit. Up to ±1.5ppm may be adjusted at a room temperature.

(C) course
In (C) and (D) courses, adjustment of 32kHz clock output frequency as well as clock is necessary. Frequency adjustment for the crystal oscillator is made by adjusting both of C_G and C_D connected to the both ends of the oscillator. Since the RS5C372A incorporates the C_G and C_D, oscillating frequency is required using C_L of the crystal oscillator as the reference.

Generally, relation between C_L and C_G or C_D is as follows:

$$C_L = \frac{C_G \times C_D}{C_G + C_D} + C_S \qquad C_S : \text{Board floating capacitance}$$

Although a crystal oscillator having C_L value of around 6 to 8pF is recommended for the RS5C372A, measure oscillation frequency as described in section 2.2 and if frequency is high (clock gains) switch to a crystal oscillator with smaller C_L while if frequency is small (clock loses) switch to an oscillator with larger C_L. Using these procedures select a crystal oscillator with optimal C_L and set unadjusted value to the clock adjustment circuit. (See section 2.4, "Time Trimming Circuit".) We recommend to consult the crystal manufacturer on compatibility of C_L values.
High oscillation frequency (clock gains) may be adjusted by externally adding C_{GOUT} as shown below.



*1) C_{GOUT} shall be from 0 to 15pF.

(D) course
Select a crystal oscillator as in the (C) course, then adjust clock error for each IC as in (B) course. For clock adjusting procedures, see "2.4 Time Trimming Circuit."

2.4 Time Trimming Circuit

Using the time trimming circuit gain or lose of clock may be adjusted with high precision by changing clock pulses for one second every 20 seconds. When adjustment with this circuit is not necessary, set (F_6, F_5, F_4, F_3, F_2, F_1, F0) to (∗, 0, 0, 0, 0, 0,∗) to disable adjustment. (∗ mark indicates 0 or 1.)
Adjustment amount may be calculated using the following formula.

2.4-1 When oscillation frequency*1 >target frequency*2 (clock gains)

$$\text{Adjustment amount}^{*3} = \frac{(\text{Oscillation frequency} - \text{Target frequency} + 0.1)}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

When 32.000kHz crystal oscillator is used, the same formula,

$$\text{Adjustment amount} = \frac{(\text{Oscillation frequency} - \text{Target frequency} + 0.1)}{\text{Oscillation frequency} \times 3.125 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10 + 1$$

is used.

∗1) Oscillation frequency : Clock frequency output from the $\overline{\text{INTRB}}$ pin as in "2.2 Oscillation Frequency Measurement" at a room temperature.
∗2) Target frequency : A frequency to be adjusted to.
Since temperature characteristics of a 32.768kHz crystal oscillator are such that it will generally generates the highest frequency at a room temperature, we recommend to set the target frequency to approx. 32768.00Hz to 32768.10Hz (+3.05ppm to 32768Hz).
We also recommend setting of approx. 32000.00Hz to 32000.10Hz (3.125ppm to 32000Hz) also for the 32.000kHz crystal.
Note that this value may differ based on the environment or place where the device will be used.
∗3) Adjustment amount : A value to be set finally to F_6 to F_0 bits. This value is expressed in 7bit binary digits with sign bit (two's compliment).

2.4-2 When oscillation frequency=target frequency (no clock gain or loss)

Set the adjustment value to 0 or +1, or –64 or –63 to disable adjustment.

2.4-3 When oscillation frequency<target frequency (clock loses)

$$\text{Adjustment amount} = \frac{(\text{Oscillation frequency} - \text{Target frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10$$

Also a 32.000kHz crystal is used, the same formula,

$$\text{Adjustment amount} = \frac{(\text{Oscillation frequency} - \text{Target frequency})}{\text{Oscillation frequency} \times 3.051 \times 10^{-6}}$$

$$\fallingdotseq (\text{Oscillation frequency} - \text{Target frequency}) \times 10$$

is used.

Example of Calculations

(1) When oscillation frequency=32768.85kHz ; target frequency=32768.05kHz
Adjustment value= (32768.85–32768.05+0.1) / (32768.85×3.051×10^{-6}) ≒ (32768.85+32768.05)×10+1=9.001=9
Set (F_6, F_5, F_4, F_3, F_2, F_1, F_0) to (0, 0, 0, 1, 0, 0, 1).
As this example shows, adjustments to be used when the clock gains shall be distance from 01h.

(2) When actual oscillation frequency=32763.95kHz ; target frequency=32768.05kHz
Adjustment value= (32763.95–32768.05) / (32763.95×3.051×10^{-6}) ≒ (32763.95–32768.05)×10=–41.015≒–41
To express –41 in 7bit binary digits with sign bit (two's compliment),
Subtract 41(29h) from 128(80h) in the above case, 80h–29h=57h.
Thus, set (F_6, F_5, F_4, F_3, F_2, F_1, F_0) to (1, 0, 1, 0, 1, 1, 1).
As this example shows, adjustments to be used when the clock loses shall be distance from 80h.

After adjustment, adjustment error against the target frequency will be approx. ±1.5ppm at a room temperature.

Notes

1) Clock frequency output from the $\overline{\text{INTRB}}$ pin will not change after adjustment by the clock adjustment circuit.
2) Adjustable range: The range of adjustment values for a case oscillation frequency is higher than target frequency (clock gains) is (F_6, F_5, F_4, F_3, F_2, F_1, F_0)=(0, 0, 0, 0, 0, 1, 0) to (0, 1, 1, 1, 1, 1, 1) and actual adjustable amount shall be –3.05ppm to –189.2ppm (–3.125ppm to –193.7ppm for 32.000kHz crystal), thus clock error may be adjusted until clock gain reaches +189.2ppm (+193.7ppm for 32.000kHz crystal). On the other hand, the range of adjustment values for a case when oscillation frequency is lower than target frequency (clock loses) is (F_6, F_5, F_4, F_3, F_2, F_1, F_0)=(1, 1, 1, 1, 1, 1, 1) to (1, 0, 0, 0, 0, 1, 0) and actual adjustable amount shall be +3.05ppm to +189.2ppm (+3.125ppm to +193.8ppm for 32.000kHz crystal), thus clock error may be adjsted until clock loss reaches –189.2ppm (–193.8ppm for 32.000kHz crystal).

3. Oscillator Halt Sensing

Oscillation halt can be sensed through monitoring the XSTP bit with preceding setting of the XSTP bit to 0 by writing data to the control register 2. Upon oscillator halt sensing, the XSTP bit is switched from 0 to 1. This function can be applied to judge clock data validity. When the XSTP bit is 1, $\overline{XSL}$, F_6 to F_0, CT_2, CT_1, CT_0, AALE, BALE, SL_2, SL_1, $\overline{CLEN}$ and TEST bits are reset to 0.

⋆1) The XSTP bit is set to 1 upon power-on from 0V.
Note that any instantaneous power disconnection may cause operation failure.
⋆2) Once oscillation halt has been sensed, the XSTP bit is held at 1 even if oscillation is restarted.

Considerations in Use of XSTP Bit

Ensure error-free oscillation halt sensing by preventing the following events:

1) Instantaneous disconnection of V_{DD}
2) Condensation on the crystal oscillator
3) Generation of noise on the PCB in the crystal oscillator
4) Application of voltage exceeding prescribed maximum ratings to the individual pins of the IC.

4. $\overline{INTRA}$ Output and $\overline{INTRB}$ Output Pins

The following three output wave forms can be output from the $\overline{INTRA}$ or the $\overline{INTRB}$ pin.

1) Alarm interrupt
When a registered time for alarm (such as day-of-the-week, hour or minute) coincide with calendar counter (such as day-of-the-week, hour or minute) interrupt to the CPU are requested with the output pin being on ("L"). Alarm interrupt consists of Alarm_A and Alarm_B, both have equivalent functions.

2) Periodic interrupt
Outputs an output wave form selected by setting the periodic interrupt frequency select bit. Wave forms include pulse mode and level mode.

3) 32kHz clock output
Clock pulses generated in the oscillation circuit are output as they are.

4.1 Control of the $\overline{INTRA}$, $\overline{INTRB}$ Output (flag bit, enable bit, interrupt output select bit)

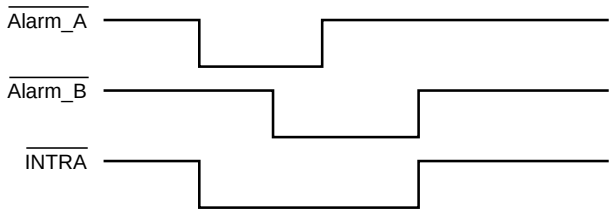
Of the three output wave forms listed above, interrupt output conditions may be set by setting the flag bit that monitors output state on the register, the enable bit that enables an output wave form and the output select bit that selects either $\overline{INTRA}$ or $\overline{INTRB}$ to be output a wave form to.

	Flag bit	Enable bit	Interrupt output select bit (SL2, SL1) (D5, D4 at Eh)			
			(0,0)	(0,1)	(1,0)	(1,1)
Alarm_A	AAFG (D1 at Fh)	AALE (D7 at Eh)	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRA}$
Alarm_B	BAFG (D0 at Fh)	BALE (D6 at Eh)	$\overline{INTRA}$	$\overline{INTRB}$	$\overline{INTRA}$	$\overline{INTRB}$
Periodic interrupt	CTFG (D2 at Fh)	Disabled at CT_2=CT_1=CT_0=0 (D2 to D0 at Eh)	$\overline{INTRA}$	$\overline{INTRA}$	$\overline{INTRB}$	$\overline{INTRB}$
32kHz clock output	No	$\overline{CLEN}$ (D3 at Fh)	$\overline{INTRB}$	$\overline{INTRB}$	$\overline{INTRB}$	$\overline{INTRB}$

· When power ON (XSTP=1) since AALE=BALE=CT_2=CT_1=CT_0=$\overline{CLEN}$=SL_2=SL_1=0,
$\overline{INTRA}$=OFF (H).
32kHz clock pulses are output from the $\overline{INTRB}$ pin.

· When more than one output wave forms are output from a single output pin, the output will have OR wave form of negative logic of both.

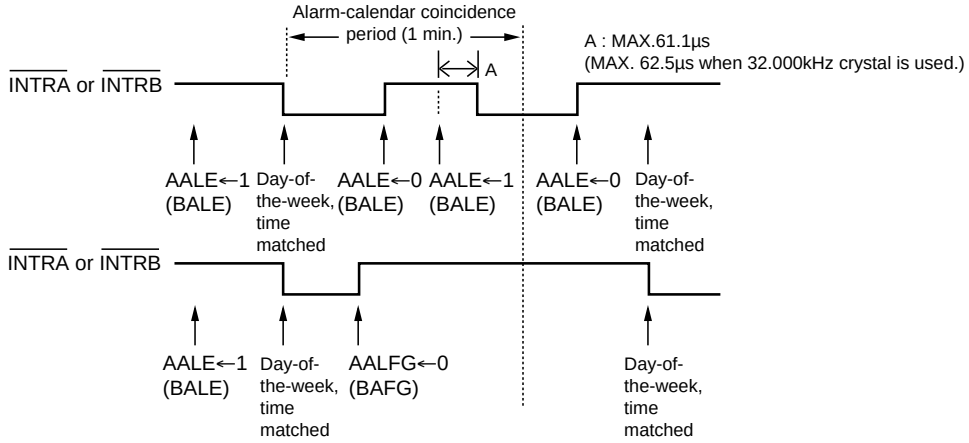
Example: When $\overline{Alarm\_A}$ and $\overline{Alarm\_B}$ are output from the $\overline{INTRA}$ pin.



In such a case which output wave form is output from the pin may be confirmed by reading the flag register.

4.2 Alarm Interrupt

For setting an alarm time, designated time such as day-of-the-week, hour or minute should be set to the alarm registers being AALE (BALE) bit to 0. After that set the AALE (BALE) bit to 1, from this moment onward when such registered alarm time coincide the value of calendar counter the $\overline{INTRA}$ or $\overline{INTRB}$ comes down to "L" (ON). The $\overline{INTRA}$ or $\overline{INTRB}$ output can be controlled by operating to the AALE (BALE) and AAFG (BAFG) bits.



*) Note that AAFG (BAFG) has an output wave form of reversed logic.

4.3 Periodic (Clock) Interrupt

The $\overline{\text{INTRA}}$ or $\overline{\text{INTRB}}$ pin output, the periodic interrupt cycle select bits (CT_2, CT_1, CT_0) and the interrupt output select bits (SL2, SL1) can be used to interrupt the CPU in a certain cycle. The periodic interrupt cycle select bits can be used to select either one of two interrupt output modes: the pulse mode and the level mode.

Interrupt Cycle Selection

CT_2	CT_1	CT_0	Description	
			Wave from mode	Cycle and falling timing
0	0	0	—	OFF (Default)
0	0	1	—	Fixed at "L"
0	1	0	Pulse	2Hz (Duty50%)
0	1	1	Pulse	1Hz (Duty50%)
1	0	0	Level	Every second (coincident with second count-up)
1	0	1	Level	Every minute (at 00 second)
1	1	0	Level	Every hour (at 00:00 on the hour)
1	1	1	Level	Every month (1st day, 00:00:00 a.m.)

1) Pulse mode : Outputs 2Hz, 1Hz clock pulses. For relationships with counting up of seconds see the diagram below.

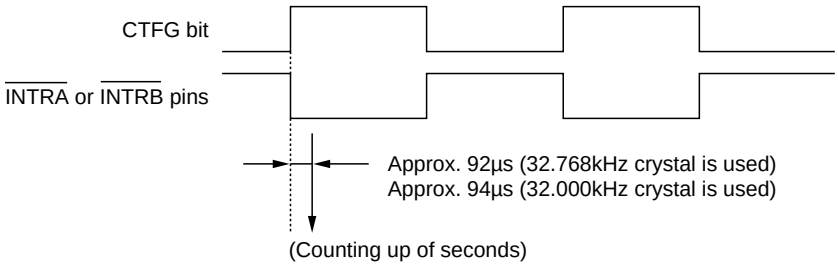
*) When 32.000kHz crystal is used,
In the 2Hz clock pulse mode, 0.496s clock pulses and 0.504s clock pulse are output alternately.
Duty cycle for 1Hz clock pulses becomes 50.4% ("L" duration is 0.496s while "H" duration is 0.504s).

2) Level mode : One second, one minute or one month may be selected for an interrupt cycle. Counting up of seconds is matched with falling edge of interrupt output.

3) When the time trimming circuit is used, periodic interrupt cycle changes every 20 seconds.
Pulse mode : "L" duration of output pulses may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)
For example, Duty will be 50±0.3784% (or 50±0.3875% when 32.000kHz crystal is used) at 1Hz.
Level mode : Frequency in one second may change in the maximum range of ±3.784ms (±3.875ms when 32.000kHz crystal is used.)

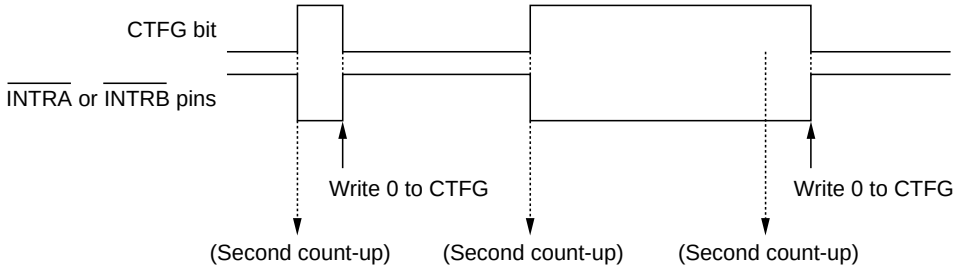
Relation Between Mode Waveforms and CTFG Bit

• Pulse mode



*) Since counting up of seconds and the falling edge has a time lag of approx. 92µs (at 32.768kHz) (approx. 94µs when 32.000kHz crystal is used), a time may be read with apparently approx. one second delayed from time of the real-time clock when time is read in synchronization with the falling edge of output.

• **Level mode**



4.4 32kHz Clock Output

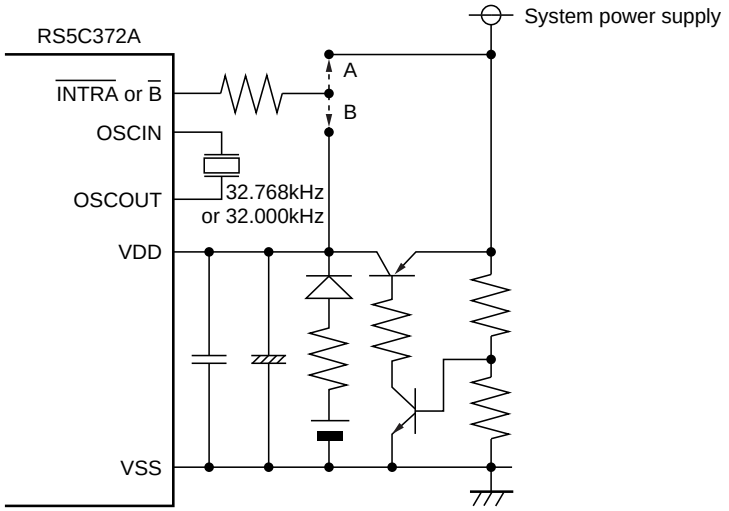
The crystal oscillator can generate clock pulses of 32kHz from the $\overline{\text{INTRB}}$ pin. The pin is changed to "H" by setting the $\overline{\text{CLEN}}$ bit to 1.

*) 32kHz clock output will not be affected from settings in the clock adjustment register.
*) When power ON (XSTP=1) 32kHz clock pulses are output from the $\overline{\text{INTRB}}$ pin.

5. Typical Applications

5.1 Examples of Circuits

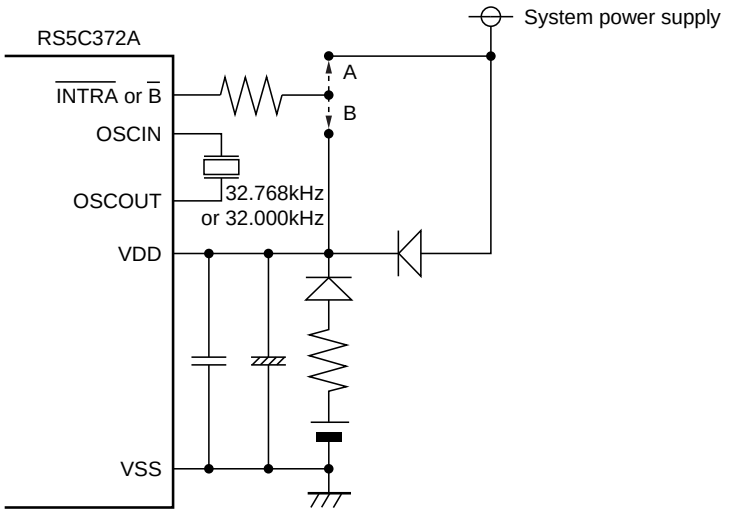
Example 1



*1) Mount the high-and low-frequency by-pass capacitors in parallel and very close to the RS5C372A.

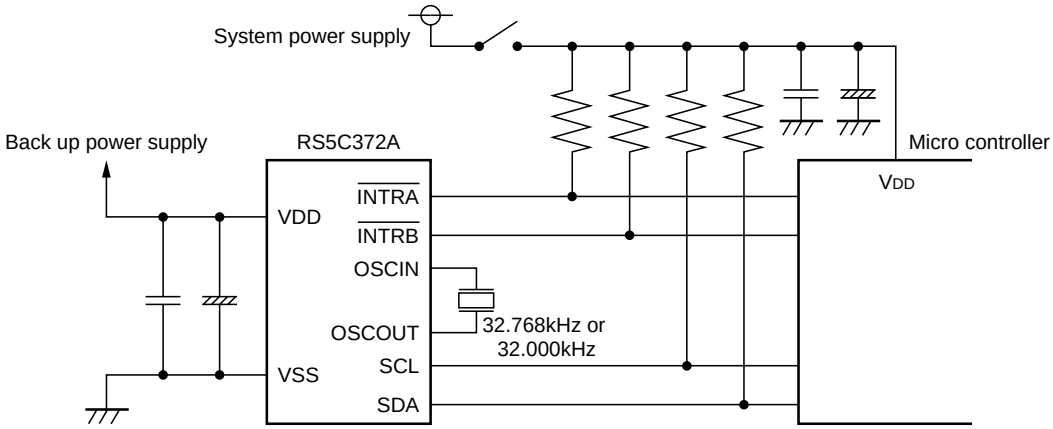
*2) Connect the pull-up resistor of the $\overline{\text{INTRA}}$ pin or the $\overline{\text{INTRB}}$ pin to two different positions depending on whether the resistor is in use during battery back-up:
(I) When not in use during battery back-up
·····Position A in the left figure
(II) When in use during battery back-up
·····Position B in the left figure

Example 2



*1) Connection in the example shown left may not affect the RS5C372A since it is designed to be operational even when the pin voltage exceeds V_{DD}.

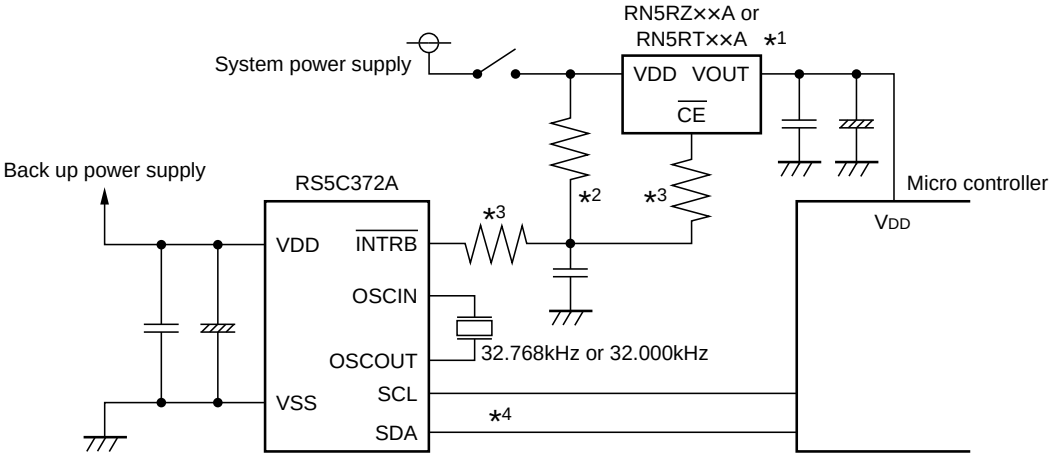
5.2 Example of Interface Circuit to the CPU



*) The SCL and SDA pins of the RS5C372A do not contain protective diodes on V_{DD} side. Therefore, back up power supply≤system power supply causes no adverse effect.

5.3 Example of Power Supply Wake-up Circuit

The sample circuit below has been designed so that system power supply turns on at a time set in the ALARM_B using the ALARM_B of the RS5C372A and the RN5RZ××A (RN5RT××A)*1.



*1) The RN5RZ××A and the RN5RT××A are RICOH regulators with stand-by functions.
*2) The INTRB of the RS5C372A outputs 32kHz clock pulses on power on. A capacitor is included so that CE will not change to "H" while 32kHz clock is off ("H") to allow the regulator to be turned on.
*3) This resistor is used to prevent excess current from flowing into the pins of the RS5C372A and the RN5RZ××A (RN5RT××A) on power on.
*4) Pull-up resistors of the SCL and SDA are not shown in the figure for clarity.

Software Setting

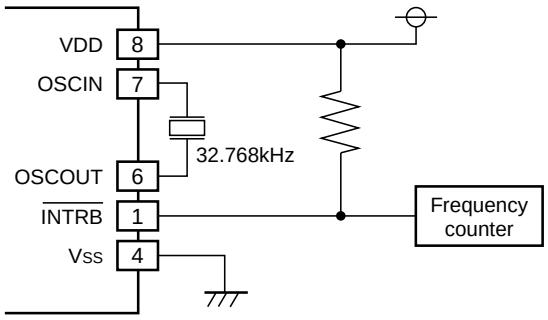
(1) Use periodic interrupt immediately after power on to output ON ("L") from the $\overline{\text{INTRB}}$ pin.

(2) When you want to turn power off use Alarm_B or periodic interrupt to set a timing for power on and output it from the $\overline{\text{INTRB}}$. The $\overline{\text{INTRB}}$ remains off ("H") until the timing specified, high voltage is applied to the regulator $\overline{\text{CE}}$ pin thus power for the micro controller is turned off.

(3) On reaching the specified timing, the $\overline{\text{INTRB}}$ pin switches to on ("L") and power turns on. Hereafter, power is turned off by setting 0 to the BALFG or the CTFG and turned on again at a next timing specified.

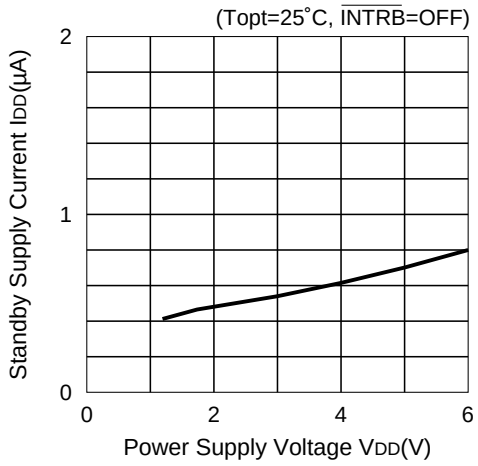
6. Typical Characteristic Measurements

• Test Circuit

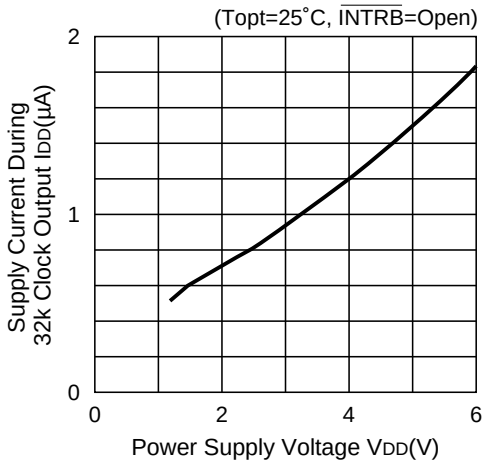


X'tal : 32.768kHz
(R_1=30kΩ TYP.)
(C_L=6pF to 8pF)
Topt : 25˚C
Output pins : Open

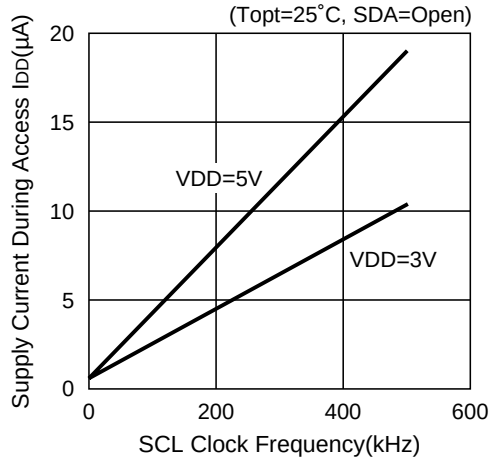
6.1 Standby Supply Current vs. Power Supply Voltage



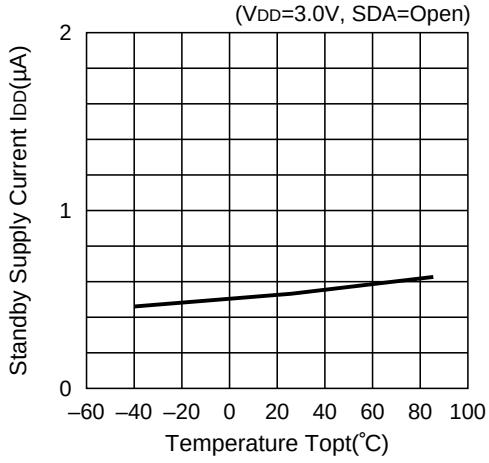
6.2 Supply Current During 32k Clock Output vs. Power Spply Voltage



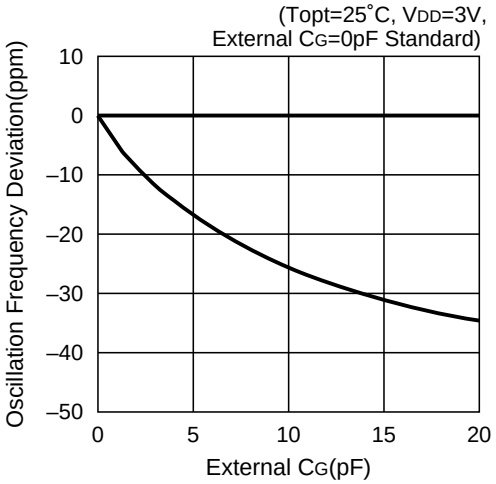
6.3 Supply Current During CPU Access vs. SCL Clock Frequency



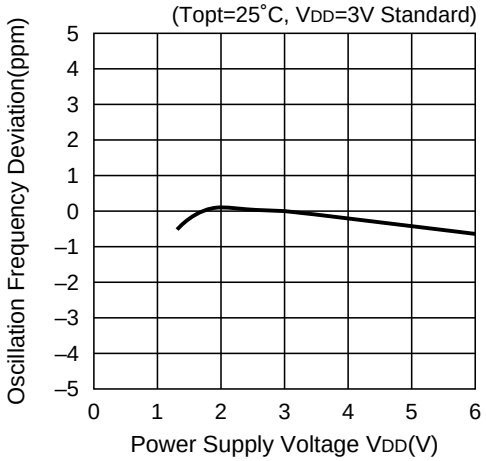
6.4 Standby Supply Current vs. Temperature



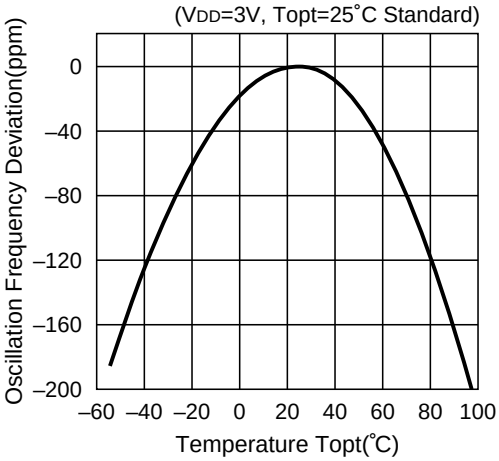
6.5 Oscillation Frequency Deviation vs. External C_G



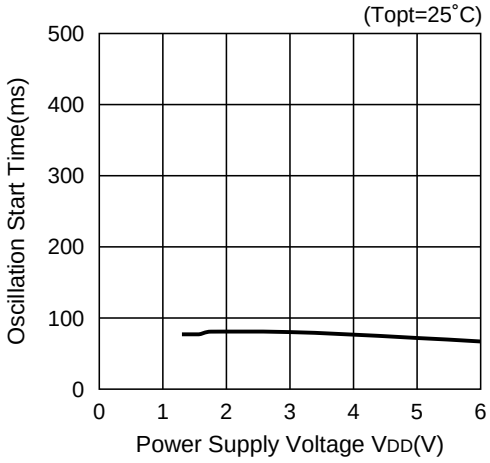
6.6 Oscillation Frequency Deviation vs. Power Supply Voltage



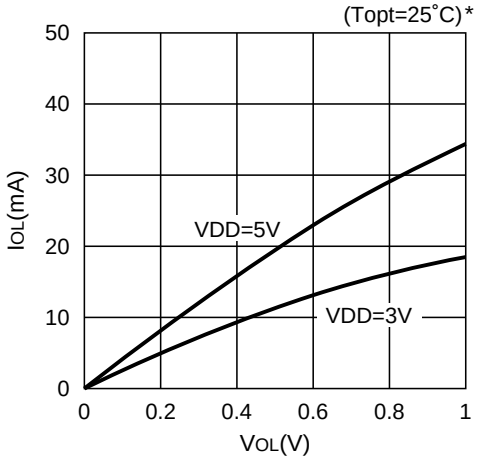
6.7 Oscillation Frequency Deviation vs. Temperature



6.8 Oscillation Start Time vs. Power Supply Voltage



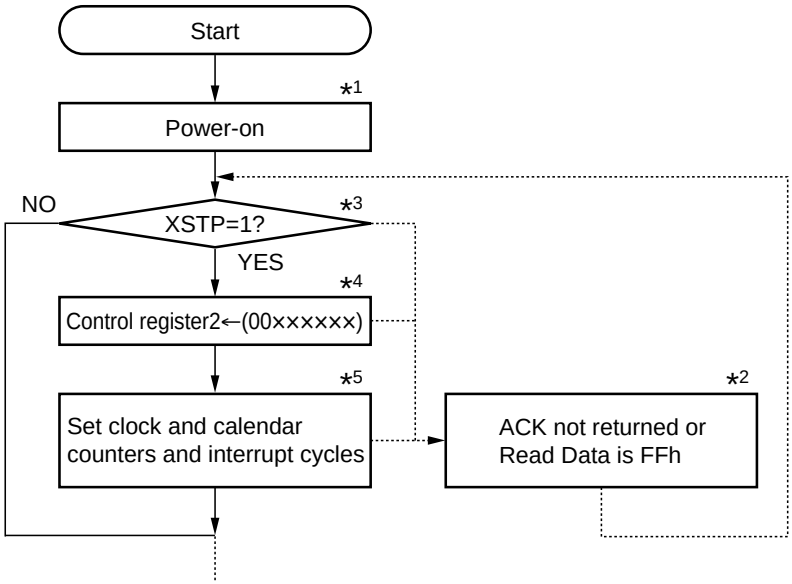
6.9 V_{OL} vs. I_{OL} ($\overline{INTRA}$, $\overline{INTRB}$ pins)



*) Avoid continuous flowing of current of 20mA or more to the $\overline{INTRA}$ or $\overline{INTRB}$ pin.

7. Typical Software-based Operations

7.1 Initialization upon Power-on



*1) Start access after waiting one to two seconds that are required for starting up of oscillation and internal initialization after power on from 0V.

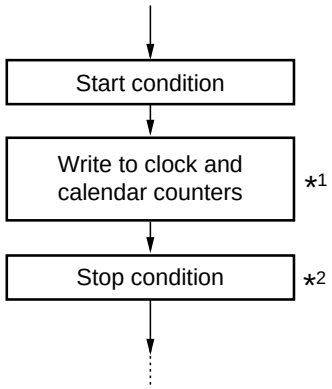
*2) If access is tried during IC internal initialization period described in *1, acknowledge signal may not be output, it is output only at first, or values read may FFh. If any of these occurs, repeat accessing. This will be required also for ordinary routines when accessing may require 0.5 seconds or more.

*3) When XSTP=0 in oscillation halt sensing, it indicates power has not been booted from 0V but from back up supply.

*4) The XSTP shall be set to 0 by setting any data to the control register 2.

*5) Perform ordinary initial setting including clock calendar or interrupt cycle.

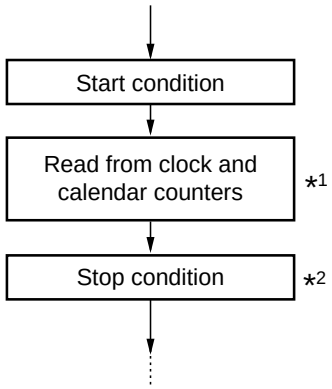
7.2 Write Operation to Clock and Calendar Counters



*1) When writing to clock and calendar counters, do not insert stop condition until all times from second to year have been written to prevent error in writing time.

*2) Take care so that process from start condition to stop condition will be completed within 0.5 seconds. (The RS5C372A forces access to the CPU to terminate within 0.5 to 1.0 seconds after start condition has occurred in case the CPU is failed during access.)

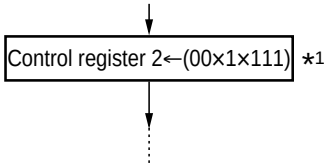
7.3 Read Operation from Clock and Calendar Counters



*1) When reading from clock and calendar counters, do not insert stop condition until all times from second to year have been read to prevent error in reading time.

*2) Take care so that process from start condition to stop condition will be completed within 0.5 seconds. (The RS5C372A forces access to the CPU to terminate within 0.5 to 1.0 seconds after start condition has occurred in case the CPU is failed during access.)

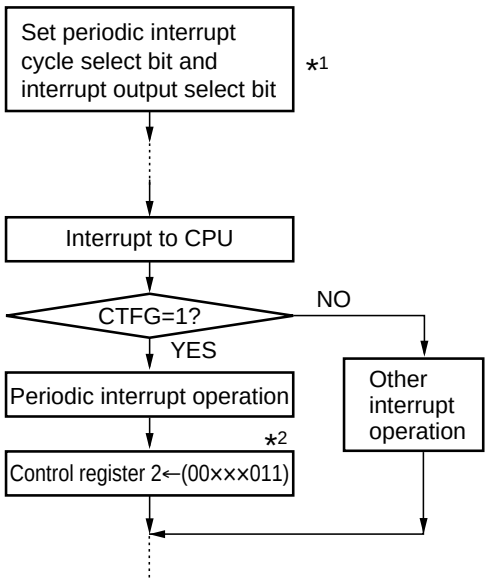
7.4 Second Digit Adjustment by ±30 seconds



*1) Write 1 to the ADJ bit. (The ±30 seconds of adjustment is made within 122.1µs (125µs when 32.000kHz crystal is used) after the ADJ bit is set to 1.)

7.5 Interrupt Operation

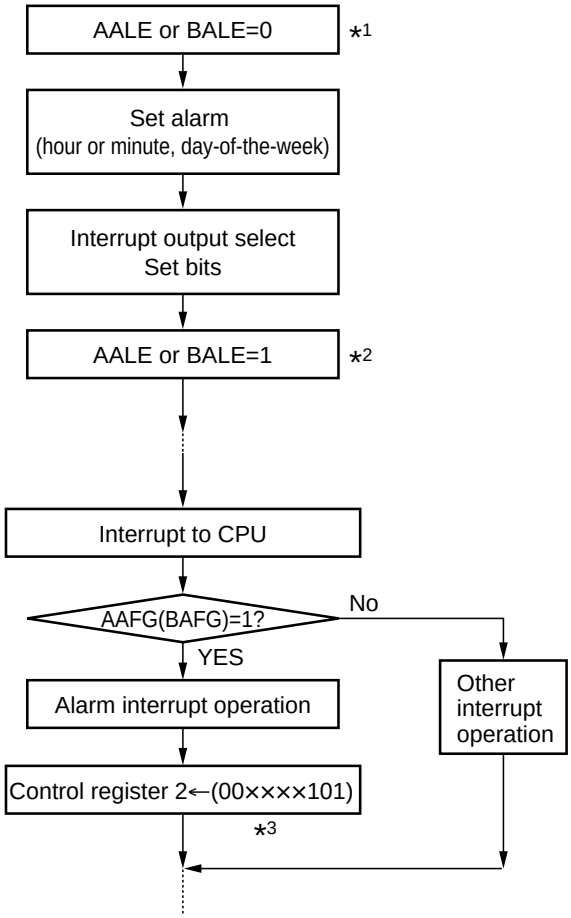
7.5-1 Periodic Interrupt Operation



*1) The level mode is used for the periodic interrupt cycle select bit.

*2) Interrupt to the CPU is cancelled by setting the CTFG bit to 0.

7.5-2 Alarm Interrupt Operation



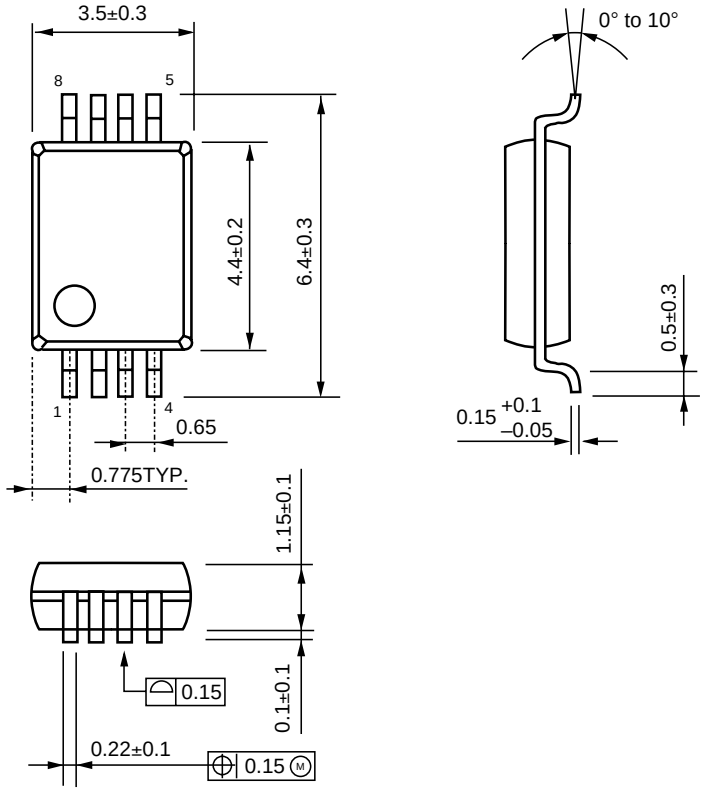
*1) Before setting alarm time, disable alarm function tentatively by setting AALE or BALE to 0 in case the set time agrees with the current time.

*2) After all alarm settings have been completed, enable alarm function.

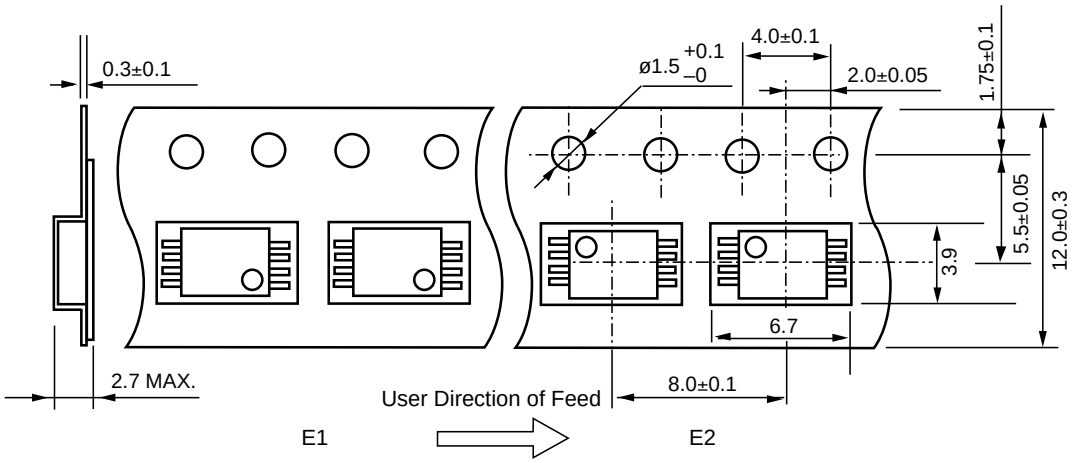
*3) Tentatively unlock alarm.
Write (00×××101) when Alarm_A is used.
Write (00×××110) when Alarm_B is used.

PACKAGE DIMENSION (Unit: mm)

• RS5C372A (8pin SSOP 0.65mm pitch)



TAPING SPECIFICATION (Unit: mm)



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