

CDMA/FM TRANSMIT AGC AMPLIFIER

Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Linear IF Amplifier
- Portable Battery Powered Equipment
- Commercial and Consumer Systems

Product Description

The RF2609 is a complete AGC amplifier designed for the transmit section of dual-mode CDMA/FM cellular applications. It is designed to amplify IF signals while providing more than 84dB of gain control range. Noise Figure, IP3, and other specifications are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. This circuit is designed as part of the RFMD CDMA Chip Set, consisting of this Transmit IF AGC Amp, a Transmit Upconverter, a Receive LNA/Mixer, and a Receive IF AGC Amp. The IC is manufactured on an advanced high frequency Silicon Bipolar process and is packaged in a standard miniature 16-lead plastic SSOP package.

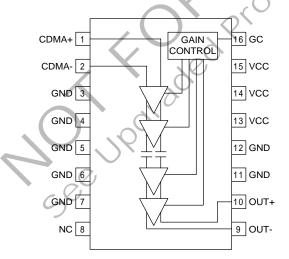
Optimum Technology Matching® Applied

▼ Si BJT

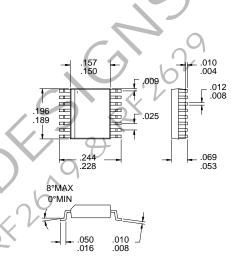
Si Bi-CMOS

☐ GaAs HBT ☐ SiGe HBT

☐ GaAs MESFET☐ Si CMOS



Functional Block Diagram



Package Style: SSOP-16

Features

- Supports Dual Mode Operation
- -48dB to +42dB Gain Control Range
- IS-95 CDMA Compatible
- Monolithic Construction
- 12MHz to 175MHz Operation
- Miniature Surface Mount Package

Ordering Information

RF2609 CDMA/FM Transmit AGC Amplifier RF2609 PCBA Fully Assembled Evaluation Board

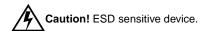
RF Micro Devices, Inc. 7625 Thorndike Road Greensboro, NC 27409, USA Tel (336) 664 1233 Fax (336) 664 0454 http://www.rfmd.com

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RF2609

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V_{DC}
Control Voltage	-0.5 to +5.0	V
Input Power Levels	+10	dBm
Operating Ambient Temperature	-40 to +85	℃
Storage Temperature	-40 to +150	℃



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Parameter	;	Specification		11:4	Condition
Parameter	Min. Typ. Max.		Unit	Condition	
Overall					T=25°C, 130MHz, V_{CC} =3.6V, Z_{S} =1kΩ, Z_{L} =1kΩ, 1kΩ External Output Terminating Resistor (Effective Z_{L} =500Ω) (See Application 1)
Frequency Range		12 to 175		MHz	tion Example)
Maximum Gain	+39	+42		dB	V _{GC} =2.76V
Minimum Gain		-48	-45	dB	V _{GC} =0.2V
Gain Slope		47		dB/V	Measured in 0.5V increments
Gain Control Voltage Range		0 to 3		V _{DC}	
Gain Control Input Impedance		30		kΩ	
Noise Figure Input IP3	-26	10 -25		dB dBm	At maximum gain and 130MHz At +10 gain and referenced to 1kΩ
Input Impedance	-20	-25 1		kΩ	Differential
Stability (Max VSWR)	10:1			Naz C	Spurious<-70dBm
Power Supply			13	10	
Voltage		3.3 to 3.6	V 05	100	
Current Consumption Current Consumption		23 22	25	mA mA	Maximum gain Minimum gain
	2ded	RKOC			
See Jipos					

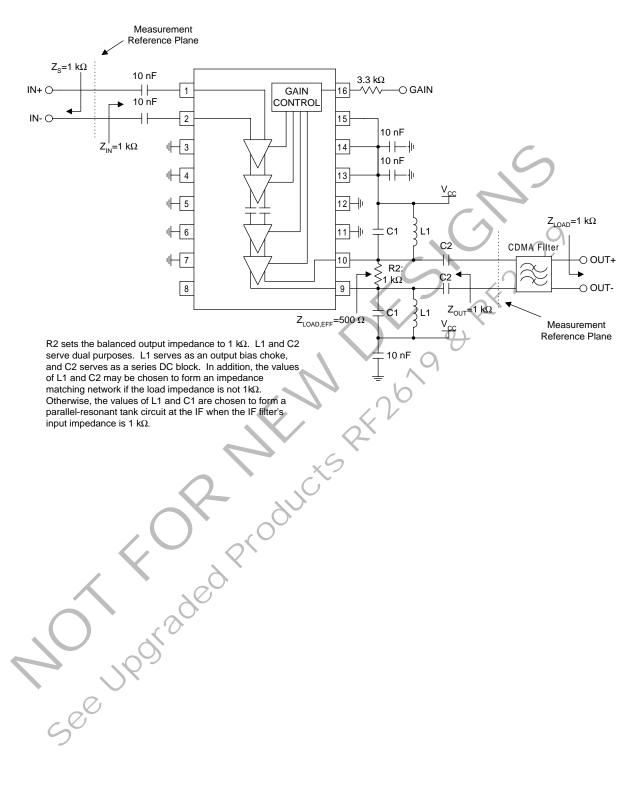
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Pin	Function	Description	Interface Schematic
1	CDMA+	CDMA Balanced Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with a DC level, other than V_{CC} ,	V _{cc}
		present. A DC to connection to V _{CC} is acceptable. For single-ended	
		input operation, one pin is used as an input and the other CDMA input is AC coupled to ground. The balanced input impedance is $1\mathrm{k}\Omega$, while	CDMA+ O CDMA-
		the single-ended input impedance is 500Ω .	, <u> </u>
			¥
2	CDMA-	Same as pin 2, except complementary input.	See pin 1 schematic.
3	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
4	GND	Same as pin 3.	
5	GND	Same as pin 3.	
6	GND	Same as pin 3.	
7	GND	Same as pin 3.	
8	NC	No Connection pin. This pin is internally biased and should not be connected to any external circuitry, including ground or V_{CC} .	
9	OUT-	Balanced Output pin. This is an open-collector output, designed to operate into a 500Ω balanced load. The load sets the operating impedance, but an external choke or matching inductor to V_{CC} must also be supplied in order to correctly bias this output. This bias inductor is typically incorporated in the matching network between the output and next stage. Because this pin is biased to V_{CC} , a DC blocking capacitor must be used if the next stage's input has a DC path to ground.	OUT+O COOUT-
10	OUT+	Same as pin 9, except complementary output.	See pin 9 schematic.
11	GND	Same as pin 3.	occ piii o scricinatic.
12	GND	Same as pin 3.	
13	VCC	Supply Voltage pin. External bypassing is required. The trace length	
10	100	between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Pins 13, 14, and 15 may share one bypass capacitor if trace lengths are kept minimal.	
14	VCC	Same as pin 13.	
15	VCC	Same as pin 13.	
16	GC	Analog gain adjustment for all amplifiers. Valid control ranges are from 0V to 3.0V. Maximum gain is selected with 3.0V. Minimum gain is selected with 0V. These voltages are valid only for a $3.3 k\Omega$ DC source impedance.	V _{CC} ≥12.7 kΩ ≥3.5 kΩ ≥15 kΩ
4) 1800 11800		

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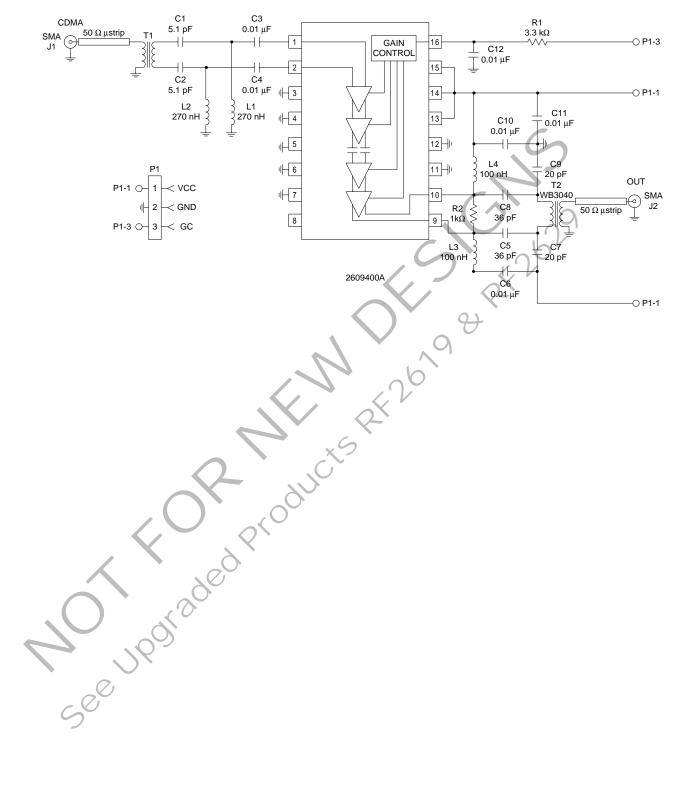
Application Schematic



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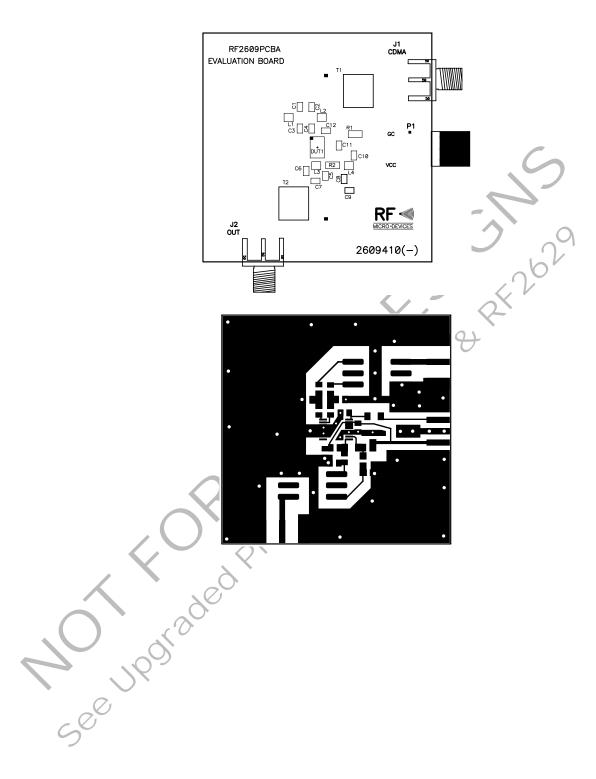
Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



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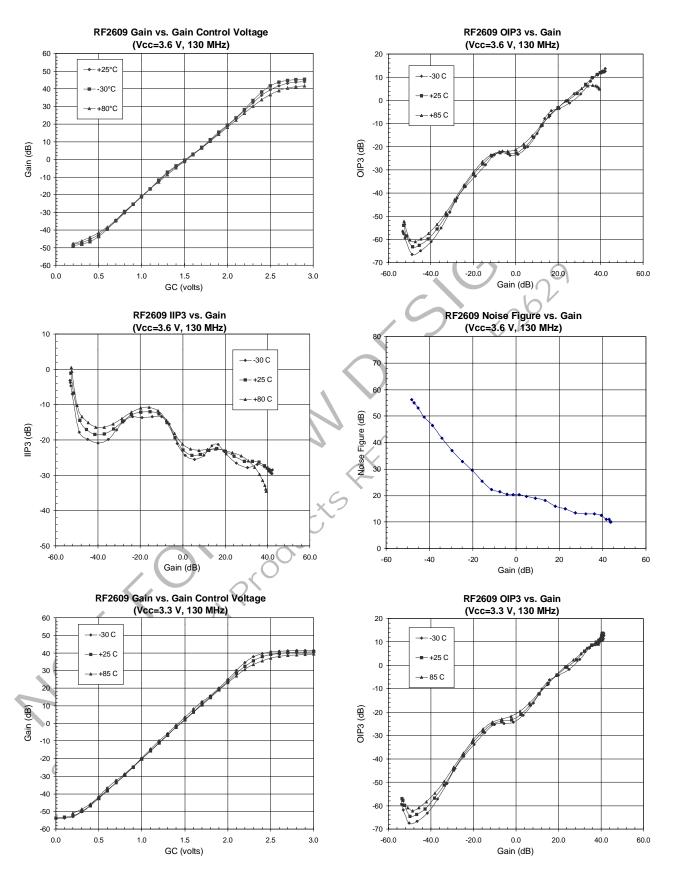
Evaluation Board Layout



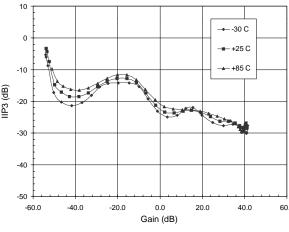
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