

#### CDMA/FM LOW NOISE AMPLIFIER/MIXER

### Typical Applications

- CDMA/FM Cellular Systems
- Supports Dual-Mode AMPS/CDMA
- Supports Dual-Mode TACS/CDMA
- General Purpose Downconverter
- Commercial and Consumer Systems
- Portable Battery Powered Equipment

### **Product Description**

The RF2406 is a receiver front-end designed for the receive section of dual-mode CDMA/FM cellular applications. It is designed to amplify and down-convert RF signals while providing 30 dB of stepped gain control range and features digital control of LNA gain, IF output selection, LO buffer enable, power down mode, and low current "lazy" mode. The digitally selected "lazy" mode reduces current drain by approximately 10mA, putting the IC in a lower current drain, noise and IP3 state. This gives the receiver designer added flexibility to dynamically optimize these downconverter parameters. Noise Figure, IP3, and other specs are designed to be compatible with the IS-95 Interim Standard for CDMA cellular communications. The IC is manufactured on an advanced Silicon Bipolar process and packaged in an SSOP-28.

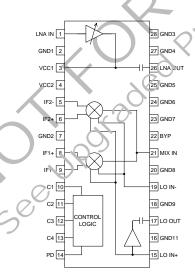
Optimum Technology Matching® Applied

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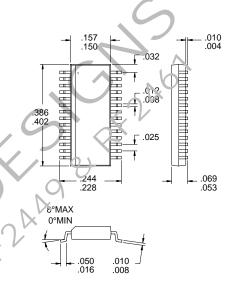
☐ GaAs HBT ☐ SiGe HBT

☐ GaAs MESFET☐ Si CMOS

Si Bi-CMOS



Functional Block Diagram



Package Style: SSOP-28

#### **Features**

- Complete Receiver Front-End
- Stepped LNA Gain Control
- Low Current-Drain "Lazy" Mode
- Buffered LO Output
- Digitally Selectable IF Outputs
- 500MHz to 1100MHz Operation

#### Ordering Information

RF2406 CDMA/FM Low Noise Amplifier/Mixer RF2406 PCBA Fully Assembled Evaluation Board

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## RF2406

### **Absolute Maximum Ratings**

Parameter	Rating	Unit
Supply Voltage	-0.5 to +5.0	$V_{DC}$
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C



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Doromotor	Specification			Unit	Condition	
Parameter	Min.	Typ. Max.		Unit	Condition	
Overall					T=25°C, V <sub>CC</sub> =3.6V, RF=881 MHz, LO=966 MHz @-3dBm RF2=882 MHz for IIP3 Measurements See Mode Control Logic Table	
RF Frequency Range		500 to 1100		MHz	Coo mode Control Eogle Table	
LO Frequency Range IF Frequency Range		500 to 1100 0.1 to 250		MHz MHz	() 10	
Power Supply		0.1 to 200		IVII IZ	.0.	
Voltage		2.7 to 4.0		V		
Current Consumption		20		mA	FM	
Current Consumption		25		mA	CDMA Max. Gain	
		26		mA	CDMA Nom. Gain	
		18		mA	CDMA Min. Gain	
		adds 4		mA	LO Buffer ON	
		subtracts 10		mA ×	"Lazy" Mode	
		< 20		uА	Power Down	
Max Dynamic Range Mode		120			1 0.00 20.00	
Cascaded Perform. to IF1			9		1k $\Omega$ balanced load, 3.0dB Image Filter Loss CDMA Max. Gain	
Cascade Conversion Gain		24	X	dB	OBINIT Max. Gain	
Cascade Input IP3 to IF1		-4	.5	dBm		
Cascade Noise Figure		4.3		dB		
Cascaded Perform. to IF2					870Ω load, 3dB Image Filter Loss	
Cascade Conversion Gain	< 1	18		dB	1 101	
Cascade Input IP3		24		dBm		
Cascade Noise Figure		4.3		dB		
First Section (LNA)	,	7.0		u.b		
Gain		14.5		dB	FM and CDMA Max. Gain	
	. 0	7.5		dB	CDMA Nom. Gain	
	70	-5		dB	CDMA Min. Gain	
Noise Figure		2.5		dB	FM and CDMA Max. Gain	
- Sant	.0	4.5		dB	CDMA Nom. Gain	
		9.0		dB	CDMA Min. Gain	
Input IP3	7	+7		dBm	FM and CDMA Max. Gain	
10,118		>+14		dBm	CDMA Nom. Gain	
		>+20		dBm	CDMA Min. Gain	
Input P1dB		-11		dBm	FM and CDMA Max. Gain	
Reverse Isolation		25		dB	FM and CDMA Max. Gain	
Input VSWR		<4:1			Internally matched for optimum noise figure from 50Ω source	
Output VSWR		<1.5:1			With external match (partial)	

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Second Section (Mixer, IF1 or IF2 Output)	Danamatan	Specification			11:4	Condition	
or IF2 Output)         dB         IF 1, 1 kΩ balanced load.           Conversion Gain         16         dB         IF 1, 1 kΩ balanced load.           Noise Figure         11.5         dB         Single sideband.           Input IP3 to IF1         +7         dBm           Input IP3 to IF2         +7         dBm           Input IP1dB, IF2         -4         dBm           Input IP1dB, IF2         -8         dBm           IF1, IF2 Output Freq. Range         70 to 100         MHz           Output Impedance         870         MHz           IF1, IF2 Output Freq. Range         70 to 100           Uput Impedance         870         MHz           UD Input Range         6 to 0         dBm           LO Input Range         6 to 0         dBm           LO Input Level         0         dBm           LO IN to IF1, IF2 Rejection         37         dB           LO Input VSWR         <2:1         With external matching network           **Lazy" Mode         **Lazy" Mode           **Cascaded Perform. to IF1         **Lazy" Mode           **Cascaded Perform. to IF2         **B         dB           **Cascaded Perform. to IF2         **B         dB	Parameter	Min.	Тур.	Max.	Unit	Condition	
or IF2 Output)         dB         IF 1, 1 kΩ balanced load.           Conversion Gain         16         dB         IF 1, 1 kΩ balanced load.           Noise Figure         11.5         dB         Single sideband.           Input IP3 to IF1         +7         dBm           Input IP3 to IF2         +7         dBm           Input P1dB, IF2         +4         dBm           Input P1dB, IF2         -4         dBm           Input P1dB, IF2         -8         dBm           IF1, IF2 Output Freq. Range         70 to 100         MHz           Output Impedance         870         MHz         With external IF interface network           IF1, IF2 Output Freq. Range         70 to 100         MHz         With external IF interface network           LO Input         B70         MHz         With external IF interface network           LO Input Range         6 to 0         dBm         dBm           LO Unput Level         0         dBm         Buffer ON, 0dBm input           LO Input Level         -35         dBm         Buffer, OFF, 0dBm input           LO Input VSWR         -2:1         Vith external matching network           *Lazy" Mode         ***         ***         ***           Cascade	Second Section (Mixer, IF1						
Noise Figure	or IF2 Output)						
Noise Figure	Conversion Gain		16		dB	IF 1, 1kΩ balanced load.	
Input VSWR			7		dB	IF 2, 870Ω load.	
Input IP3 to IF1	Noise Figure		11.5		dB	Single sideband.	
Input   P3 to   F2   Input   P1dB,   F2   Input   P1dB,   F2   Input   P1dB,   F2   Input   P1dB,   F3   Input   P1dB,   F4   Input   P1dB   Inp	Input VSWR		<1.5:1			With external matching network	
Input P1dB, IF2   -4   -8   dBm	Input IP3 to IF1		+7		dBm		
Input P1dB, IF1	Input IP3 to IF2		+7		dBm		
Mix   N to   F1,   F2 Rejection   70 to 100   MHz   F1   F2 Output Freq, Range   70 to 100   MHz   F1   F2 Output Freq, Range   70 to 100   MHz   F1   balanced, open collector   F2   single ended, with external inductor.   F3   Single ended, with external inductor.   F4   Single ended, w	Input P1dB, IF2		-4		dBm		
F1, IF2 Output Freq. Range	Input P1dB, IF1				-		
Section   Sec	MIX IN to IF1, IF2 Rejection		35		-		
B70			70 to 100				
LO Input   LO Input Range   LO Input Range   LO Output Level   O	Output Impedance		· ·				
LO   Input Range   Co to 0   Description   Coutput Level   Co   Coutput Level   Cou			870		Ω	IF2, single ended, with external inductor.	
LO Output Level         0         dBm dBm dBm Buffer ON, 0 dBm input           LO Output Level         -35         dBm Buffer OPF, 0 dBm input           LO IN to LNA Input Rejection         15         dB           LO IN to IF1, IF2 Rejection         15         dB           LO Input VSWR         <2:1	- I						
LO Output Level         -35         dBm dB         Buffer OFF, 0dBm input           LO IN to LNA Input Rejection         15         dB         dB           LO IN to IF1, IF2 Rejection         15         dB         With external matching network           **Cascaded Perform. to IF1           Cascaded Perform. to IF1         21         dB         dBm dBm           Cascade Conversion Gain         21         dB         dBm dBm           Cascaded Perform. to IF2         8         dBm dBm         dBm           Cascaded Perform. to IF2         8         dBm         dBm           Cascade Conversion Gain         15.3         dBm         dBm           Cascade Input IP3         8         dBm         dBm           Cascade Input IP3         8         dBm         dBm           Cascade Input IP3         8         dBm         CDMA Max. Gain           CDMA Nom. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Noise Figure         2.4         dB         FM and CDMA Max. Gain           Input IP3         +1         dBm         FM and CDMA Max. Gain           Input IP3         +1         dBm         FM and CDMA Max. Gain           Input IP4B         -16         dBm							
LO IN to LNA Input Rejection         37         dB dB         With external matching network           LO IN to IF1, IF2 Rejection         42.1         With external matching network           "Lazy" Mode         **LSD balanced load, 3.0 dB Image Filter Loss. CDMA Max. Gain           Cascaded Perform. to IF1         dB         CDMA Max. Gain           Cascade Input IP3 to IF1         -8         dBm           Cascaded Perform. to IF2         B870Ω load, 3dB Image Filter Loss.           Cascade Conversion Gain         15.3         dB           Cascade Input IP3         -8         dBm           Cascade Noise Figure         4.0         dB           First Section (LNA)         9.0         dB         FM and CDMA Max. Gain           CDMA Nom. Gain         CDMA Nom. Gain         CDMA Nom. Gain           CDMA Nom. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Lobert Gain         4.8         dB         CDMA Nom. Gain           Lobert Gain			0				
LO IN to IF1, IF2 Rejection						Buffer OFF, 0dBm input	
Cascaded Perform. to IF1						<u> </u>	
"Lazy" Mode  Cascaded Perform. to IF1  Cascade Conversion Gain Cascade Input IP3 to IF1 Cascade Perform. to IF2  Cascaded Perform. to IF2  Cascaded Perform. to IF2  Cascaded Perform. to IF2  Cascaded Conversion Gain Cascade Input IP3 Cascade Roise Figure  First Section (LNA)  Gain  Noise Figure  A.8  A.9  A.9  A.9  A.9  A.9  A.9  A.9	-				dB	0.)	
Cascaded Perform. to IF1   Cascade Conversion Gain   Cascade Input IP3 to IF1   -8   dBm   dB			<2:1			With external matching network	
Cascade Conversion Gain         21         dB         CDMA Max. Gain           Cascade Input IP3 to IF1         -8         dBm         870Ω load, 3dB Image Filter Loss.           Cascade Perform. to IF2         870Ω load, 3dB Image Filter Loss.         FM           Cascade Conversion Gain         15.3         dB           Cascade Input IP3         -8         dBm           Cascade Noise Figure         4.0         dB           First Section (LNA)         4.0         dB           Gain         9.0         dB         FM and CDMA Max. Gain           CDMA Nom. Gain         CDMA Nom. Gain         CDMA Min. Gain           Noise Figure         4.8         dB         FM and CDMA Max. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA Nom. Gain         CDMA Nom. Gain           Low A Max. Gain         CDMA	"Lazy" Mode						
Cascade Input IP3 to IF1         -8         dBm         dB           Cascaded Perform. to IF2         Cascaded Perform. to IF2         870Ω load, 3dB Image Filter Loss. FM           Cascade Conversion Gain Cascade Input IP3         -8         dBm         4.0         BFM and CDMA Max. Gain CDMA Max. Gain CDMA Max. Gain CDMA Min. Gain Internally matched for optimum noise figure from 50Ω source	Cascaded Perform. to IF1		•		N.A.	1kΩ balanced load, 3.0dB Image Filter Loss. CDMA Max. Gain	
Cascade Noise Figure         4.1         dB           Cascaded Perform. to IF2         870Ω load, 3dB Image Filter Loss. FM           Cascade Conversion Gain Cascade Input IP3 Cascade Noise Figure         4.0         dB           First Section (LNA)         4.0         dB         FM and CDMA Max. Gain CDMA Nom. Gain CDMA Min. Gain FM and CDMA Max. Gain CDMA Nom. Gain CDMA Max. Gain Internally matched for optimum noise figure from 50Ω source					( )		
Cascaded Perform. to IF2         870Ω load, 3dB Image Filter Loss. FM           Cascade Conversion Gain         15.3         dB           Cascade Input IP3         -8         dBm           Cascade Noise Figure         4.0         dB           First Section (LNA)         9.0         dB         FM and CDMA Max. Gain           Gain         6.2         dB         CDMA Nom. Gain           CDMA Min. Gain         CDMA Min. Gain         CDMA Nom. Gain           Logonome         4.8         dB         CDMA Min. Gain           Logonome         4.8         dB         CDMA Min. Gain           Logonome         4.8         dBm         CDMA Mom. Gain           Logonome         4.8         dBm         CDMA Mom. Gain           Logonome         4.8         dBm         CDMA Mom. Gain           Logonome         CDMA Mom. Gain         CDMA Mom. Gain           Logonome         CDMA Min. Gain         CDMA Min. Gain				7	dBm		
Cascade Conversion Gain         15.3         dB dBm dBm dB           Cascade Input IP3         4.0         dB           Cascade Noise Figure         4.0         dB           First Section (LNA)           Gain         9.0         dB         FM and CDMA Max. Gain           6.2         dB         CDMA Nom. Gain           Noise Figure         2.4         dB         FM and CDMA Max. Gain           Input IP3         4.8         dB         CDMA Nom. Gain           Input IP3         +1         dBm         FM and CDMA Max. Gain           Input P1dB         >+6         dBm         CDMA Nom. Gain           Input P1dB         -16         dBm         FM and CDMA Max. Gain           Reverse Isolation         25         dB         FM and CDMA Max. Gain           Input VSWR         44:1         Internally matched for optimum noise figure from 50Ω source	Cascade Noise Figure		4.1		dB		
Cascade Input IP3         -8         dBm           Cascade Noise Figure         4.0         dB           First Section (LNA)           Gain         9.0         dB         FM and CDMA Max. Gain           6.2         dB         CDMA Nom. Gain           Noise Figure         2.4         dB         FM and CDMA Max. Gain           Noise Figure         4.8         dB         CDMA Nom. Gain           1	Cascaded Perform. to IF2						
Cascade Noise Figure   4.0   dB			15.3	x9	dB		
Section (LNA)   Sain   Solution   Solutio	Cascade Input IP3		-8		dBm		
Sain	Cascade Noise Figure		4.0		dB		
CDMA Nom. Gain   CDMA Min. Gain   GB   CDMA Min. Gain   GB   CDMA Min. Gain   GB   CDMA Mom. Gain   GB   CDMA Nom. Gain   GB   CDMA Nom. Gain   GB   CDMA Min. Gain   GB   GB   GB   GB   GB   GB   GB   G	First Section (LNA)						
CDMA Min. Gain	Gain				dB	FM and CDMA Max. Gain	
Description					dB	CDMA Nom. Gain	
4.8 9.0 Input IP3  And CDMA Nom. Gain CDMA Min. Gain FM and CDMA Max. Gain CDMA Nom. Gain CDMA		) 1	-5		dB	CDMA Min. Gain	
9.0 Input IP3  dB CDMA Min. Gain FM and CDMA Max. Gain CDMA Nom. Gain CDMA Nom. Gain CDMA Min.	Noise Figure		2.4		dB	FM and CDMA Max. Gain	
Input IP3  +1 >+6 >+20 Input P1dB Reverse Isolation Input VSWR  +1 >+6 >+20 dBm dBm CDMA Nom. Gain CDMA Min. Gain CDMA Min. Gain CDMA Max. Gain dBm FM and CDMA Max. Gain dBm FM and CDMA Max. Gain Internally matched for optimum noise figure from 50Ω source			4.8		-	CDMA Nom. Gain	
S+6   S+20   Shape		70				CDMA Min. Gain	
Several Input P1dB	Input IP3						
Input P1dB		<b>&gt;</b>					
Reverse Isolation 25 dB FM and CDMA Max. Gain Internally matched for optimum noise figure from 50Ω source							
Input VSWR							
from 50Ω source					dB		
Output VSWR /   <1.5:1   With external match (partial)			<4:1				
That officer (partial)	Output VSWR		<1.5:1			With external match (partial)	

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Doromotor	Specification		11!4	O a malistica m		
Parameter	Min.	Тур.	Max.	Unit	Condition	
Second Section (Mixer, IF1						
or IF2 Output)						
Conversion Gain		14		dB	IF 1, 1kΩ balanced load.	
		5.5		dB	IF 2, 870Ω load.	
Noise Figure		9.5		dB	Single sideband.	
Input VSWR		<1.5:1			With external matching network	
Input IP3 to IF1		+2		dBm	_	
Input IP3 to IF2		+2		dBm		
Input P1dB, IF2		-9		dBm		
Input P1dB, IF1		-6		dBm		
MIX IN to IF1, IF2 Rejection		35		dB		
IF1, IF2 Output Freq. Range		70 to 100		MHz	With external IF interface network	
Output Impedance		>1		kΩ	IF1, balanced, open collector	
		870		Ω	IF2, single ended, with external inductor.	
LO Input						
LO Input Range		-6 to 0		dBm		
LO Output Level		0		dBm	Buffer On, 0dBm input	
LO Output Level		-35		dBm	Buffer Off, 0dBm input	
LO IN to LNA Input Rejection		30		dB	/ -	
LO IN to IF1, IF2 Rejection		15		dB		
LO Input VSWR		<2:1		LX/	With external matching network	

### Mode Control Logic

					V *
MODE	C1	C2	C3	C4	PD
FM (IF2)	L	H	X	)H	Н
CDMA Max. Gain (IF1)	Н	Н	Х	H	Н
CDMA Nom. Gain (IF1)	Η	L	X	H	Η
CDMA Min. Gain (IF1)	L	1	X	H	Ι
Lazy FM (IF2)	L	Н	X	L	Η
Lazy CDMA Max. Gain (IF1)	Н	Ĥ	X	L	Η
Lazy CDMA Nom. Gain (IF1)	H	L	Х	L	Н
Lazy CDMA Min. Gain (IF1)		L	X	L	Η
LO Buffer ON	X	Х	Н	X	Н
LO Buffer OFF	X	Х	L	Х	X
Power Down		X	X	Х	L
See John	X 2de				

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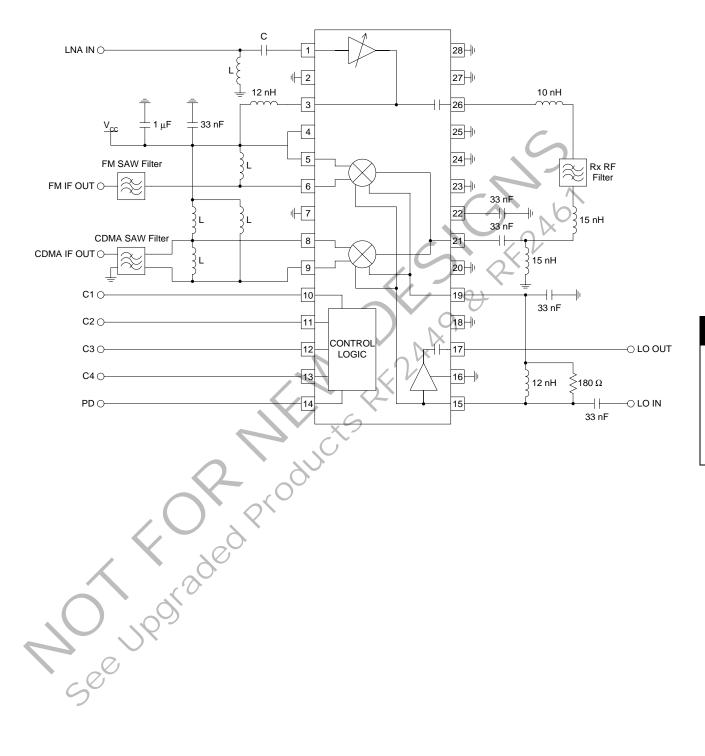
Pin	Function	Description	Interface Schematic
1	LNA IN	RF Input pin. This pin is internally matched for optimum noise figure from a $50\Omega$ source. This pin is internally DC biased and, if connected to a device with DC present, should be DC blocked with a capacitor suitable for the frequency of operation.	LNA IN O
2	GND1	Ground connection for the LNA circuits. Keep traces physically short and connect immediately to ground plane for best performance.	
3	VCC1	Supply Voltage for the LNA. External inductance, ~12nH, is required in addition to internal inductance to achieve optimum LNA performance. This extra inductance can be easily achieved with a thin microstrip line. The value of this inductance will change with the frequency of operation. RF and IF bypassing is required on the supply side of the inductance. The ground side of the bypass capacitors should connect immediately to ground plane.	See pin 1.
4	VCC2	Supply Voltage for the LO buffer amplifier, bias circuits, and control logic. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	VCC2 BIAS COUT
5	IF2-	Same as pin 6, except complementary output. For typical single ended operation, this pin is connected directly to $V_{\rm CC}$ .	See pin 6.
6	IF2+	FM IF Output pin. This is a balanced output, but is typically used as a single-ended output. The internal circuitry, in conjunction with an external matching/bias inductor to $V_{CC}$ , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, is about $870\Omega$ at $85\text{MHz}$ . Because this pin is biased to $V_{CC}$ , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	1F2+ 1F2- 8.5 pF 2.1 kΩ
7	GND2	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
8	IF 1+	CDMA IF Output pin. This is a balanced output. The internal circuitry, in conjunction with an external matching/bias inductor to $V_{CC}$ , sets the operating impedance. This inductor is typically incorporated in the matching network between the output and IF filter. The net output impedance, including the external inductor, at 85MHz is higher than $1k\Omega$ , even though the part is designed to drive a $1k\Omega$ load. Because this pin is biased to $V_{CC}$ , a DC blocking capacitor must be used if the IF filter input has a DC path to ground. See Application Schematic.	IF1+ GND2 IF1- 1.2 1.2 pF pF
9	IF 1-	Same as pin 8, except complementary output.	See pin 8.
10	C1 0	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6 V, and the pin draws less than $50\mu\text{A}$ when selected.	C1 O - W
11	C2	Control line for mode/gain select. See specification table for details. The threshold voltage is 1.6 V, and the pin draws less than $50\mu\text{A}$ when selected.	C3 O−√√√ ▶ ↓ ↓
12	C3	Enable pin for the LO output buffer amplifier. This is a digitally controlled input. A logic "high" turns the buffer amplifier on, and the current consumption increases by 4mA (with 0dBm LO input). A logic "low" turns the buffer amplifier off. The threshold voltage is approximately 1.6 V.	C3 O//

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Pin	Function	Description	Interface Schematic
13	C4	Enable pin for "Lazy Mode". This is a digitally controlled input. A logic "high" maintains the part in full performance mode. A logic "low" places the part in a reduced-current/reduced performance mode. See the specification table for details. The threshold voltage is 1.6 V, and the pin draws less than $50\mu\text{A}$ when selected.	C4 Ο—VVV—————————————————————————————————
14	PD	Power down pin. A logic "low" turns the part off. A logic "high" (>1.6V) turns the part on. In addition, pin 10 (C1) should also be taken low during power down.	PD 0
15	LO IN+	Mixer LO Balanced Input Pin. For single-ended input operation, this pin is used as an input and pin 18 is bypassed to ground.	LO IN-
16	GND11	Ground connection for LO buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
17	LO OUT	Optional Buffered LO Output. This pin is internally DC blocked and matched to $50\Omega$ . The buffer amplifier is switched on or off by the voltage level at pin 12.	See pin 4.
18	GND9	Die flag ground. Keep traces physically short and connect immediately to ground plane for best performance.	
19	LO IN-	Mixer LO bypass.	See pin 15.
20	GND8	Ground connection for the mixer. Keep traces physically short and connect immediately to ground plane for best performance.	
21	MIX IN	Mixer RF Input Pin. This pin is internally DC biased and should be DC blocked if connected to a device with DC present. External matching network sets RF and IF impedance for optimum performance.	MIX IN O
22	ВҮР	Internal voltage reference. External RF and IF bypassing is required. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane.	
23	GND7	Same as pin 2.	
24	GND6	Same as pin 2.	
25	GND5	Same as pin 2.	
26	LNA OUT	LNA Output pin. This pin is internally DC blocked and externally matched to $50\Omega$ at pin 3 in order to facilitate an easy interface to a $50\Omega$ lmage Filter.	See pin 1.
27	GND4	Same as pin 25.	
28	GND3	Same as pin 25.	
1	See		

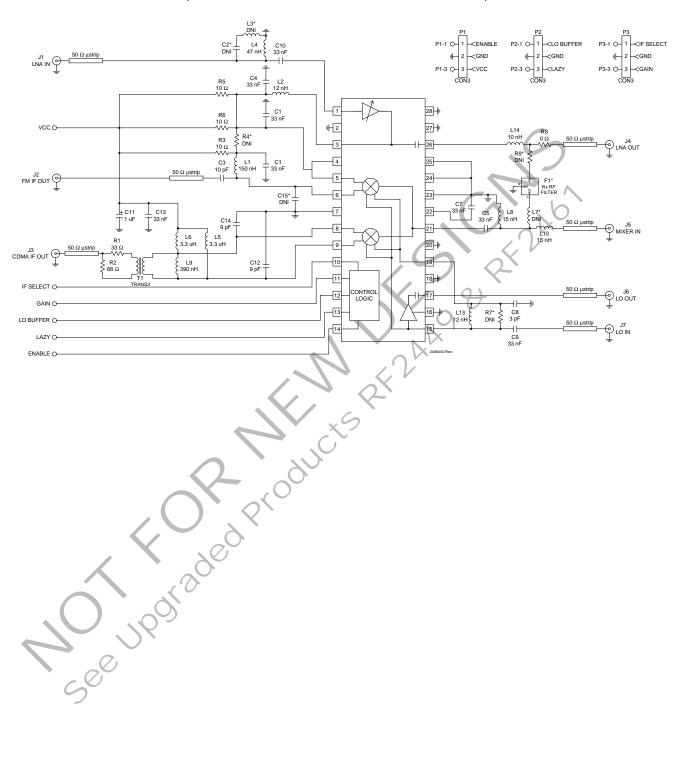
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### **Application Schematic**



### **Evaluation Board Schematic**

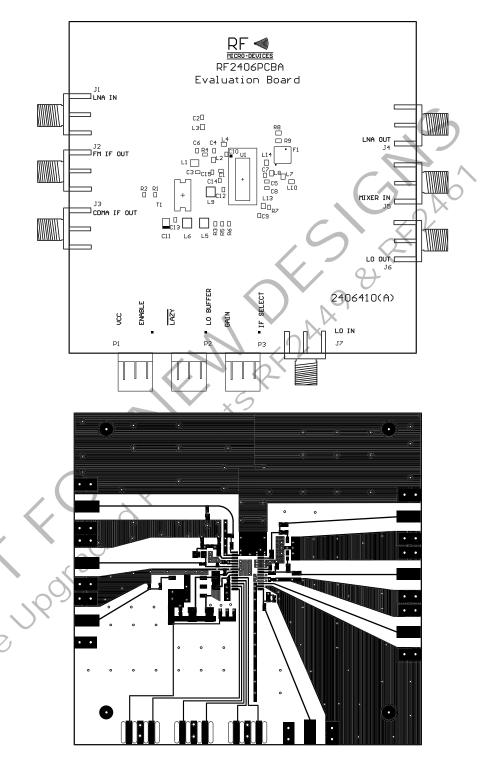
(Download Bill of Materials from www.rfmd.com.)

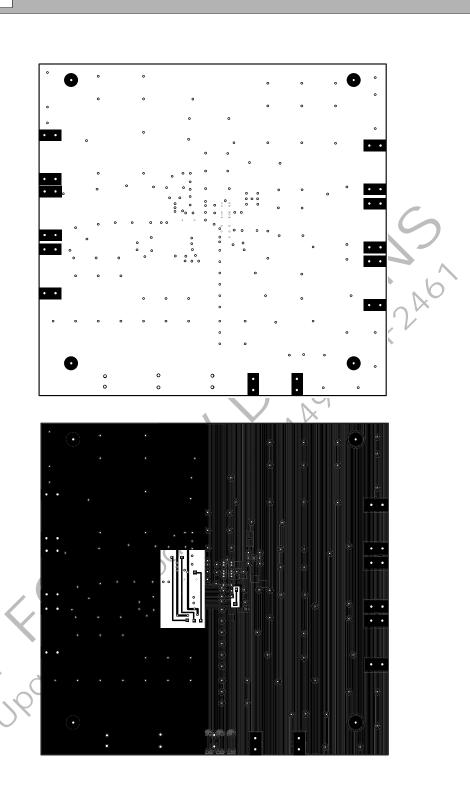


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# Evaluation Board Layout Board Size 3.088" x 2.948"

Board Thickness 0.056", Board Material FR-4, Multi-Layer





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