RF9901

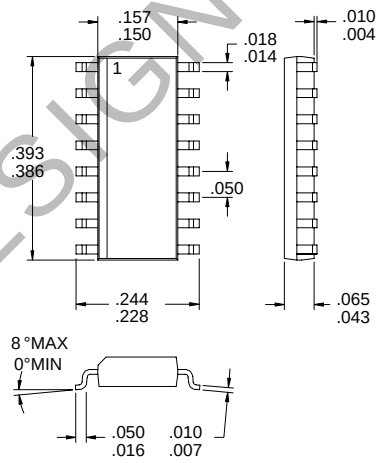
FSK TRANSMITTER

Typical Applications

- Hand-Held POS Terminals
- General Purpose 868MHz and 915MHz ISM Band Applications
- Digital Communication Systems
- Commercial and Consumer Products

Product Description

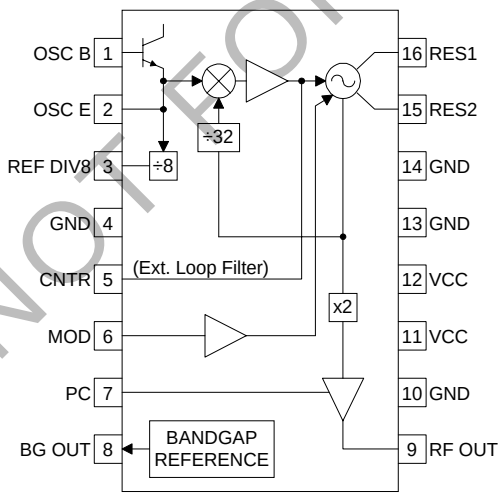
The RF9901 is a monolithic integrated circuit intended for use as a low-cost FSK transmitter. The unit is provided in 16-lead plastic packaging, and is designed to mate directly with the RF9902 FSK receiver. The two-chip set provides all functions necessary to implement a binary FSK transceiver for such applications as 868/915 MHz ISM-band hand-held terminals for POS, meter-reading, bar-code reading; as well as other digital applications such as SMR. The self-contained VCO and divide-by-32 circuitry simplify the system requirements, and the on-chip bandgap reference provides temperature stability and minimizes process variations. The part operates from a 3V to 5V supply, with no negative voltage required.



Package Style: SOP-16

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] Si Bi-CMOS
- [ ] GaAs HBT
- [ ] SiGe HBT
- [ ] GaAs MESFET
- [ ] Si CMOS



Functional Block Diagram

Features

- Single 3V to 5V Supply
- Direct Binary FSK Modulation
- On-Chip Divider for PLL
- Output Power up to +4dBm
- On-Chip VCO
- 400MHz to 930MHz Operation

Ordering Information

RF9901	FSK Transmitter
RF9901 PCBA	Fully Assembled Evaluation Board, 915MHz

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage V_{CC}	-0.5 to +7.5	V_{DC}
Input Modulation Level	V_{CC}	V
Output Load VSWR	50:1	
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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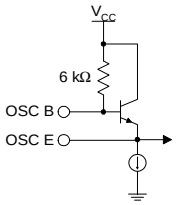
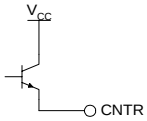
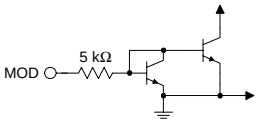
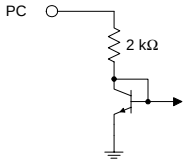
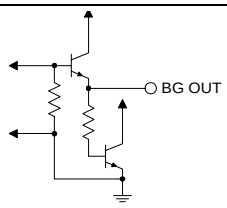
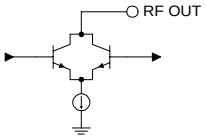
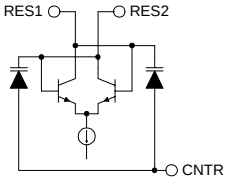
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=4.0V, V_{PC}=+3.5V, Freq=915MHz
Reference Frequency		F_C/64		Hz	Set by external crystal
PLL Lock Time			10	ms	
Modulation Type		Binary FSK			
Modulation Frequency		10 to 500		kHz	
Modulation Input Level	0		V_{CC}	V	
VCO Sensitivity		25		MHz/V	
Phase Detector Sensitivity		0.4		µA/°	
RF Output					
RF Output Frequency Range		400 to 930		MHz	
Output Power		0	+4	dBm	
Output Power in Off Mode			-10	dBm	
Output Impedance		2		kΩ	Open Collector Output
Harmonic Output			-30	dBc	
Other Spurious Components			-30	dBc	
Power Supply					
Voltage		3.0 to 5.0		V	
Current		30		mA	

Pin	Function	Description	Interface Schematic
1	OSC B	Oscillator base. The application schematic shows a typical Colpitts oscillator circuit. This pin may be driven by an external source. If so, it should be AC coupled using a capacitor. The level should be about 500mV$_{PP}$	
2	OSC E	Oscillator emitter. See pin 1 description.	See pin 1.
3	REF DIV8	Reference Oscillator Divide By Eight output. This output can be used as a reference frequency for other circuitry. Leave this pin unconnected if this signal is not used.	
4	GND	Ground. This pin should be connected to the ground plane as close to the package as possible. A recommended method is to put a via through to the backside ground plane either in the pad or connected to the pad to which the pin is soldered.	
5	CNTR	Loop filter. A series RC network to ground is needed to stabilize the loop. The smaller the capacitance, the higher the loop bandwidth will be. The lockup time specified is for a capacitor value of 50nF or less. The lockup time may be varied by changing these values. Note that loop lockup time is also a function of the VCO resonator setting. Fastest lock time results when the VCO resonator is set to resonate at just above F_O with the control voltage forced to V_{CC} / 2. The loop is a classical type 2 loop, consisting of a "lead" resistor and a capacitor, and the associated calculations can be used.	
6	MOD	Digital modulation input. The upper frequency limit of this input is 500kHz. The lower frequency limit is set by the loop filter. If the duty cycle of the input is 50%, then the frequency deviation at the output will be symmetric about the carrier frequency. Duty cycles of other than 50% will result in an asymmetric frequency deviation where the carrier frequency will not be centered between the two output frequencies. The amplitude of the modulation input sets the amount of frequency deviation. A larger amplitude results in a larger deviation. The modulation input is designed to be driven by a logic level (0V and V_{CC}). With no external resistor, the maximum modulation is > 500kHz. A series resistor is used to reduce the modulation (frequency deviation) to the desired amount. Note that the modulation is applied to an internal varactor in the VCO circuit causing the PLL to attempt to "correct" the deviation. It is therefore necessary to make the loop time constant sufficiently long (slow) so that this "correction" does not take place.	
7	PC	Power control input. When at 0V, the output amplifier is disabled. At positive voltages above 1V, the output power is turned on. The higher the voltage, the higher the power. If the full power supply voltage is to be connected to this pin, a series resistor of 1.5kΩ should be placed in series with the pin. Note that the sensitivity of this voltage was deliberately set so that maximum power could be obtained with a very low voltage.	
8	BG OUT	Bandgap reference voltage output. The output voltage is 1.1V. The maximum current drain is about 1mA. If a long lead is used to connect this pin, a series resistor should be used to prevent the lead from causing oscillation.	

Pin	Function	Description	Interface Schematic
9	RF OUT	Power amplifier output. There must be a DC connection to V_{CC}, typically through an RF choke. The recommended circuit is shown in the application schematic. It uses inductors to feed DC to the PA collector. The output frequency is the crystal frequency multiplied by 64. If the output is properly matched into 50Ω, then greater than +4dBm output power can be achieved. Output power is also dependent upon the operating frequency.	
10	GND	Ground. See pin 4 description.	
11	VCC	Power supply voltage input. This pin is used to supply the operating voltage. This pin should be bypassed to ground as close to the package as possible.	
12	VCC	Power supply voltage input. See pin 11 description.	
13	GND	Ground. See pin 4 description.	
14	GND	Ground. See pin 4 description.	
15	RES2	VCO resonator. There must be a DC path to V_{CC} on these pins. Chip inductors are recommended. The values of the inductors connected to pins 15 and 16 must also change depending on the required F_O. As the inductor values increase, the output frequency will decrease. At 915MHz, 18nH is recommended. At 450MHz, 56nH is recommended. The maximum DC voltage at the resonator pins is 4.5V. Therefore, a series resistor will improve the locking of the PLL depending upon the supply voltage. The resistor should be placed between V_{CC} and the choke inductor L3. A recommended resistor value at 5.0V is 500Ω. At 6.0V, the resistor value will increase to approximately 1kΩ.	
16	RES1	VCO resonator. See pin 15 description.	See pin 15.

RF9901 Evaluation Board Crystal Oscillator

Background

The RF9901 is an FSK transmitter that can be used to transmit FSK data using an RF carrier frequency in the range of 400MHz to 930MHz. This device is intended for and ideally suited to both European and United States ISM band applications.

The RF9901 evaluation board (RFMD Part Number RF9901PCBA) utilizes a Colpitts oscillator to generate the reference frequency for the PLL phase detector. The PLL consists of an integrated voltage controlled oscillator (VCO), a divide by 32 prescaler, and a reference frequency oscillator amplifier. The output carrier frequency is then the reference frequency multiplied by 64.

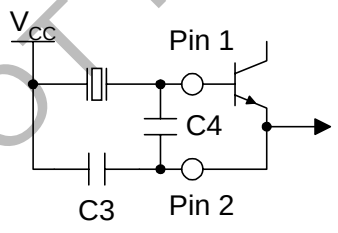
Which Topology?

The Colpitts oscillator is only one of many types of oscillators that could have been used and was chosen primarily for its low parts count. Other oscillators have various trade-offs for the designer which may result in choosing another oscillator type.

This article does not delve into oscillator design, but is simply to provide assistance in understanding why the particular crystal was chosen and what the general topology of the oscillator used on the evaluation board is. There are many references available to aid the designer who wishes to better understand the Colpitts oscillator and oscillator design in general.

Colpitts Topology

The basic topology of the Colpitts oscillator used is below:



The transistor is acting as an emitter-follower. The voltage gain is set by capacitors C3 and C4 which are acting as a tapped capacitive impedance transformer. The output power and frequency of the crystal oscillator can be optimized by adjusting C3 and C4. The frequency can be tuned by placing an adjustable inductor in series with the crystal.

What Type of Crystal?

After determining which type of oscillator was going to be used, a crystal needed to be chosen. The Colpitts crystal oscillator can use either a parallel or series resonant crystal. Examples of oscillators using each type of crystal would be fundamental mode and third overtone, respectively.

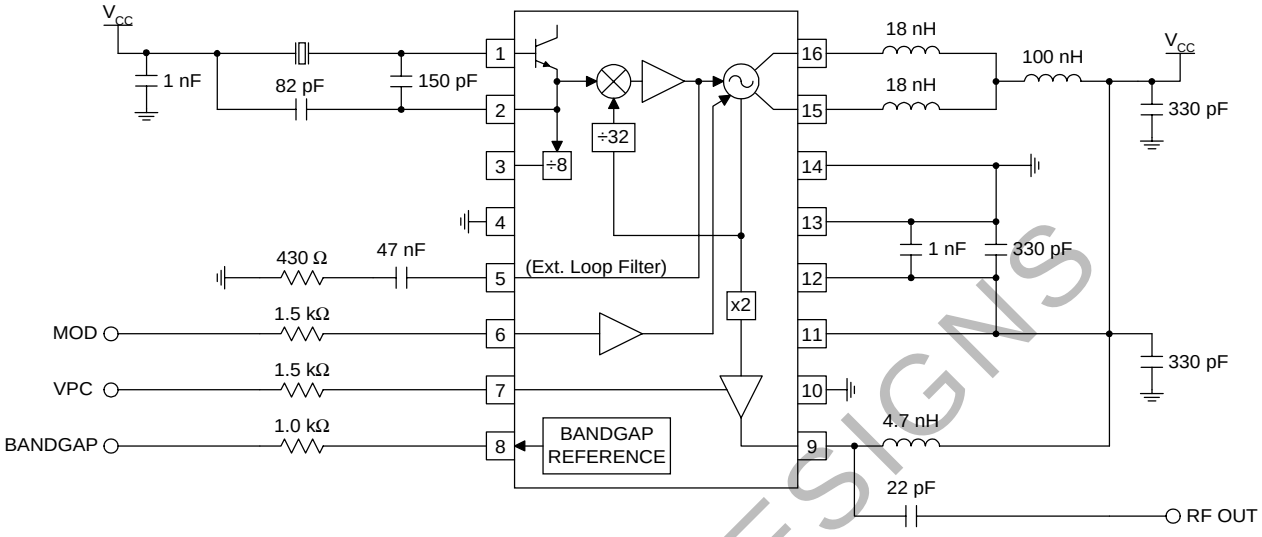
For our application, since we are using a fundamental mode common-emitter Colpitts oscillator, a parallel resonant crystal was chosen. For the RF9901 we wanted an RF output frequency of 916MHz, so we chose a crystal whose frequency is 14.31818MHz, resulting in an RF output frequency of 64x14.31818MHz=916.36MHz.

Which Crystal?

Specifically, a crystal manufactured by Epson America, Inc. which is available from Digi-Key, is used. It is a cylinder-type quartz crystal, type CA-301. The Epson part number is CA-301 14.31818M-C. This crystal has the following properties:

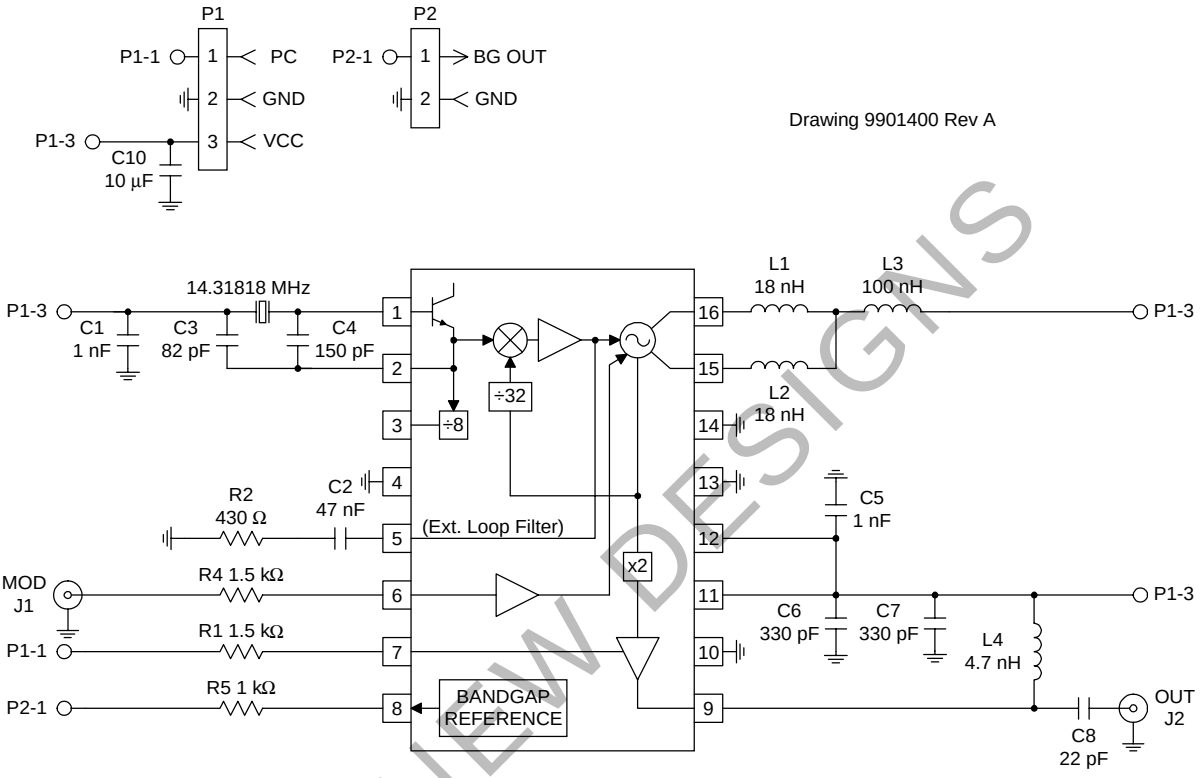
Specification	Value
Operating Temperature	-20°C to +70°C
Maximum Drive Level	2mW Max
Recommended Level	10mW to 100mW
Frequency Tolerance	±30ppm
Load Capacitance	18pF
Series Resistance	50Ω Max

Application Schematic



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Component values for 916 MHz output frequency (F0). The output frequency is related to the crystal frequency (Fref) by F0 = Fref x 64. L1 and L2 must also change depending on the required F0.

Evaluation Board Layout