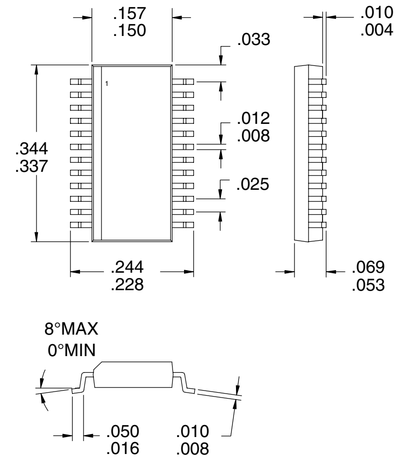
INTEGRATED SPREAD SPECTRUM RECEIVER

Typical Applications

- Spread Spectrum Systems
- Dual-IF Strip for PCS and 2.4 GHz ISM Band Receivers
- Dual Mode Digital/Analog Receivers
- POS Terminals
- Commercial Handheld Systems

Product Description

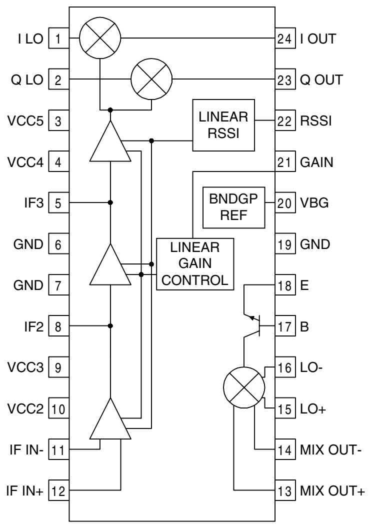
The RF2903 spread spectrum receiver IC includes an RF front-end with an RF pre-amp and mixer, a variable-gain IF section with RSSI, and a demodulator section. The front-end can accept inputs from 150MHz to 1000MHz and is suitable for ISM band receivers and the first IF stage in superheterodyne receivers. The IF amplifier provides up to 90dB of gain up to 200MHz, controlled with an analog voltage. A Received Signal Strength Indicator (RSSI) is present for power level detection. Two double-balanced mixers are provided which may be configured for quadrature demodulation, FM/FSK discrimination, or AM detection. AM detection is accomplished with an external detector circuit. An internal band-gap reference maintains consistent performance over temperature and power supply voltage.



Package Style: SSOP-24

Optimum Technology Matching® Applied

- [x] Si BJT
- [ ] GaAs HBT
- [ ] GaAs MESFET
- [ ] Si Bi-CMOS
- [ ] SiGe HBT
- [ ] Si CMOS



Functional Block Diagram

Features

- 3V to 6V Operation
- FM, PM, or Quadrature Demodulation
- Linear Analog Gain Control and RSSI
- DC to 50MHz I/Q Frequency
- 10 to 200MHz IF, 150 to 1000MHz RF
- Stable Biasing Via Band-Gap Reference

Ordering Information

RF2903	Integrated Spread Spectrum Receiver
RF2903 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.5	V_{DC}
Input RF Level	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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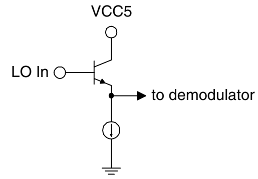
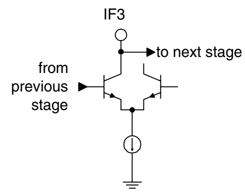
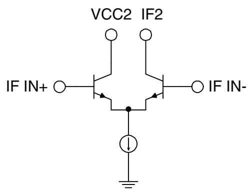
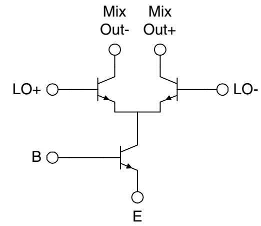
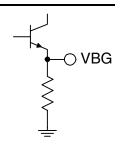
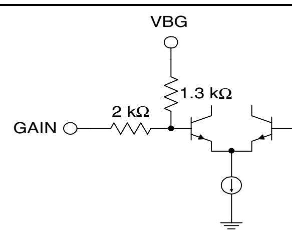
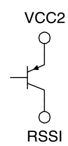
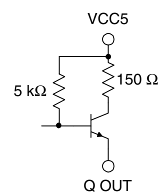
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=5V, RF=350MHz, L01=400MHz, LO2=55MHz
Conversion Gain	87	90	100	dB	RF=350MHz
		84		dB	RF=900MHz
Input IP_3		-10		dBm	Common emitter configuration
Input IP_3		0		dBm	Common base configuration
Cascade Noise Figure		5		dB	RF=300MHz, CE configuration
		14		dB	RF=900MHz, CE configuration
Input Section					
Frequency Range		150 to 1000		MHz	
Conversion Gain		11		dB	RF=350MHz
		5		dB	RF=900MHz
Noise Figure		4		dB	RF=350MHz
		13.5		dB	RF=900MHz
Input VSWR		2:1			
First LO					
Frequency Range		10 to 1200		MHz	
Input Level		0		dBm	Driven single-ended, resistively matched
LO Input Impedance	set by external components			Ω	
IF Section					
Frequency Range		10 to 200		MHz	
Input Impedance		>5 || <2pF		kΩ	
Noise Figure		10		dB	50MHz, 500Ω source impedance, max gain
Input IP3		+3		dBm	50MHz, minimum gain
Gain Range		0 to 79		dB	Driven single-ended
Gain Control Voltage Range		0.6 to 1.6		V	
Gain Control Speed		100		ns	Minimum gain to maximum gain
RSSI DC Output Range		0.6 to 2		V	
RSSI Input Resolvable Range		80		dB	
RSSI Sensitivity		20		mV/dB	
RSSI Linearity		±3		dB	
I/Q Demodulator					
LO Input Level		0		dBm	Resistively matched
LO Input Impedance	set by external components			Ω	
Output Frequency Range		DC to 90		MHz	
Saturated Output Voltage		1.5		V_{PP}	
Amplitude Balance		0.2	1.0	dB	This performance will also be affected by the accuracy of the external phase shift network.
Phase Error		1		°	This performance will also be greatly affected by the accuracy of the external phase shift network.
DC Offset		20		mV	Between I and Q
Power Supply					
Voltage		5		V	Specifications
		3 to 6		V	Operating limits
Band-Gap Reference Voltage	1.58	1.63	1.68	V	
Current	15	23	25	mA	V_{CC}=5.0V

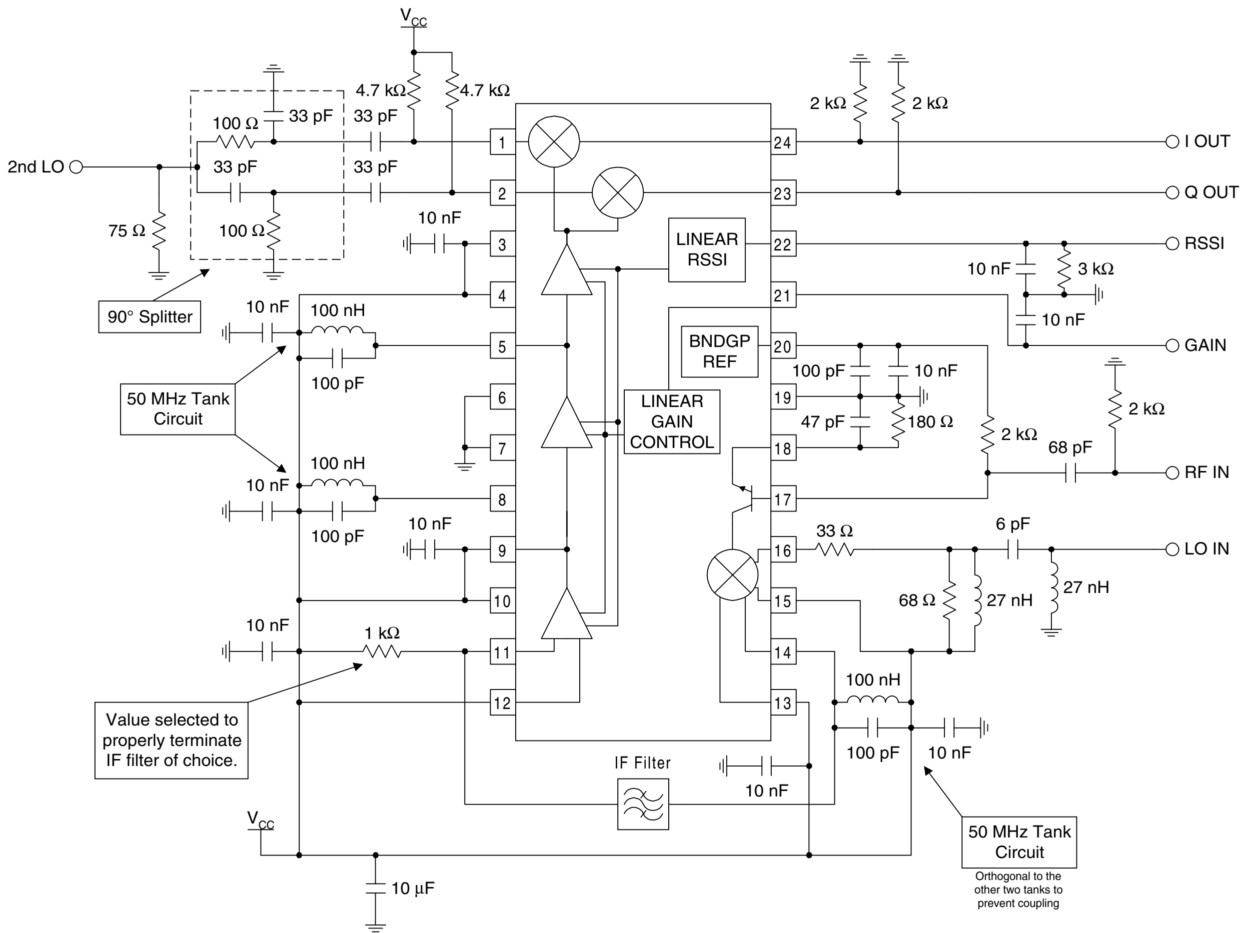
Pin	Function	Description	Interface Schematic
1	I LO	I-Channel demodulation mixer LO input (High Impedance). This pin is NOT internally DC blocked. This pin must be connected to V_{CC} through a matching inductor or resistor (see the application schematic). An external blocking capacitor should be supplied if a DC voltage, other than V_{CC}, is present on the device driving this input. In order to cause this mixer to operate in a "pass through" mode (no mixing), this pin is DC biased with an external resistor divider that applies a voltage at least 1.4V below V_{CC}, and then I OUT (pin 24) will be the same signal as is present at the IF3 amplifier output.	
2	Q LO	Q Channel demodulation mixer LO input (High Impedance). This pin is NOT internally DC blocked. This pin must be connected to V_{CC} through a matching inductor or resistor (see the application schematic). Otherwise, an external blocking capacitor should be supplied if a DC voltage, other than V_{CC}, is present on the device driving this input. In order to cause this mixer to operate in a "pass through" mode (no mixing), this pin may be connected to ground, and Q OUT (pin 23) will be the same signal as is present at the IF3 amplifier output.	See pin 1.
3	VCC5	Voltage supply for the I and Q demodulation mixers. This pin should be well bypassed at IF and Baseband frequencies.	
4	VCC4	Voltage supply for the IF3 amplifier stage. This pin should be well bypassed at IF frequencies.	
5	IF3	IF2 Output/ IF3 Input pin. This pin must be connected to V_{CC} through an inductor to provide DC bias for IF2's output and IF3's input. The inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit. A resistor may be placed in parallel with the tank circuit in order to adjust the tank's bandwidth, but the net gain of the device may be reduced if the value of the resistor is too small.	
6	GND	Ground connection. Keep traces physically short and connect immediately to ground plane for best performance.	
7	GND	Same as pin 6.	
8	IF2	IF1 Output/ IF2 Input pin. This pin must be connected to V_{CC} through an inductor to provide DC bias for IF1's output and IF2's input. The inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit. A resistor may be placed in parallel with the tank circuit in order to adjust the tank's bandwidth, but the net gain of the device may be reduced if the value of the resistor is too small.	See pin 5.
9	VCC3	Voltage supply for the IF2 amplifier stage. This pin should be well bypassed at IF frequencies. Pins 9 and 10 can share common bypass capacitors.	
10	VCC2	Voltage supply for the IF1 amplifier stage. This pin should be well bypassed at IF frequencies. Pins 9 and 10 can share common bypass capacitors.	
11	IF IN-	IF1 Amplifier differential input (High Impedance). This pin must be connected to V_{CC} through an inductor to provide DC bias to IF1's input. If an IF filter is not used before this input, then a single inductor may be used to bias pins 11 and 14, and the inductance at this pin should be parallel resonated with a capacitor in order to form a noise band-limiting tank circuit (see the application circuit). For single-ended input operation, the unused balanced input pin must be connected to V_{CC} and well bypassed at the IF frequency.	
12	IF IN+	Same as pin 11, except complementary input.	See pin 11.

Pin	Function	Description	Interface Schematic
13	MIX OUT+	RF mixer output. Pins 13 and 14 are open-collector, complementary outputs. This pin must be connected to V_{CC} through an inductor to provide DC bias for the mixer. If operating in the single-ended mode, either output may be used, but both must be DC connected to V_{CC}. The unused output should be bypassed at LO and IF frequencies. Keep in mind that for single-ended operation, the mixer's gain is 6dB lower (1/2 of the output voltage is not used).	
14	MIX OUT-	Same as pin 13, except complementary output.	See pin 13.
15	LO+	RF Mixer LO differential input (High Impedance). This pin must be connected to V_{CC} through an inductor or a resistor to provide DC bias for the mixer. If operating in the single-ended mode, either LO input may be used, but both must be DC connected to V_{CC}. The unused input should be bypassed at RF, LO, and IF frequencies.	See pin 13.
16	LO-	Same as pin 15, except complementary input.	See pin 13.
17	B	RF input pin (High Impedance). This is the base of an RF transistor used as a pre-amplifier. This pin must be properly biased. In most applications, biasing is accomplished by resistively connecting this pin to the band-gap reference at pin 20 though a ~2kΩ resistor.	See pin 13.
18	E	Emitter of the RF transistor. This pin should be AC coupled to ground with a RF bypass capacitor. In most applications, a 180Ω resistor to ground is used for the appropriate biasing and DC feedback level.	See pin 13.
19	GND	Same as pin 6.	
20	BG OUT	Band Gap voltage reference output. This voltage output (1.6V) is held constant over variations in supply voltage and operating temperature and may be used as a reference for other external circuitry. This pin should not be loaded such that the sourced current exceeds 1mA. This pin should be well bypassed.	
21	GC	Analog gain control pin. The DC voltage applied to this pin determines the gain of all three IF amplifiers. Minimum gain occurs when 0V is applied. Maximum gain occurs when approximately 2.5V is applied (for V_{CC}=5V).	
22	RSSI	Received Signal Strength Indicator. The DC voltage at this pin is proportional to the level of signal (in dB) present in all three IF amplifiers. A capacitor should be placed on this pin to eliminate ripple. A resistor is required to generate the RSSI voltage.	
23	Q OUT	Q Channel demodulation mixer Baseband output. This is an emitter-follower output with an open emitter. DC resistance to ground must be provided by the load. If the load has DC present, a series DC blocking capacitor and a shunt loading resistor must be provided. The single-ended output impedance is ~50Ω. These outputs are designed, however, to drive high impedance loads, and the total voltage gain of the part will be higher for larger values of a loading resistor.	

Pin	Function	Description	Interface Schematic
24	I OUT	I Channel demodulation mixer Baseband output. This is an emitter-follower output with an open emitter. DC resistance to ground must be provided by the load. If the load has DC present, a series DC blocking capacitor and a shunt loading resistor must be provided. The single-ended output impedance is ~50Ω. These outputs are designed, however, to drive high impedance loads, and the total voltage gain of the part will be higher for larger values of a loading resistor.	See pin 23.

Application Schematic

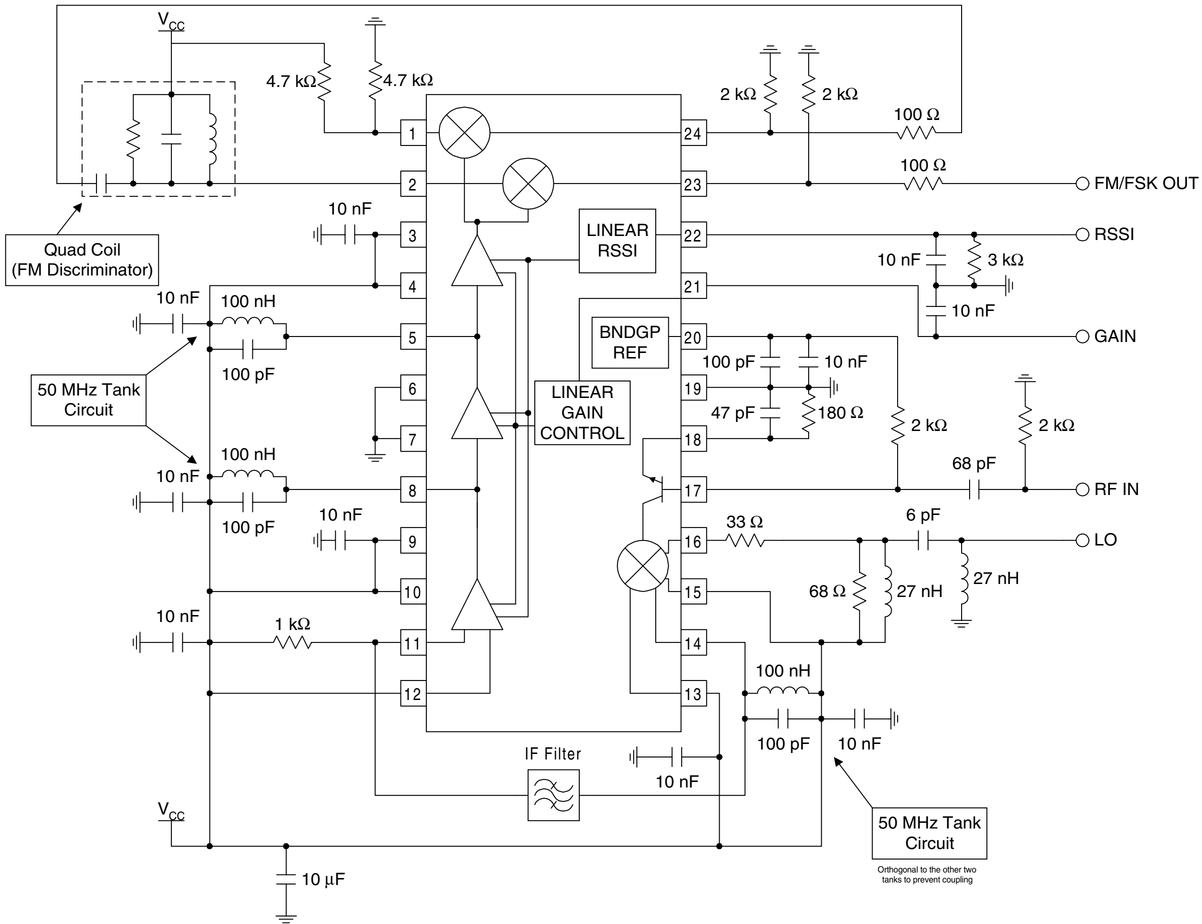
Quadrature Demodulation
900 MHz RF and 50 MHz IF Operation



Application Schematic

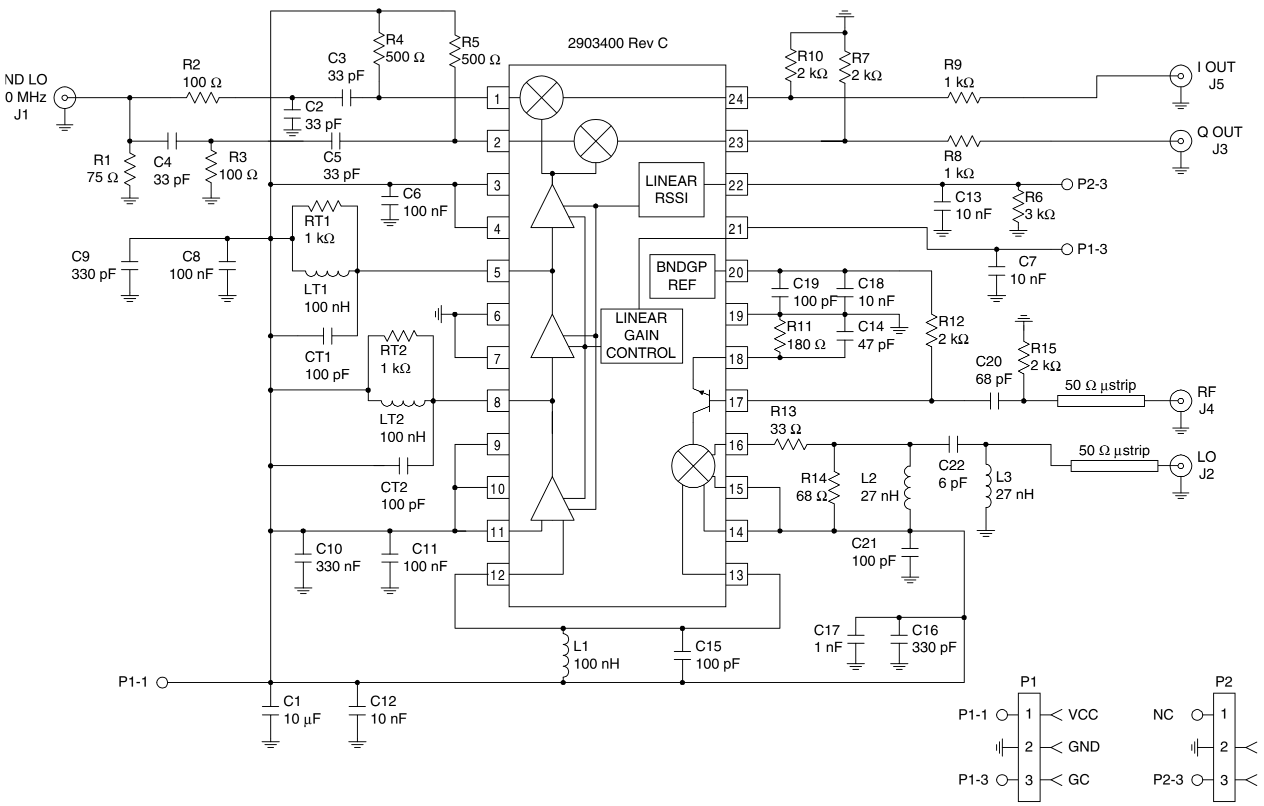
FM/FSK Demodulation

900MHz RF and 50MHz IF Operation



Evaluation Board Schematic

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout

Scale 1:1, Board size 2” x 3”

Board Thickness 0.031”; Board Material FR-4