# 960JX Embedded 32-Bit RISC Processor

## Features

- Functionally equivalent to *Intel*'s 80960JA/JF embedded 32-bit microprocessor
- High-performance embedded architecture
- High-speed interrupt controller
- Two on-chip timers
- Two-way set associative instruction cache
- Direct mapped data cache
- On-chip stack frame cache
- On-chip data RAM
- High bandwidth burst bus
- Halt mode for low-power operation
- *IEEE* 1149.1 (JTAG) boundary-scan compatibility
- Samples available for system emulation:
- 132-pin, plastic, bumpered quad flat pack (BQFP)

## Description

The 960JX provides high performance to low-cost 32-bit embedded applications. The 960JX features a generous instruction cache, data cache, and data RAM. It also has a fast interrupt mechanism, dual programmable timer units, and new instructions.

The processor combines two important peripherals: a timer unit and an interrupt controller. These and other hardware resources are programmed through memory-mapped control registers.

The timer unit offers two independent 32-bit timers for use as real-time system clocks and general-purpose system timing. These operate in either single-shot or auto-reload mode and can generate interrupts.

The interrupt controller unit (ICU) has a flexible, low-latency means for processing and handling interrupts. The ICU provides full programmability of up to 240 interrupt sources into 31 priority levels and takes advantage of a cached priority table and optional routine caching to minimize interrupt latency. The ICU, independent from the core, compares the priorities of posted interrupts with the current process priority. The ICU also supports the integrated timer interrupts.

When using memory subsystems for low-cost embedded applications, substantial wait-state penalties are often required. The 960JX integrates considerable storage resources on-chip to decouple CPU execution from the external bus.

Both the instruction cache and data cache included in the 960JX can be configured for different sizes. For details, please refer to Figure 40 on the next page.

The 32-bit multiplexed burst bus provides a high-speed interface to system memory and I/O. A full complement of control signals makes the connection of the 960JX to external components easier. The user programs physical and logical memory attributes through memory-mapped control registers (MMRs). Physical and logical configuration registers enable the processor to operate with multiple combinations of bus width and byte ordering. The processor supports a homogeneous byte ordering model.

A halt mode is included to support applications where low power consumption is critical. The halt instruction enables the shutdown of instruction execution, which results in a power savings of up to 90%.

The 960JX's testability features, which include *ONCE** (on-circuit emulation) mode and boundary scan (JTAG), provide a powerful environment for design debug and fault diagnosis.

Figure 40 shows the main blocks of the 960JX.

* *ONCE* is a trademark of Intel Corporation.

## 960JX Embedded 32-Bit RISC Processor (continued)

### Description (continued)

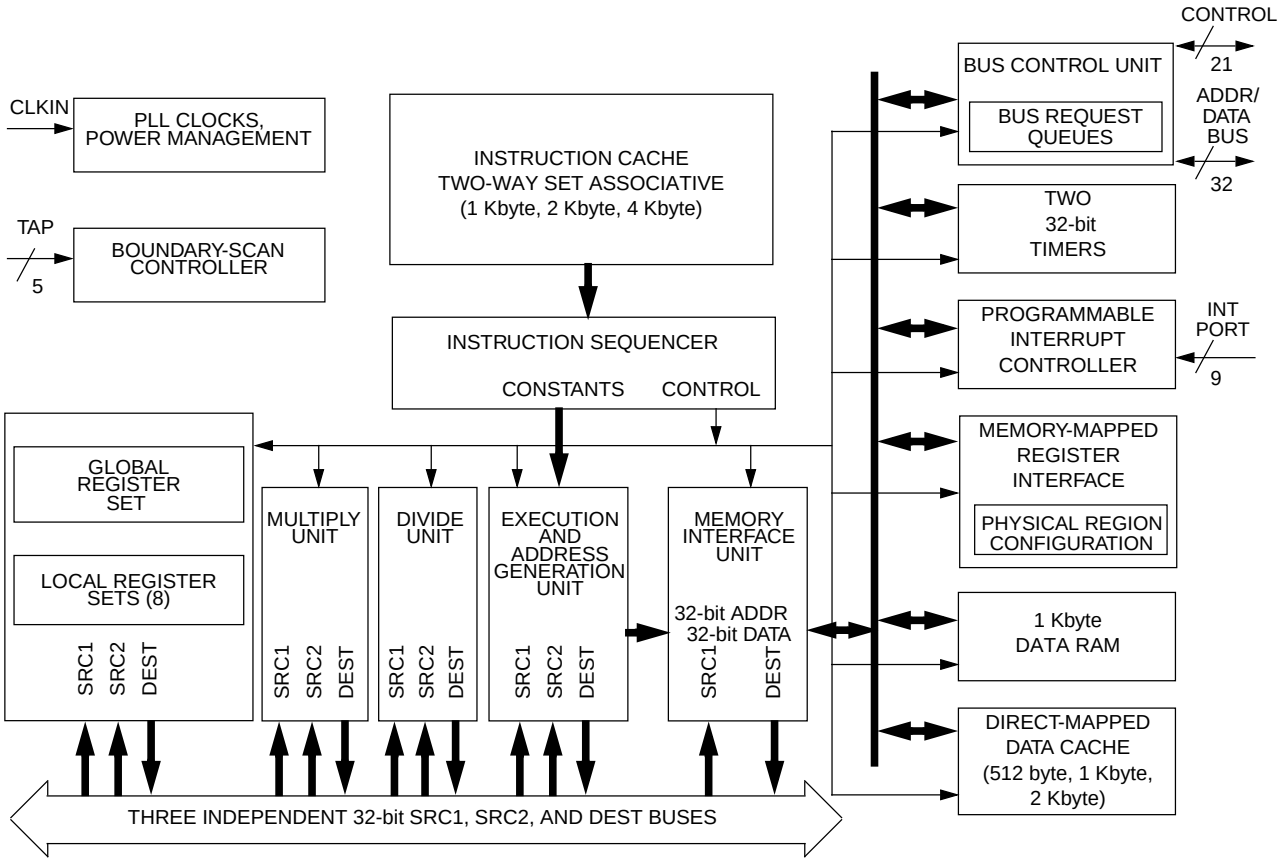


**Figure 40. 960JX Embedded 32-Bit RISC Processor Block Diagram**