# *Advance Information*

## 68K RISC Embedded 32-Bit RISC Microprocessor

### Features

- Functionally equivalent to *Motorola's ColdFire** (MCF5202/03)
- Variable-length RISC code density (requires less memory and slower memory)
- Dynamic bus sizing (32-, 16-, and 8-bit bus support)
- High-performance, nonblocking, on-chip unified cache:
  — Four-way set associative
  — 2 Kbyte size
- Optimized for high-level language constructs
- Designed to minimize die size
- 16 user-visible 32-bit wide registers
- Supervisor/user modes for system protection
- Vector base register to relocate exception-vector table
- Debug module including background debug and real-time debug support
- Low interrupt latency accelerates responsiveness in real-time applications
- Low-power consumption due to full-static design logic
- 3-state pin
- Single bus clock output
- Compliance with JTAG *IEEE* 1149.1
- Fully supported industry-leading third-party tools developers
- Samples available for system evaluation:
  — 100-pin TQFP

### Description

The 68K RISC has been optimized for embedded processing applications. It is based on the concept of variable-length RISC technology and combines the architectural simplicity of the 32-bit RISC with a memory-saving, variable-length instruction set.

By using a variable length instruction set architecture, the 68K RISC processor offers designers substantial system-level advantage over conventional fixed-length RISC architectures. Since the 68K RISC has a dense binary code, less valuable memory is occupied than for a fixed-length instruction set RISC processor. This greater code density results in systems that require less memory per application, and it enables the use of slower and less costly memory while still attaining a given performance level.

***** *ColdFire* is a trademark of Motorola, Inc.

## 68K RISC Embedded 32-Bit RISC Microprocessor (continued)

### Description (continued)

The 68K RISC is available in a 100-pin thin quad flat pack package with the pinout shown in Figure 38.

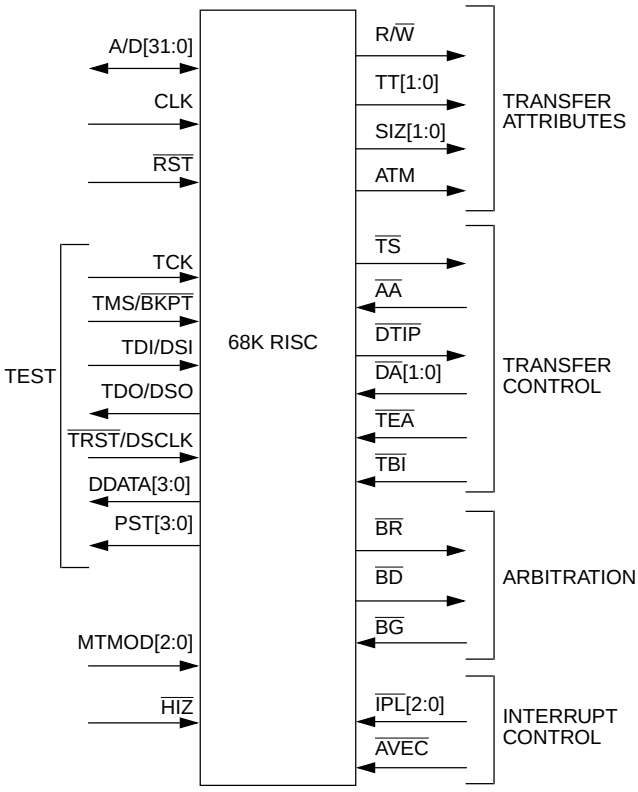


**Figure 38. 68K RISC Pinout**

## Signal Information

#### Netlist Order

Inputs: CLK, RST, TCK, TMS/BKPT, TDI/DSI, TRST/DSCLK, MTMOD[2:0], HIZ, AA, DA[1:0], TEA, TBI, BG, IPL[2:0], AVEC

Outputs: TDO/DSO, DDATA[3:0], PST[3:0], R/W, TT[1:0], SIZ[1:0], ATM, TS, DTIP, BR, BD

IOputs: A/D[31:0]

## Functional Description

The 68K RISC is composed of five main blocks: 2 Kbyte unified cache, processor core, bus controller, debug module, and JTAG interface. Figure 39 is a block diagram of the 68K RISC. The following paragraph provides a description of the JTAG interface.

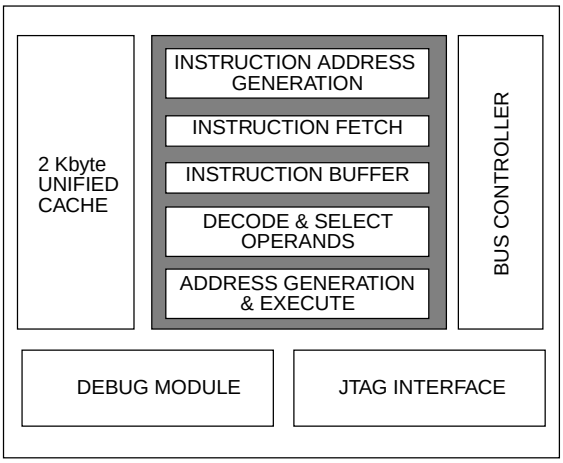


**Figure 39. 68K RISC Block Diagram**

## JTAG Interface

To help with system diagnostics and manufacturing testing, the 68K RISC includes dedicated user-accessible test logic that complies with the *IEEE* 1149.1 standard for boundary-scan testability, often referred to as joint test action group (JTAG). For more information, refer to the *IEEE* 1149.1 standard.