RC5601

1.5V Output Step-Down DC-DC Converter

Features

- Fixed 1.5V output from 5V supply
- 80% efficiency
- Excellent transient response
- Continuous short circuit protection
- Oscillator frequency adjustable from 200KHz to 1MHz
- Precision trimmed low TC voltage reference
- Soft start control during power-up
- Drives P-channel MOSFETs
- 8 pin SOIC package

Applications

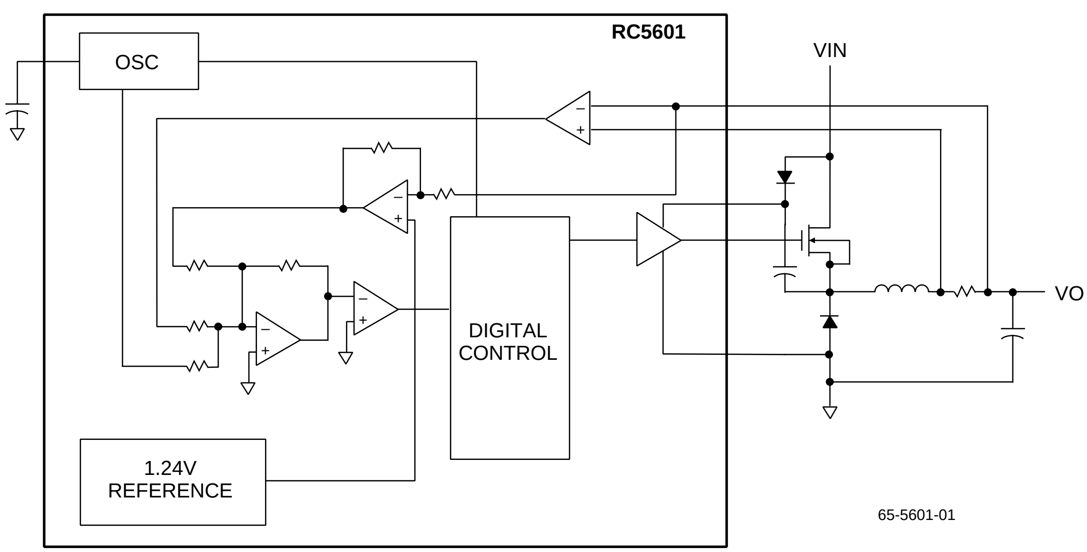
- Pentium® Pro power supply for GTL+ bus termination
- High efficiency 1.5V power supply

Description

The RC5601 is a step-down DC-DC controller for a 1.5V output from either a 5V or a 3.3V supply. Using the appropriate application circuitry, it can be configured to deliver load currents greater than 6A. The RC5601 is designed to operate in a standard PWM control mode under heavy load conditions and in PFM control mode while supplying light loads for optimal efficiency. An on-chip precision low TC voltage reference eliminates the requirement for external components in order to achieve tight voltage regulation. The internal oscillator can be programmed to operate over a range of 200KHz to 1MHz using an external capacitor in order to allow flexibility in choosing external components.

Preliminary Information

Block Diagram



Rev. 0.9.1

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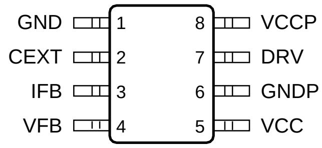
Preliminary Information

Pin Assignments



65-5601-02

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Ground
2	CEXT	External capacitor for setting oscillator frequency
3	IFB	Current Feedback Input
4	VFB	Voltage Feedback Input
5	VCC	Analog VCC; Nominally 5V
6	GNDP	Power ground for high current driver
7	DRV	FET driver output
8	VCCP	FET driver supply voltage; Nominally 12V

Absolute Maximum Ratings

Analog supply voltage, VCC	13V
FET driver supply voltage, VCCP	13V
Junction Temperature	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Short Circuit Duration	Continuous

Note:

1. Functional operation under any of these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Analog Supply Voltage, VCC		4.5	5	7	V
FET driver supply voltage, VCCP		9	12	13	V
Ambient Temperature, T_A		0		70	°C

DC Electrical Specifications

(VCC = 5V, f_{osc} = 650 KHz, and T_A = +25°C using circuit in Figure 1, unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Voltage	T_A = 0–70°C		1.5		V
Output Current			5.5		A
Setpoint Accuracy	I_{LOAD} = 3A		3	5	%
Output Temperature Drift	T_A = 0–70°C		+40		ppm/°C
Load Regulation	I_{LOAD} = 0.5 to 5.5A		0.5		%Vo
Line Regulation	V_{IN} = 4.75- 5.25V, I_{LOAD} = 3A		0.07		%Vo
Output Ripple/Noise	20MHz BW, I_{LOAD} = 5.5A		30		mV
Cumulative Accuracy[1]	T_A = 0–70°C		8	10	%
Efficiency	I_{LOAD} > 4A		80		%
Short Circuit Detect Threshold	Internal comparator offset	100	120	140	mV
Output Current Driver	Open Loop	0.5	0.7		A
Power Dissipation	No external components		0.1		W
Thermal Impedance, θ_{JA}			85		°C/W

Note:

1. Cumulative Accuracy is determined by Setpoint Accuracy, Line and Load Regulation, Output Ripple/Noise, Transient Performance and Temperature Drift.

AC Electrical Specifications[1]

(V_{CC} = 5V, T_A = +25°C using circuit in Figure 1, unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units
Response Time Sleep-to-Full Load, I_{LOAD} = 0.5A to 5.5A		10		µs
Oscillator Frequency Range	0.2		1	MHz
Oscillator Frequency Precision (excluding tolerance of C_{EXT})		10		%
Maximum Duty Cycle in PWM Mode	90	95		%
Minimum Duty Cycle in PFM Mode			100	ns
Response Time to Short Circuit Condition		15	30	ns
Soft Start duration at Power-Up and Power-Down		1		ms

Note:

1. Guaranteed by characterization, not tested 100%.

Preliminary Information

Preliminary Information

Test Circuit

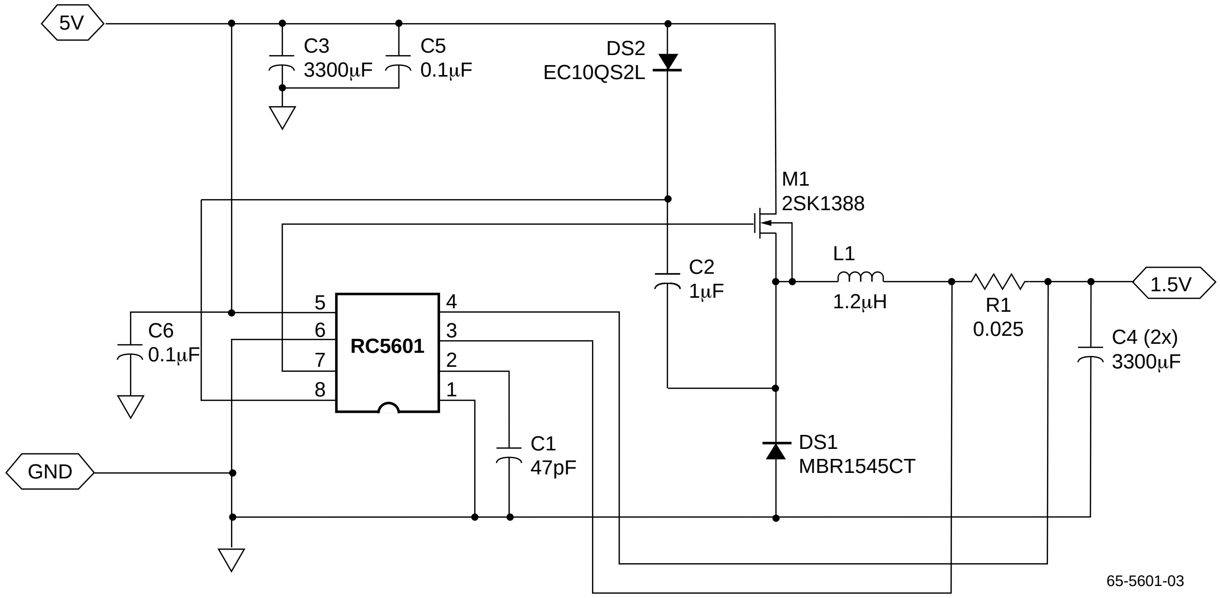


Figure 1. RC5601 Standard Test or Application Schematic for 5.5A, 1.5V Load

Table 1. Components for RC5601

RC5601 Standard Application Circuit Bill of Materials			
Ref Designator	**Quantity**	**Part No.**	**Manufacturer**
L1	1	CDRH127-1R2NC 1.2µH	Inductor, Sumida
M1	1	2SK1388	MOSFET, Fuji
DS1	1	MBR1545CT	Schottky Diode, Motorola 10A
DS2	1	EC10QS02L	Schottky Diode, Nihon
C1	1	47pF	SMD Cap
C2	1	1µF	SMD Ceramic
C5, C6	2	0.1µF	SMD Cap
C3, C4	3	6MV3300CG	Sanyo 3300 µF, 6.3V
R1	1	0.025Ω	MnCu Jumper

Applications Discussion

Standard Application Circuit

The application circuit shown in Figure 1 represents an optimized step down regulator using the RC5601 to power the GTL+ bus for a Pentium Pro processor application. Some users may want to develop their own DC-DC converter solution that is uniquely tailored to a specific application requirement. In that case, the user should review the detailed information contained within the Design Procedure and Applications Information section.

Detailed Description

The RC5601 is a step-down DC-DC controller. When designed around the appropriate external components, it can be configured to deliver more than 6A of output current. During heavy loading conditions, the RC5601 functions as a current-mode PWM step down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation), or pulse skipping mode. The controller will sense the load level and switch between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

Main Control Loop

The main control loop of the regulator contains two main sections; the analog control block and the digital control block. The analog block consists of signal conditioning amplifiers feeding into a set of comparators which provide the inputs to the digital block. The signal conditioning section accepts inputs from the IFB (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The voltage control path amplifies the VFB signal and presents the output to one of the summing amplifier inputs. The current control path takes the difference between the IFB and VFB pins and presents the resulting signal to another input of the summing amplifier. These two signals are then summed together with the slope compensation input from the oscillator. This output is then presented to a comparator, which provides the main PWM control signal to the digital control block.

The additional comparators in the analog control section set the thresholds of where the RC5601 enters its pulse skipping mode during light loads as well as the point at which the max current comparator disables the output drive signal to the external power MOSFET.

The digital control block is designed to take the comparator inputs along with the main clock signal from the oscillator and provide the appropriate pulses to the DRV output pin that controls the external power MOSFET. The digital section was designed utilizing high speed schottky transistor logic, thus allowing the RC5601 to operate at clock speeds as high as 1MHz.

High Current Output Drivers

The RC5601 contains a high current output driver which utilizes high speed bipolar transistors arranged in a push-pull configuration. The driver is capable of delivering 1A of current in less than 100ns. The power and ground connections are separated from the overall chip power and ground for additional switching noise immunity. The DRV driver has a power supply, VCCP, which is boot-strapped from a flying capacitor as illustrated in Figure 1. Using this configuration, C2 is alternately charged from VCC via the schottky diode DS2 and then boosted up when the FET is turned on. This scheme provides a VCCP voltage equal to 2•VCC – V_{DS}(DS2), or approximately 9.5V with VCC = 5V. This voltage is sufficient to provide the 9V gate drive to the external MOSFET required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the RC5601 is a precision 1.24V band-gap voltage reference. The internal resistors are precisely trimmed to provide a very low temperature coefficient (TC).

Oscillator

The RC5601 oscillator section is implemented using a fixed current capacitor charging configuration. An external capacitor (C_{EXT}) is used to preset the oscillator frequency between 200KHz and 1MHz. This scheme allows maximimum flexibility in setting the switching frequency as well as choosing external components.

In general, a lower operating frequency will increase the peak ripple current flowing in the output inductor and thus require the use of a larger inductor value. Operation at lower frequencies also increases the amount of energy storage that must be provided by the bulk output capacitors during load transients due to the slower loop response of the controller.

The user should note that the efficiency losses due to switching are relatively fixed per switching cycle. Therefore as the switching frequency is increased, so is the contribution towards efficiency due to switching losses.

Careful analysis of the RC5601 DC-DC controller has resulted in an optimal operating frequency of 650KHz, which allows the use of smaller inductive and capacitive components while maximizing peak efficiency under all operating conditions.

Preliminary Information

Preliminary Information

Design Procedure and Applications Information

Simple Step-Down Converter

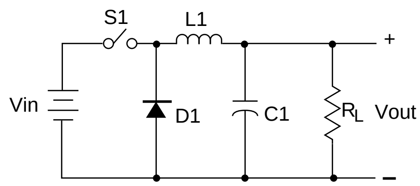


Figure 2. Simple Buck DC-DC Converter

Figure 1 illustrates a step-down DC-DC converter with no feedback control. The derivation of the basic step-down converter will serve as a basis for the design equations for the RC5601. Referring to Figure 2, the basic operation begins by closing the switch S1. When S1 is closed, the input voltage V_{IN} is impressed across inductor L1. The current flowing in this inductor is given by the following equation:

$$I_L = \frac{(V_{IN} - V_{OUT})T_{ON}}{L1}$$

where T_{ON} is the duty cycle (the time when S1 is closed).

When S1 opens, the diode D1 will conduct the inductor current and the output current will be delivered to the load according to the equation:

$$I_L = \frac{V_{OUT}(T_S - T_{ON})}{L1}$$

where: T_S is the overall switching period.
$(T_S – T_{ON})$ is the time during which S1 is open.

By solving these two equations, we can arrive at the basic relationship for the output voltage of a step-down converter:

$$V_{OUT} = V_{IN}\left(\frac{T_{ON}}{T_S}\right)$$

In order to obtain a more accurate approximation for V_{OUT}, we must also include the forward voltage V_D across diode D1 and the switching loss, Vsw. After taking into account these factors, the new relationship becomes:

$$V_{OUT} = (V_{IN} + V_D - V_{SW})\frac{T_{ON}}{T_S} - V_D$$

Selecting the Inductor

The inductor is one of the most critical components to be selected in the DC-DC converter application.. The critical parameters are inductance (L), maximum DC current (Io) and the coil resistance (R1). The inductor core material is a crucial factor in determining the amount of current the inductor will be able to withstand. As with all engineering designs, tradeoffs exist between various types of core materials. In general, Ferrites are popular due to their low cost, low EMI properties and high frequency (>500KHz) characteristics. Molypermalloy powder (MPP) materials exhibit good saturation characteristics, low EMI and low hysteresis losses; however, they tend to be expensive and more effectively utilized at operating frequencies below 400KHz. Another critical parameter is the DC winding resistance of the inductor. This value should typically be reduced as much as possible, as the power loss in the DC resistance will degrade the efficiency of the converter by the relationship: $P_{LOSS} = I_O^2$ x R1. The value of the inductor is a function of the oscillator duty cycle (T_{ON}) and the maximum inductor current (I_{PK}). I_{PK} can be calculated from the relationship:

$$I_{PK} = I_{MIN} + \left(\frac{V_{IN} - V_{SW} - V_D}{L}\right)T_{ON}$$

Where T_{ON} is the maximum duty cycle and V_D is the forward voltage of diode DS1.

Then the inductor value can be calculated using the relationship:

$$L = \left(\frac{V_{IN} - V_{SW} - V_O}{I_{PK} - I_{MIN}}\right)T_{ON}$$

Where V_{SW} (R_{DSON} x I_O) is the drain-to-source voltage of M1 when it is switched on.

Current-Sense Resistor

The current sense resistor will be required to carry the same peak current as the inductor L1. As a result, the sense current should be set at a level greater than the maximum load current I_{MAX}. The RC5601 will begin to limit the output current to the load by turning off the FET driver when the voltage across the sense resistor exceeds 100mV. When this occurs, the output voltage will temporarily lose its regulation. As the voltage across the resistor increases, the FET will continue to turn off until the current limit value is reached and the RC5601 will continuously deliver the limit current at a reduced output voltage level. To insure that load transient conditions do not momentarily cause deregulation of the output voltage, a 20% margin in the limit voltage is advisable. The current-sense resistor should therefore be set by the relationship:

$$R_{SENSE} = 100mV / I_{peak}$$

where: $I_{peak} = I_{MAX} \bullet 1.33$

Since the value of the sense resistor is generally in the milliohm region, care should be taken in the layout of the PCB to minimize trace resistances. The traces to the IFB and VFB pins of the RC5601 should be Kelvin connected to the pads of the current sense resistor as illustrated in the sample layout of Figure 4. To minimize the influence of noise, the two traces should be run directly next to each other and the pins should be bypassed with a 0.1µF capacitor to GND as close to the device pins as possible.

Output Filter Capacitors

Optimal ripple performance and transient response are functions of the filter capacitors used. Since the 5V supply of a PC motherboard may be located several inches away from the DC-DC converter, input capacitance can play an important role in the load transient response of the RC5601.
The higher the input capacitance, the more charge storage is available for improving the current transfer through the FET. Low "ESR" capacitors are best suited for this type of application and can influence the converter's efficiency if not chosen carefully. The input capacitor should be placed as close to the drain of the FET as possible to reduce the effect of ringing caused by long trace lengths.

The ESR rating of a capacitor is a difficult number to quantify. ESR or Equivalent Series Resistance, is defined as the resonant impedance of the capacitor. Since the capacitor is actually a complex impedance device having resistance, inductance and capacitance, it is quite natural for this device to have a resonant frequency. As a rule, the lower the ESR, the better suited the capacitor is for use in switching power supply applications. Many capacitor manufacturers do not supply ESR data. A useful estimate of the ESR can be obtained using the following equation:

$$ESR = \frac{DF}{2\pi fC}$$

Where:

- DF is the dissipation factor of the capacitor
- f is the operating frequency
- C is the capacitance in farads

With this in mind, correct calculation of the output capacitance is crucial to the performance of the DC-DC converter. The output capacitor determines the overall loop stability, output voltage ripple and load transient response. The calculation is as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR}$$

Where ΔV is the maximum voltage deviation due load transient

ΔT is reaction time of the power source (Loop response time of the RC5601) and it is approximately 8µs

I_O is the output load current

For I_O = 10A, and ΔV = 75mV, the bulk capacitor required can be approximated as follows:

$$C(\mu F) = \frac{I_O \times \Delta T}{\Delta V - I_O \times ESR} = \frac{10A \times 8\mu s}{75mV - 10A \times 5m\Omega} = 3200\mu F$$

Schottky Diode Selection

The application circuit diagram of Figure 1 shows two Schottky diodes, DS1 and DS2. In synchronous mode, DS1 is used in parallel with M3 to prevent the lossy diode in the FET from turning on. DS2 serves a dual purpose. As configured, it allows the VCCQP supply pin of the RC5040 to be bootstrapped up to 9V using capacitor C12. When the lower MOSFET M3 is turned on, one side of capacitor C12 is connected to ground while the other side of the capacitor is being charged up to voltage VIN - VD through DS2. The voltage that is then applied to the gate of the MOSFET is VCCQP – VSAT, or typically around 9V. A vital selection criteria for DS1 and DS2 is that they exhibit a very low forward voltage drop, as this parameter can directly affect the regulator efficiency. In non-synchronous mode, DS1 is used as a flyback diode to provide a constant current path for the inductor when M1 is turned off. Table 2 lists several suitable Schottky diodes. Note that the MBR2015CTL has a very low forward voltage drop. This diode is most ideal for application where output voltage is required to be less than 2.8V.

Table 2. Schottky Diode Selection Table

Manufacturer Model #	Conditions	Forward Voltage V_F
Philips PBYR1035	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2035CT	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR1545CT	I_F = 15A; T_j = 25°C I_F = 15A; T_j = 125°C	< 0.84V < 0.72V
Motorola MBR2015CTL	I_F = 20A; T_j = 25°C I_F = 20A; T_j = 150°C	< 0.58V < 0.48V

MOSFET Switch

The MOSFET switch in the RC5601 application circuit of Figure 1 is an N-channel, "logic-level" FET. This means that it will be fully on with a V_{GS} of 4V. Many manufacturers offer logic-level FETs, where the primary goal is to select the device with the lowest $R_{DS, ON}$ at the given maximum current level, I_{MAX}. The value of R_{DSON} factors directly into the efficiency equation as a power loss. Also influencing the efficiency is the gate charge of the FET and the clock frequency of the RC5601. At higher clock frequencies, the amount of charge required by the FET will lower the overall efficiency. In higher current applications, the upper FET can be paralleled to provide greater output current capability.

Preliminary Information

Preliminary Information

PCB Layout and Grounding

As is the case with most analog circuitry, good layout practices are necessary to achieve the optimal overall performance of the DC-DC converter. In general, it is always preferrable to create a tight layout that attempts to utilize short, low inductance traces to the RC5601.

The use of a multilayer PCB is recommended. In particular, a continuous ground plane should be placed directly beneath the circuit, using 2 oz copper in high current applications. As was previously stated, the current-sense resistor R_{SENSE} should be located as close as possible to the RC5601 and the IFB and VFB traces should be Kelvin connected to the pads of R_{SENSE}. To minimize switching losses and noise, place M1, L1 and DS2 as close together as possible and also attempt to keep the DRV gate drive signal trace as short as possible. Furthermore, the noisy switching portion of the circuit should be physically distanced from the low current pins of the device such as IFB, VFB, VREF and CEXT. All 0.1µF bypass capacitors should be as close to the device pins as possible and all ground pins should be terminated at the ground plane directly under the chip. A sample layout for the RC5601 is provided in Figure 3, illustrating the optimum layout for meeting the Intel® voltage requirements for powering the GTL+ bus in a Pentium Pro processor application.

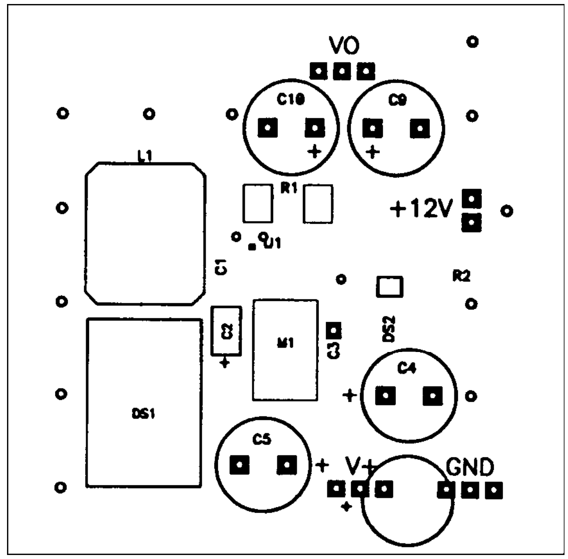


Figure 3. Sample PCB Layout for RC5601

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Preliminary Information

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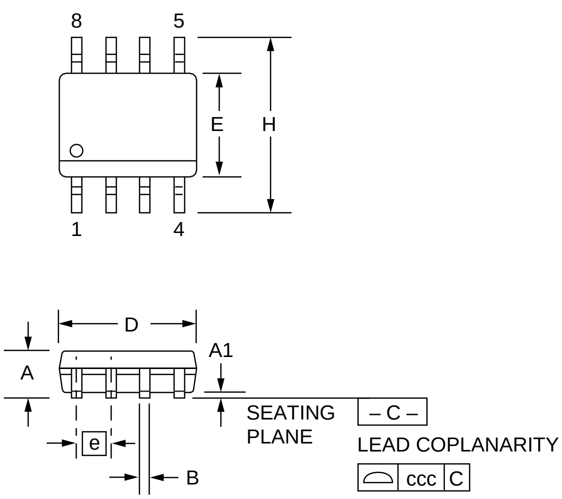
Preliminary Information

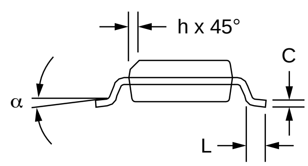
Mechanical Dimensions – 8 Lead SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.





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Ordering Information

Product Number	Package
RC5601M	8 pin SOIC

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