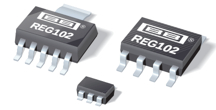
Burr-Brown Products from Texas Instruments

REG102



SBVS024E – NOVEMBER 2000 – REVISED MARCH 2003

DMOS 250mA Low-Dropout Regulator

FEATURES

- **NEW DMOS TOPOLOGY:**
  Ultra Low Dropout Voltage:
  150mV typ at 250mA
  Output Capacitor *not* Required for Stability
- **FAST TRANSIENT RESPONSE**
- **VERY LOW NOISE: 28µVrms**
- **HIGH ACCURACY: ±1.5% max**
- **HIGH EFFICIENCY:**
  I_{GND} = 600µA at I_{OUT} = 250mA
  Not Enabled: I_{GND} = 0.01µA
- **2.5V, 2.8V, 2.85V, 3.0V, 3.3V, AND 5.0V ADJUSTABLE OUTPUT VERSIONS**
- **OTHER OUTPUT VOLTAGES AVAILABLE UPON REQUEST**
- **FOLDBACK CURRENT LIMIT**
- **THERMAL PROTECTION**
- **SMALL SURFACE-MOUNT PACKAGES: SOT23-5, SOT223-5, and SO-8**

APPLICATIONS

- **PORTABLE COMMUNICATION DEVICES**
- **BATTERY-POWERED EQUIPMENT**
- **PERSONAL DIGITAL ASSISTANTS**
- **MODEMS**
- **BAR-CODE SCANNERS**
- **BACKUP POWER SUPPLIES**

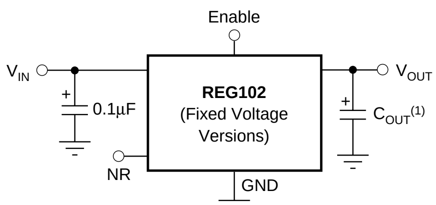
DESCRIPTION

The REG102 is a family of low-noise, low-dropout linear regulators with low ground pin current. The new DMOS topology provides significant improvement over previous designs, including low-dropout voltage (only 150mV typ at full load), and better transient performance. In addition, no output capacitor is required for stability, unlike conventional low-dropout regulators that are difficult to compensate and require expensive low ESR capacitors greater than 1µF.

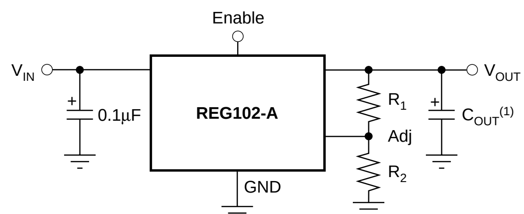
Typical ground pin current is only 600µA (at I_{OUT} = 250mA) and drops to 10nA when not enabled. Unlike regulators with PNP pass devices, quiescent current remains relatively constant over load variations and under dropout conditions.

The REG102 has very low output noise (typically 28µVrms for V_{OUT} = 3.3V with C_{NR} = 0.01µF), making it ideal for use in portable communications equipment. On-chip trimming results in high output voltage accuracy. Accuracy is maintained over temperature, line, and load variations. Key parameters are tested over the specified temperature range (–40°C to +85°C).

The REG102 is well protected—internal circuitry provides a current limit that protects the load from damage; furthermore, thermal protection circuitry keeps the chip from being damaged by excessive temperature. The REG102 is available in SOT23-5, SOT223-5, and SO-8 packages.



NR = Noise Reduction

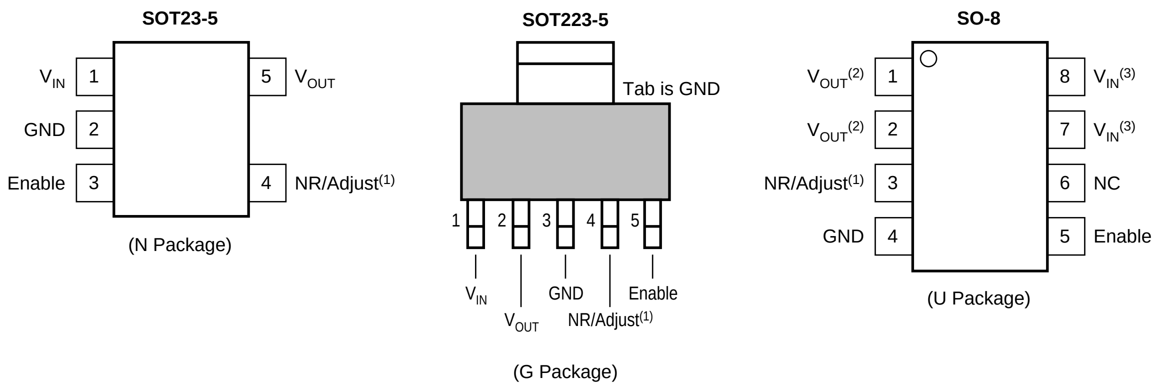


NOTE: (1) Optional.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PIN CONFIGURATIONS

Top View



NOTES: (1) For REG102A-A: voltage setting resistor pin.
All other models: noise reduction capacitor pin.
(2) Both pin 1 and pin 2 must be connected.
(3) Both pin 7 and pin 8 must be connected.

ABSOLUTE MAXIMUM RATINGS(1)

Supply Input Voltage, V_{IN}	–0.3V to 12V
Enable Input	–0.3V to V_{IN}
Output Short-Circuit Duration	Indefinite
Operating Temperature Range (T_J)	–55°C to +125°C
Storage Temperature Range (T_A)	–65°C to +150°C
Lead Temperature (soldering, 3s)	+240°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
5V Output					
REG102	SOT23-5	DBV	R02B	REG102NA-5/250	Tape and Reel, 250
"	"	"	"	REG102NA-5/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102U5	REG102UA-5	Rails, 100
"	"	"	"	REG102UA-5/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102G50	REG102GA-5	Rails, 78
"	"	"	"	REG102GA-5/2K5	Tape and Reel, 2500
3.3V Output					
REG102	SOT23-5	DBV	R02C	REG102NA-3.3/250	Tape and Reel, 250
"	"	"	"	REG102NA-3.3/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102U33	REG102UA-3.3	Rails, 100
"	"	"	"	REG102UA-3.3/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102G33	REG102GA-3.3	Rails, 78
"	"	"	"	REG102GA-3.3/2K5	Tape and Reel, 2500
3V Output					
REG102	SOT23-5	DBV	R02G	REG102NA-3/250	Tape and Reel, 250
"	"	"	"	REG102NA-3/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102U3	REG102UA-3	Rails, 100
"	"	"	"	REG102UA-3/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102G30	REG102GA-3	Rails, 78
"	"	"	"	REG102GA-3/2K5	Tape and Reel, 2500
2.85V Output					
REG102	SOT23-5	DBV	R02N	REG102NA-2.85/250	Tape and Reel, 250
"	"	"	"	REG102NA-2.85/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102285	REG102UA-2.85	Rails, 100
"	"	"	"	REG102UA-2.85/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102285	REG102GA-2.85	Rails,78
"	"	"	"	REG102GA-2.85/2K5	Tape and Reel, 2500
2.8V Output					
REG102	SOT23-5	DBV	R02E	REG102NA-2.8/250	Tape and Reel, 250
"	"	"	"	REG102NA-2.8/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102U28	REG102UA-2.8	Rails, 100
"	"	"	"	REG102UA-2.8/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102G28	REG102GA-2.8	Rails, 78
"	"	"	"	REG102GA-2.8/2K5	Tape and Reel, 2500
2.5V Output					
REG102	SOT23-5	DBV	R02D	REG102NA-2.5/250	Tape and Reel, 250
"	"	"	"	REG102NA-2.5/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102U25	REG102UA-2.5	Rails, 100
"	"	"	"	REG102UA-2.5/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	REG102G25	REG102GA-2.5	Rails, 78
"	"	"	"	REG102GA-2.5/2K5	Tape and Reel, 2500
Adjustable Output					
REG102	SOT23-5	DBV	R02A	REG102NA-A/250	Tape and Reel, 250
"	"	"	"	REG102NA-A/3K	Tape and Reel, 3000
REG102	SO-8	D	REG102UA	REG102UA-A	Rails, 100
"	"	"	"	REG102UA-A/2K5	Tape and Reel, 2500
REG102	SOT223-5	DCQ	R102GA	REG102GA-A	Rails, 78
"	"	"	"	REG102GA-A/2K5	Tape and Reel, 2500

NOTE: (1) For most current specifications and package information, refer to our web site at www.ti.com.

Many custom output voltage versions, from 2.5V to 5.1V in 50mV increments, are available upon request. Minimum order quantities apply. Contact factory for details.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, T_J = –40°C to +85°C.

At T_J = +25°C, V_{IN} = V_{OUT} + 1V (V_{OUT} = 2.5V for REG102-A), V_{ENABLE} = 1.8V, I_{OUT} = 5mA, C_{NR} = 0.01µF, and C_{OUT} = 0.1µF(1), unless otherwise noted.

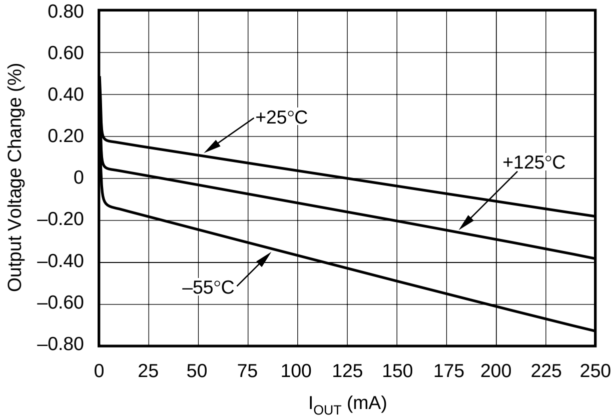
PARAMETER		CONDITION	REG102NA REG102GA REG102UA MIN	TYP	MAX	UNITS
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT}					
REG102-2.5				2.5		V
REG102-2.8				2.8		V
REG102-2.85				2.85		V
REG102-3.0				3.0		V
REG102-3.3				3.3		V
REG102-5				5		V
REG102-A			2.5		5.5	V
Reference Voltage	V_{REF}			1.26		V
Adjust Pin Current	I_{ADJ}			0.2	1	µA
Accuracy				±0.5	±1.5	%
Over Temperature					**±2.3**	%
vs Temperature	**dV_{OUT}/dT**			**50**		ppm/°C
vs Line and Load		I_{OUT} = 5mA to 250mA, V_{IN} = (V_{OUT} + 0.4V) to 10V		±0.8	±2.0	%
Over Temperature		**V_{IN} = (V_{OUT} + 0.6V) to 10V**			**±2.8**	**%**
DC DROPOUT VOLTAGE(2)	V_{DROP}	I_{OUT} = 5mA		4	10	mV
For all models		I_{OUT} = 250mA		150	220	mV
Over Temperature		**I_{OUT} = 250mA**			**270**	mV
VOLTAGE NOISE						
f = 10Hz to 100kHz	V_n					
Without C_{NR} (all models)		C_{NR} = 0, C_{OUT} = 0		23µVrms/V • V_{OUT}		µVrms
With C_{NR} (all fixed voltage models)		C_{NR} = 0.01µF, C_{OUT} = 10µF		7µVrms/V • V_{OUT}		µVrms
OUTPUT CURRENT						
Current Limit(3)	I_{CL}		340	400	470	mA
Over Temperature			**300**		**490**	mA
Short-Circuit Current Limit	I_{SC}			150		mA
RIPPLE REJECTION						
f = 120Hz				65		dB
ENABLE CONTROL						
V_{ENABLE} High (output enabled)	V_{ENABLE}		1.8		V_{IN}	V
V_{ENABLE} Low (output disabled)			–0.2		0.5	V
I_{ENABLE} High (output enabled)	I_{ENABLE}	V_{ENABLE} = 1.8V to V_{IN}, V_{IN} = 1.8V to 6.5(4)		1	100	nA
I_{ENABLE} Low (output disabled)		V_{ENABLE} = 0V to 0.5V		2	100	nA
Output Disable Time		C_{OUT} = 1.0µF, R_{LOAD} = 13Ω		50		µs
Output Enable Softstart Time		C_{OUT} = 1.0µF, R_{LOAD} = 13Ω		1.5		ms
THERMAL SHUTDOWN						
Junction Temperature						
Shutdown				160		°C
Reset from Shutdown				140		°C
GROUND PIN CURRENT						
Ground Pin Current	I_{GND}	I_{OUT} = 5mA		400	500	µA
		I_{OUT} = 250mA		600	800	µA
Enable Pin Low		V_{ENABLE} ≤ 0.5V		0.01	0.2	µA
INPUT VOLTAGE	V_{IN}					
Operating Input Voltage Range(5)			1.8		10	V
Specified Input Voltage Range		V_{IN} > 1.8V	V_{OUT} + 0.4		10	V
Over Temperature		**V_{IN} > 1.8V**	**V_{OUT} + 0.6**		**10**	V
TEMPERATURE RANGE						
Specified Range	T_J		–40		+85	°C
Operating Range	T_J		–55		+125	°C
Storage Range	T_A		–65		+150	°C
Thermal Resistance						
SOT23-5 Surface-Mount	θ_{JA}	Junction-to-Ambient		200		°C/W
SO-8 Surface-Mount	θ_{JA}	Junction-to-Ambient		150		°C/W
SOT223-5 Surface-Mount	θ_{JC}	Junction-to-Case		15		°C/W
	θ_{JA}	Junction-to-Ambient		See Figure 8		°C/W

NOTES: (1) The REG102 does not require a minimum output capacitor for stability, however, transient response can be improved with proper capacitor selection. (2) Dropout voltage is defined as the input voltage minus the output voltage that produces a 2% change in the output voltage from the value at V_{IN} = V_{OUT} + 1V at fixed load. (3) Current limit is the output current that produces a 10% change in output voltage from V_{IN} = V_{OUT} + 1V and I_{OUT} = 5mA. (4) For V_{ENABLE} > 6.5V, see typical characteristic *I_{ENABLE} vs V_{ENABLE}*. (5) The REG102 no longer regulates when V_{IN} < V_{OUT} + $V_{DROP\ (MAX)}$. In dropout, the impedance from V_{IN} to V_{OUT} is typically less than 1Ω at T_J = +25°C.

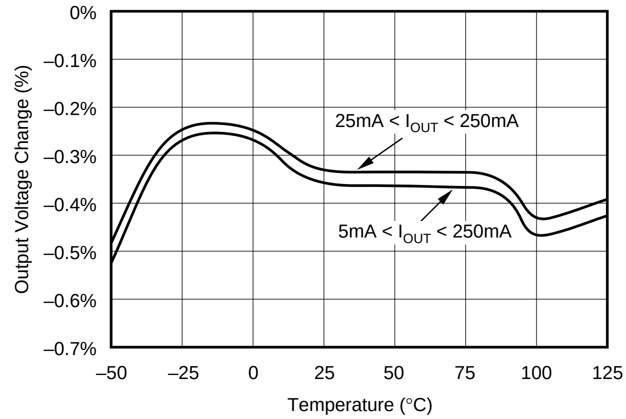
TYPICAL CHARACTERISTICS

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

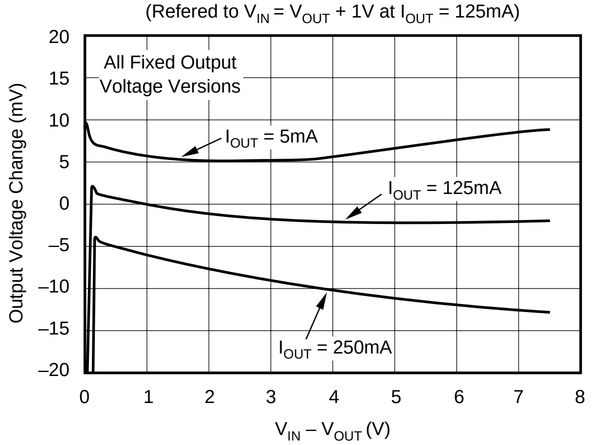
OUTPUT VOLTAGE CHANGE vs I_{OUT}
($V_{IN} = V_{OUT}$ + 1V, Output Voltage % Change
Refered to I_{OUT} = 125mA at +25°C)



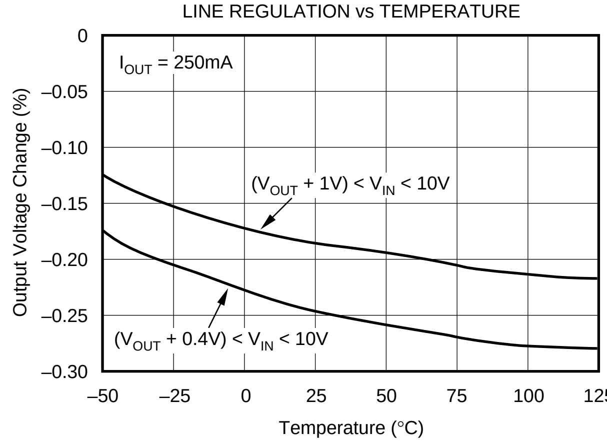
LOAD REGULATION vs TEMPERATURE
($V_{IN} = V_{OUT}$ + 1V)



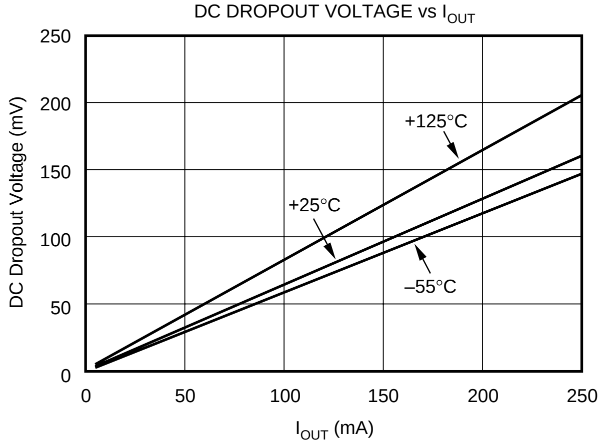
LINE REGULATION
(Refered to $V_{IN} = V_{OUT}$ + 1V at I_{OUT} = 125mA)



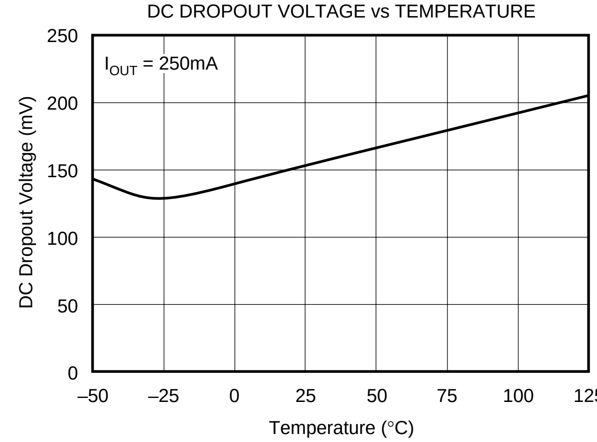
LINE REGULATION vs TEMPERATURE



DC DROPOUT VOLTAGE vs I_{OUT}



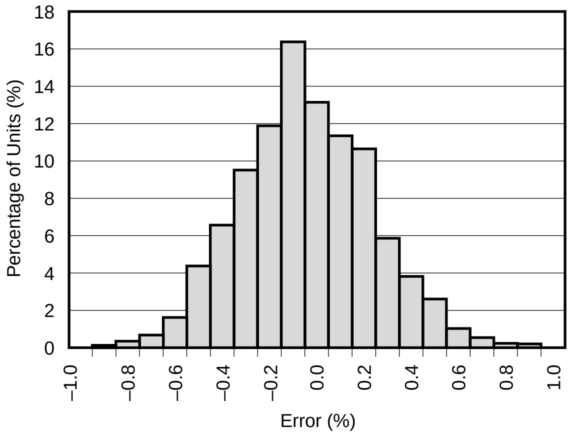
DC DROPOUT VOLTAGE vs TEMPERATURE



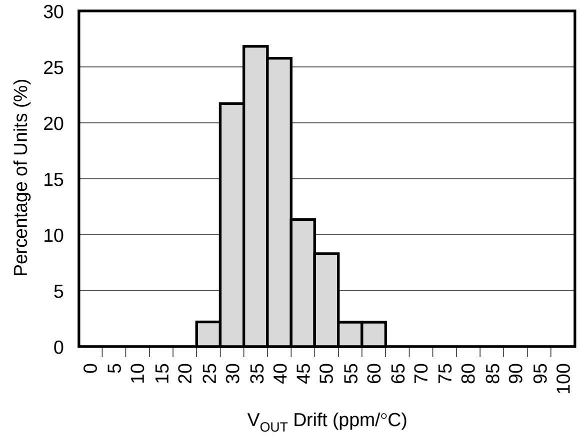
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

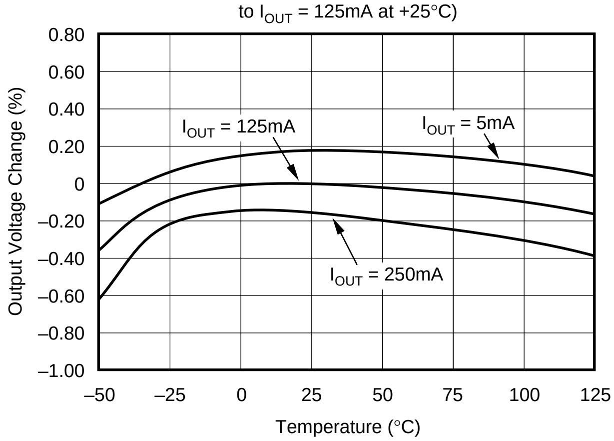
OUTPUT VOLTAGE ACCURACY HISTOGRAM



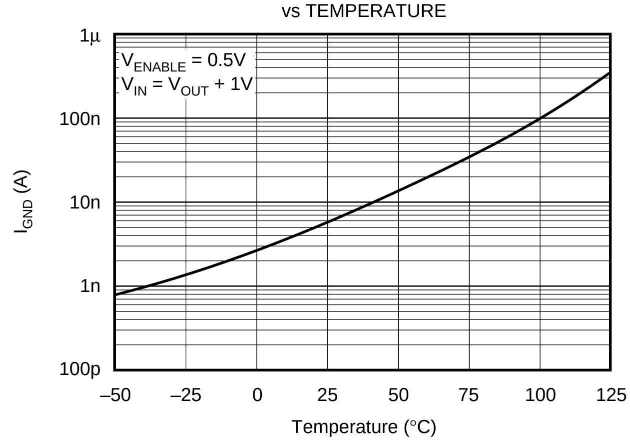
OUTPUT VOLTAGE DRIFT HISTOGRAM



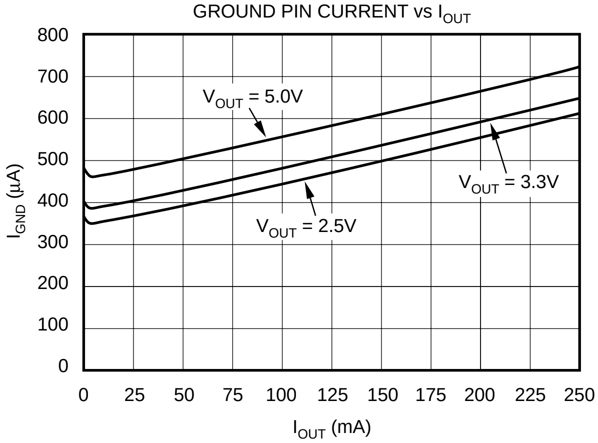
OUTPUT VOLTAGE vs TEMPERATURE
(Output Voltage % Change Refered
to I_{OUT} = 125mA at +25°C)



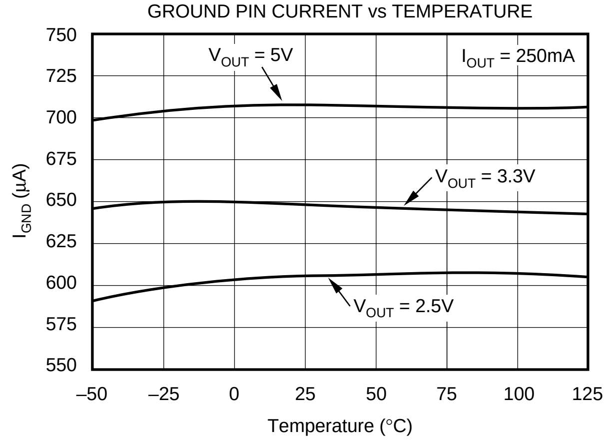
GROUND PIN CURRENT, NOT ENABLED
vs TEMPERATURE



GROUND PIN CURRENT vs I_{OUT}



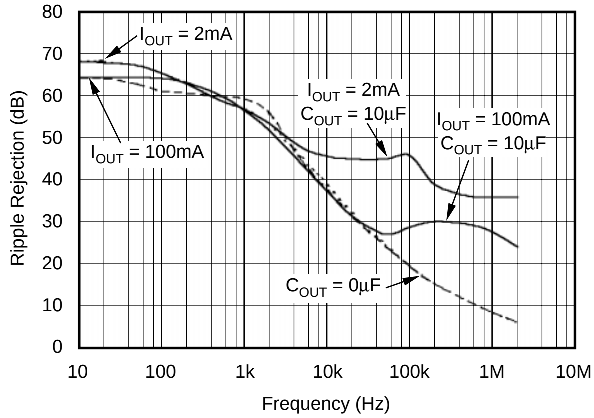
GROUND PIN CURRENT vs TEMPERATURE



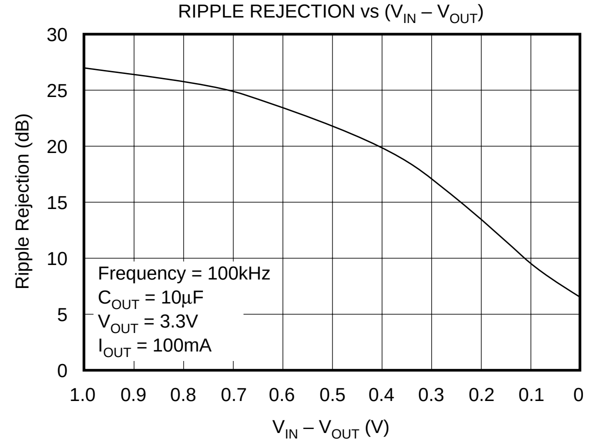
TYPICAL CHARACTERISTICS (Cont.)

For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

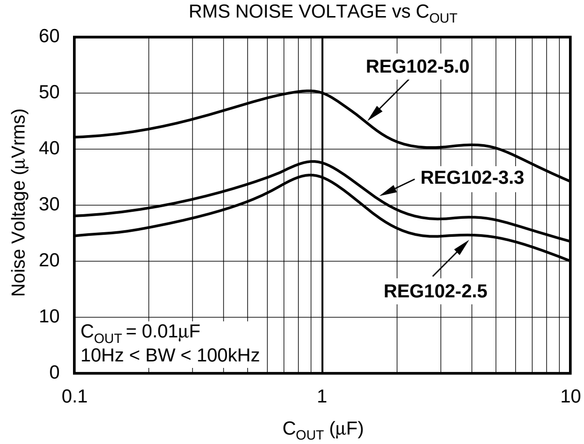
RIPPLE REJECTION vs FREQUENCY



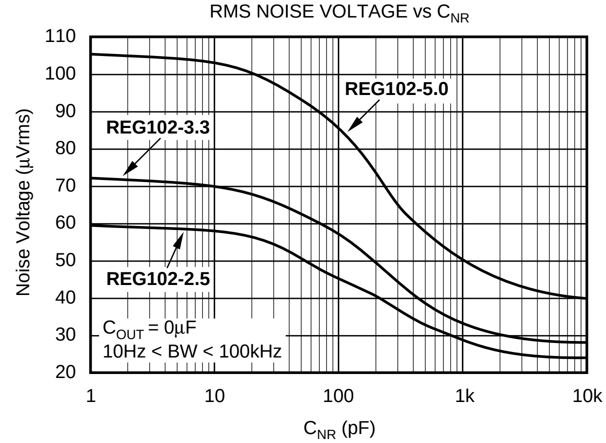
RIPPLE REJECTION vs (V_{IN} – V_{OUT})



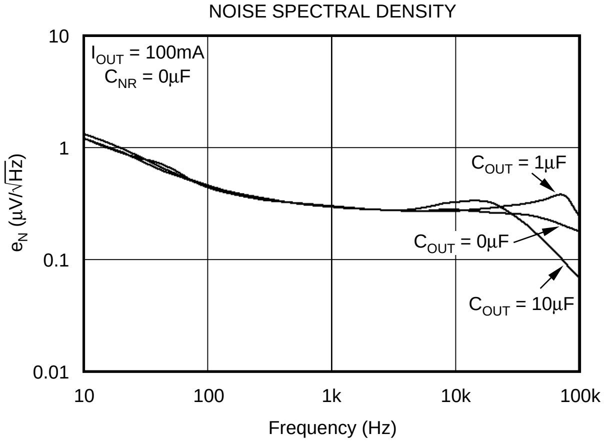
RMS NOISE VOLTAGE vs C_{OUT}



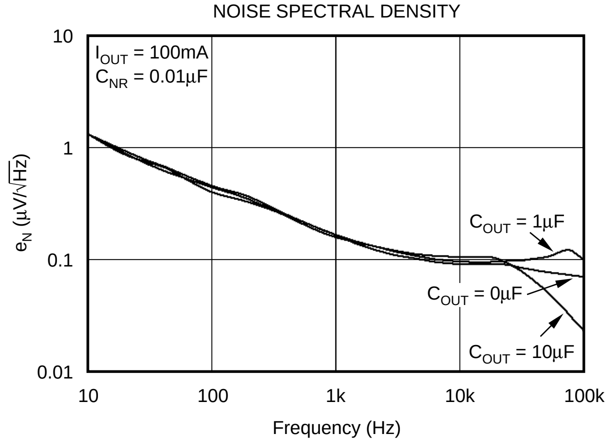
RMS NOISE VOLTAGE vs C_{NR}



NOISE SPECTRAL DENSITY

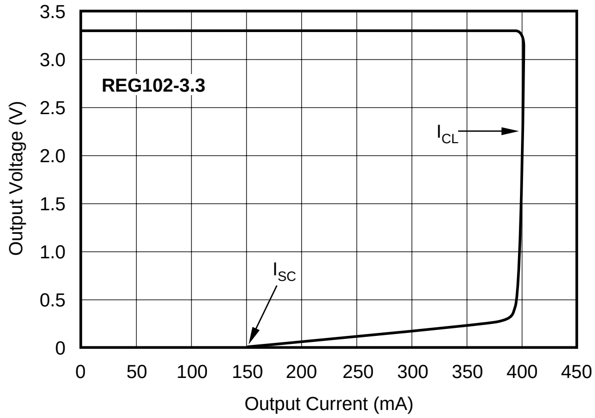


NOISE SPECTRAL DENSITY

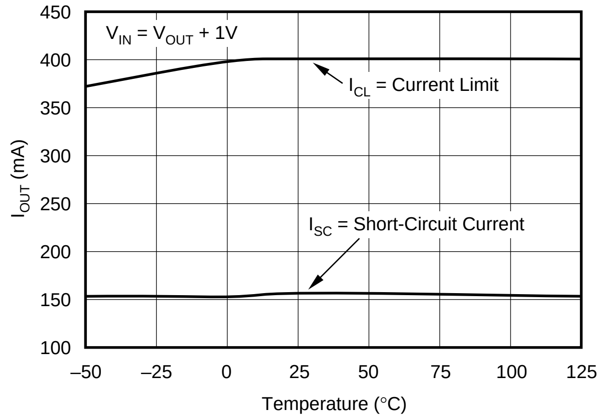


For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

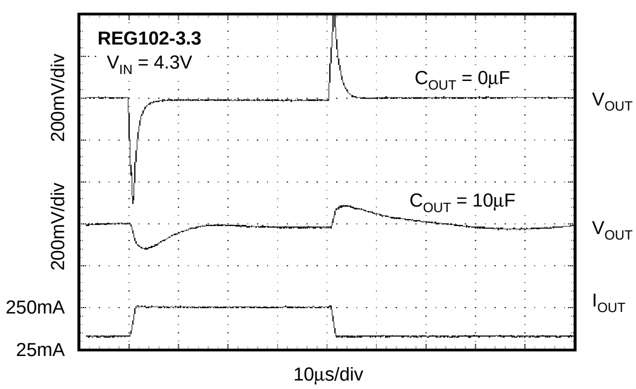
CURRENT LIMIT FOLDBACK



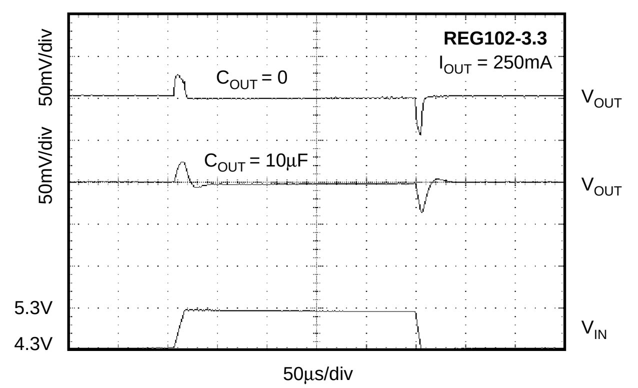
CURRENT LIMIT vs TEMPERATURE



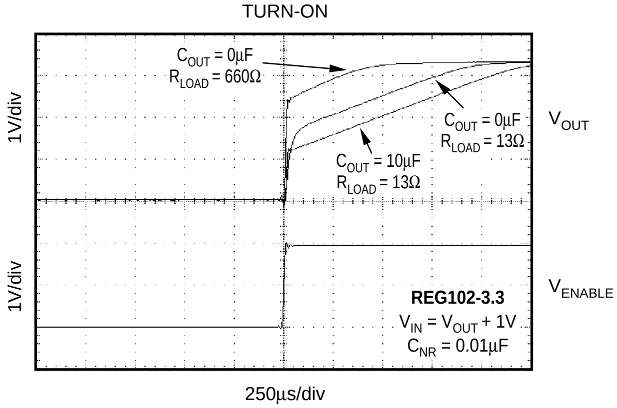
LOAD TRANSIENT RESPONSE



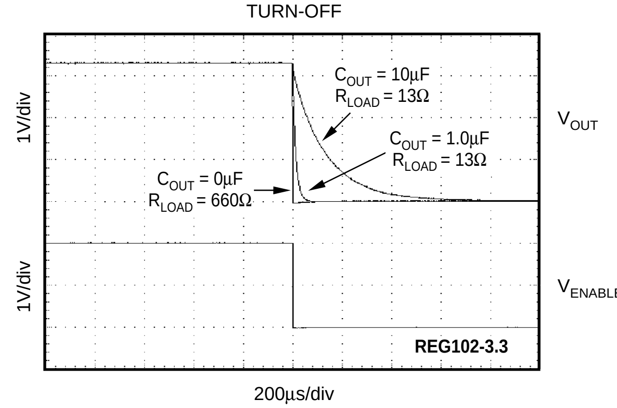
LINE TRANSIENT RESPONSE



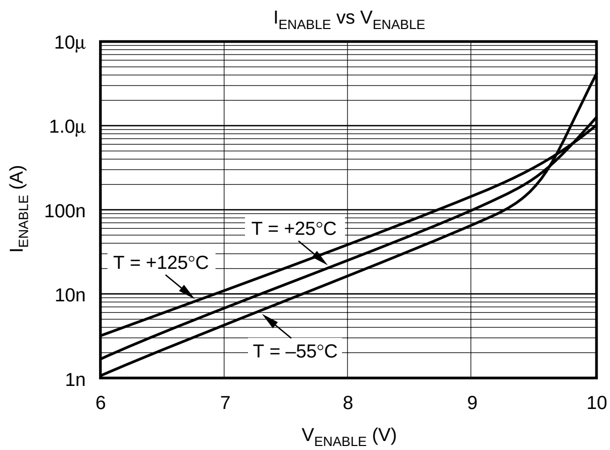
TURN-ON

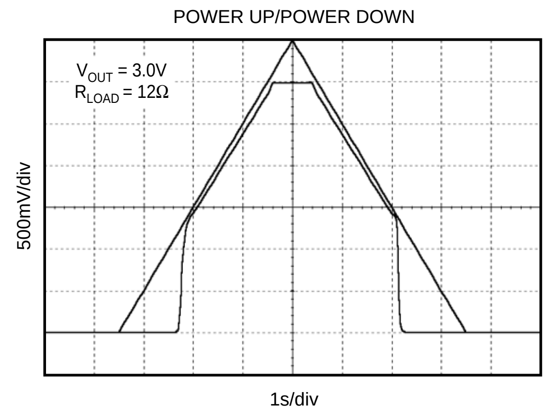


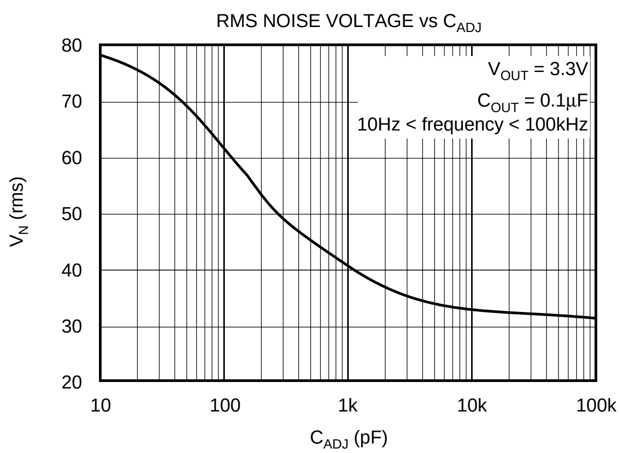
TURN-OFF

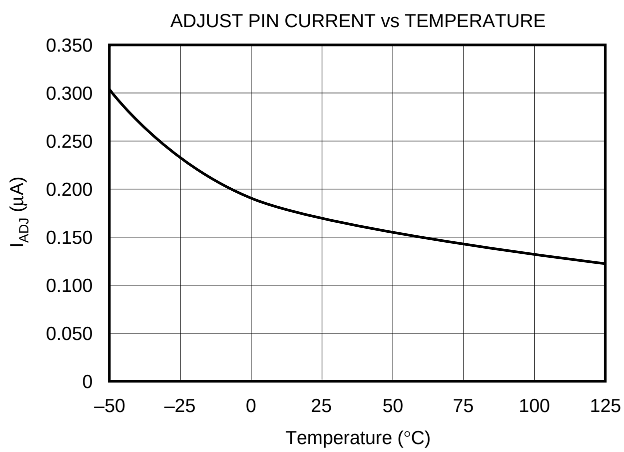


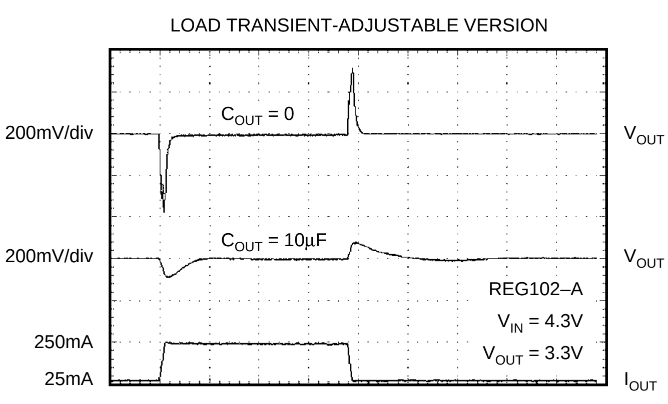
For all models, at T_J = +25°C and V_{ENABLE} = 1.8V, unless otherwise noted.

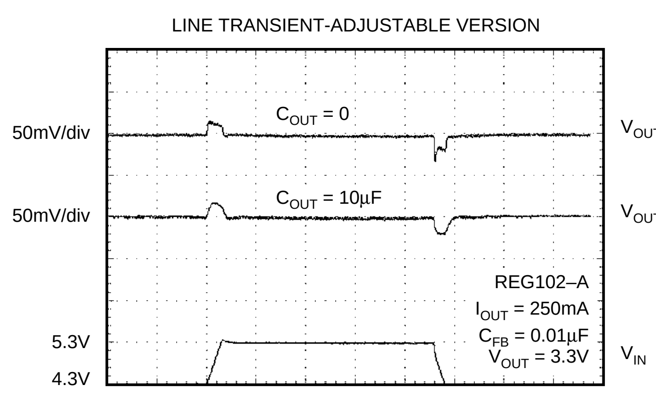












BASIC OPERATION

The REG102 series of LDO (low dropout) linear regulators offers a wide selection of fixed output voltage versions and an adjustable output version as well. The REG102 belongs to a family of new generation LDO regulators that use a DMOS pass transistor to achieve ultra low-dropout performance and freedom from output capacitor constraints. Ground pin current remains under 1mA over all line, load, and temperature conditions. All versions have thermal and over-current protection, including foldback current limit.

The REG102 does not require an output capacitor for regulator stability and is stable over most output currents and with almost any value and type of output capacitor up to 10µF or more. For applications where the regulator output current drops below several milliamps, stability can be enhanced by adding a 1kΩ to 2kΩ load resistor, using capacitance values smaller than 10µF, or keeping the effective series resistance greater than 0.05Ω including the capacitor ESR and parasitic resistance in printed circuit board traces, solder joints, and sockets.

Although an input capacitor is not required, it is a good standard analog design practice to connect a 0.1µF low ESR capacitor across the input supply voltage. This is recommended to counteract reactive input sources and improve ripple rejection by reducing input voltage ripple.

Figure 1 shows the basic circuit connections for the fixed voltage models. Figure 2 gives the connections for the adjustable output version (REG102A) and example resistor values for some commonly used output voltages. Values for other voltages can be calculated from the equation shown in Figure 2.

INTERNAL CURRENT LIMIT

The REG102 internal current limit has a typical value of 400mA. A foldback feature limits the short-circuit current to a typical short-circuit value of 150mA, which helps to protect the regulator from damage under all load conditions. A characteristic of V_{OUT} versus I_{OUT} is given in Figure 3 and in the Typical Characteristics section.

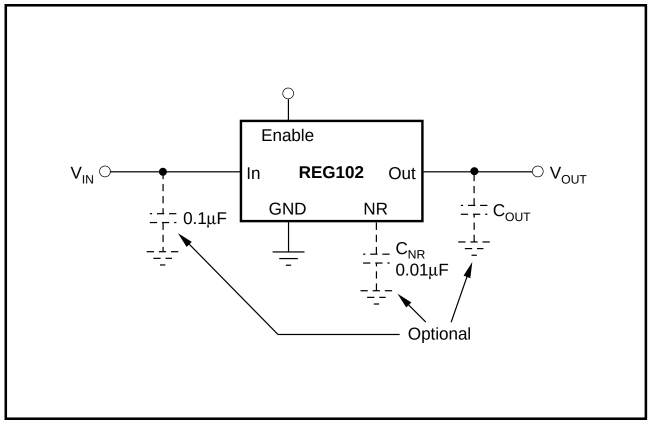


FIGURE 1. Fixed Voltage Nominal Circuit for the REG102.

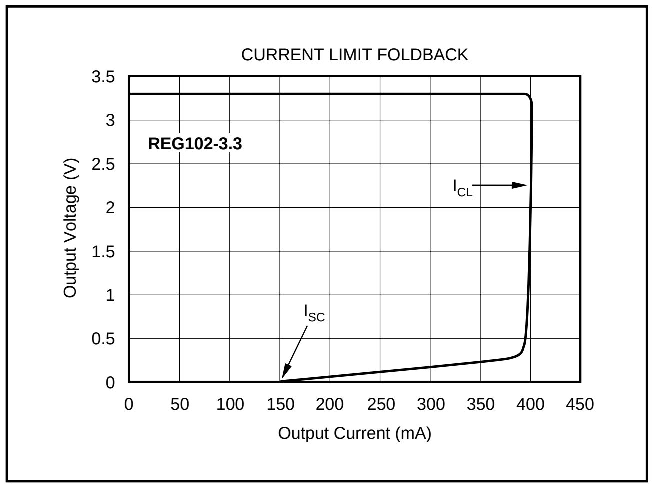
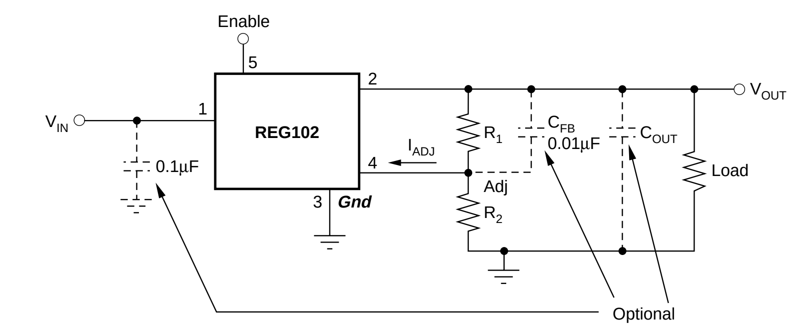


FIGURE 3. Foldback Current Limit of the REG102-3.3 at 25°C.



Pin numbers for the SOT-223 package.

EXAMPLE RESISTOR VALUES

V_{OUT} (V)	R_1 (Ω)(1)	R_2 (Ω)(1)
2.5	11.3k 1.13k	11.5k 1.15k
3.0	15.8k 1.58k	11.5k 1.15k
3.3	18.7k 1.87k	11.5k 1.15k
5.0	34.0k 3.40k	11.5k 1.15k

NOTE: (1) Resistors are standard 1% values.

$$V_{OUT} = (1 + R_1/R_2) \cdot 1.26V$$

To reduce current through divider, increase resistor values (see table at right).

As the impedance of the resistor divider increases, I_{ADJ} (~200nA) may introduce an error.

C_{FB} improves noise and transient response.

FIGURE 2. Adjustable Voltage Circuit for the REG102A.

ENABLE

The Enable pin is active high and compatible with standard TTL-CMOS levels. Inputs below 0.5V (max) turn the regulator off and all circuitry is disabled. Under this condition, ground pin current drops to approximately 10nA. When not used, the Enable pin can be connected to V_{IN}. When a pull-up resistor is used, and operation below 1.8V is required, use pull-up resistor values below 50kΩ.

OUTPUT NOISE

A precision bandgap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the REG102 and generates approximately 29µVrms in the 10Hz to 100kHz bandwidth at the reference output. The regulator control loop gains up the reference noise, so that the noise voltage of the regulator is approximately given by:

$$V_N = 29\mu Vrms \frac{R_1 + R_2}{R2} = 29\mu Vrms \bullet \frac{V_{OUT}}{V_{REF}} \quad (1)$$

As the value of V_{REF} is 1.26V, this relationship reduces to:

$$V_N = 23 \frac{\mu Vrms}{V} \bullet V_{OUT} \quad (2)$$

Connecting a capacitor, C_{NR}, from the Noise Reduction (NR) pin to ground forms a low-pass filter for the voltage reference. Adding C_{NR} (as shown in Figure 4) forms a low-pass filter for the voltage reference. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by approximately a factor of 2.8 for V_{OUT} = 3.3V. This noise reduction effect is shown in Figure 5 and as *RMS Noise Voltage vs C_{NR}* in the Typical Characteristcs section.

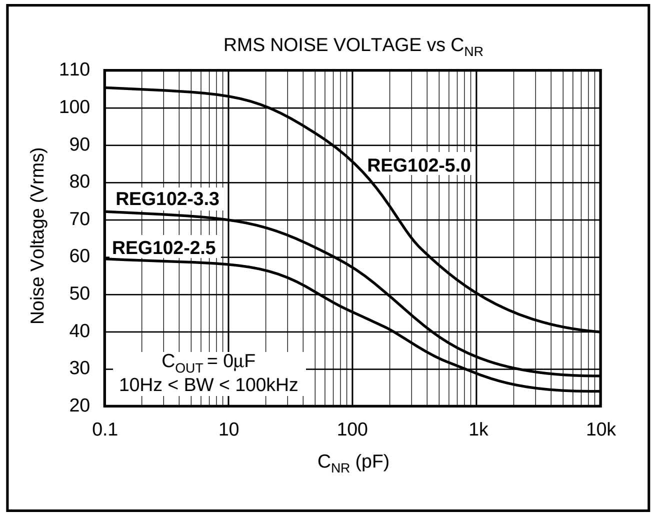


FIGURE 5. Output Noise versus Noise Reduction Capacitor.

Noise can be further reduced by carefully choosing an output capacitor, C_{OUT}. Best overall noise performance is achieved with very low (< 0.22µF) or very high (> 2.2µF) values of C_{OUT} (see the *RMS Noise Voltage vs C_{OUT}* typical characteristic).

The REG102 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the DMOS pass element above V_{IN}. The charge-pump switching noise (nominal switching frequency = 2MHz) is not measurable at the output of the regulator over most values of I_{OUT} and C_{OUT}.

The REG102 adjustable version does not have the noise-reduction pin available; however, the adjust pin is the summing junction of the error amplifier. A capacitor, C_{FB}, connected from the output to the adjust pin can reduce both the output noise and the peak error from a load transient (see the typical characteristics for output noise performance).

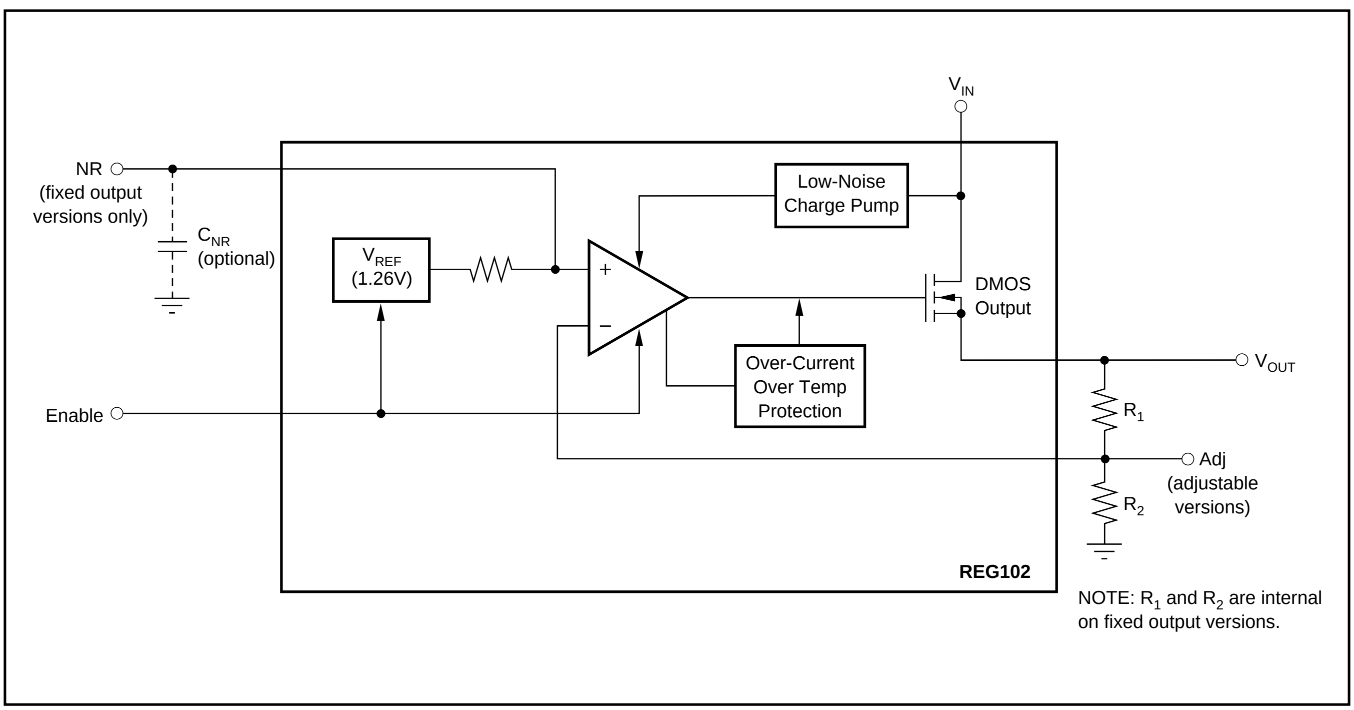


FIGURE 4. Block Diagram.

DROPOUT VOLTAGE

The REG102 uses an N-channel DMOS as the pass element. When (V_{IN} – V_{OUT}) is less than the drop-out voltage (V_{DROP}), the DMOS pass device behaves like a resistor; therefore, for low values of (V_{IN} – V_{OUT}), the regulator input-to-output resistance is the Rds_{ON} of the DMOS pass element (typically 600mΩ). For static (DC) loads, the REG102 typically maintains regulation down to a (V_{IN} – V_{OUT}) voltage drop of 150mV at full rated output current. In Figure 6, the bottom line (DC dropout) shows the minimum V_{IN} to V_{OUT} voltage drop required to prevent dropout under DC load conditions.

For large step changes in load current, the REG102 requires a larger voltage drop across it to avoid degraded transient response. The boundary of this transient drop-out region is shown as the top line in Figure 6 and values of V_{IN} to V_{OUT} voltage drop above this line insure normal transient response.

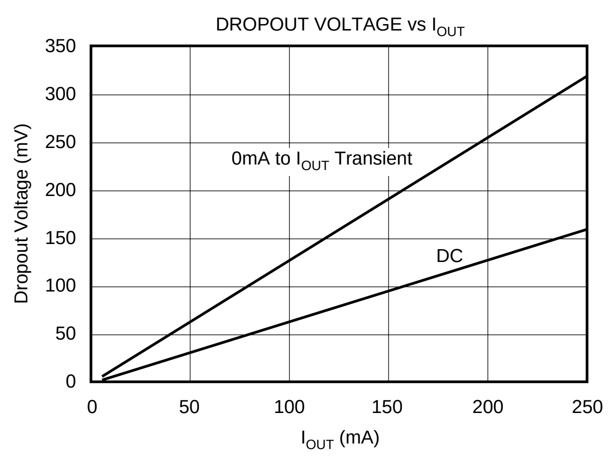


FIGURE 6. Transient and DC Dropout.

In the transient dropout region between DC and Transient, transient response recovery time increases. The time required to recover from a load transient is a function of both the magnitude and rate of the step change in load current and the available headroom V_{IN} to V_{OUT} voltage drop. Under worst-case conditions (full-scale load change with (V_{IN} – V_{OUT}) voltage drop close to DC dropout levels), the REG102 can take several hundred microseconds to re-enter the specified window of regulation.

TRANSIENT RESPONSE

The REG102 response to transient line and load conditions improves at lower output voltages. The addition of a capacitor (nominal value 0.47μF) from the output pin to ground can improve the transient response. In the adjustable version, the addition of a capacitor, C_{FB} (nominal value 10nF), from the output to the adjust pin can also improve the transient response.

THERMAL PROTECTION

Power dissipated within the REG102 can cause the junction temperature to rise. The REG102 has thermal shutdown circuitry that protects the regulator from damage which disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on various conditions, the thermal protection circuit can cycle on and off. This limits the dissipation of the regulator, but can have an undesirable effect on the load.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger more than 35°C above the maximum expected ambient condition of the application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the REG102 is designed to protect against overload conditions and is not intended to replace proper heat sinking. Continuously running the REG102 into thermal shutdown will degrade reliability.

POWER DISSIPATION

The REG102 is available in three different package configurations. The ability to remove heat from the die is different for each package type and, therefore, presents different considerations in the printed circuit-board layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Although it is difficult to impossible to quantify all of the variables in a thermal design of this type, performance data for several simplified configurations are shown in Figure 7. In all cases, the PCB copper area is bare copper (free of solder resist mask), not solder plated, and are for 1-ounce copper. Using heavier copper will increase the effectiveness in moving the heat from the device. In those examples where there is copper on both sides of the PCB, no connection has been provided between the two sides. The addition of plated through holes will improve the heat sink effectiveness.

Power dissipation depends on input voltage, load conditions, and duty cycle and is equal to the product of the average output current times the voltage across the output element, V_{IN} to V_{OUT} voltage drop.

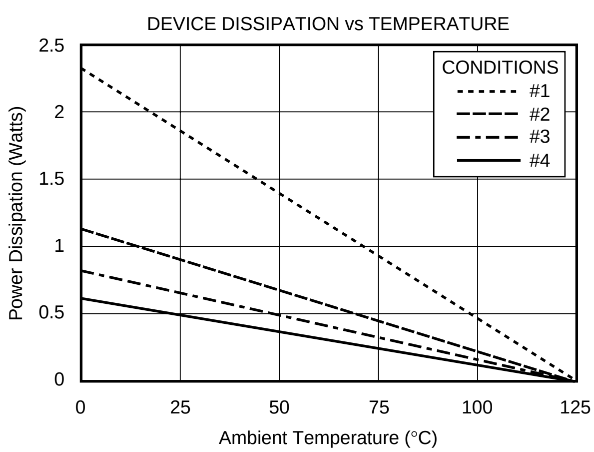
$$P_D = (V_{IN} - V_{OUT}) \bullet I_{OUT} \quad (3)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

REGULATOR MOUNTING

The tab of the SOT-223 package is electrically connected to ground. For best thermal performance, this tab must be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation, as shown in Figure 8.

Although the tab of the SOT-223 is electrical ground, it is not intended to carry current. The copper pad that acts as a heat sink should be isolated from the rest of the circuit to prevent current flow through the device from the tab to the ground pin. Solder pad footprint recommendations for the various REG102 devices are presented in Application Bulletin *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015), available from the Texas Instruments web site (www.ti.com).



CONDITION	PACKAGE	PCB AREA	THETA J-A
1	SOT-223	4in2 Top Side Only	53°C/W
2	SOT-223	0.5in2 Top Side Only	110°C/W
3	SO-8	—	150°C/W
4	SOT-23	—	200°C/W

FIGURE 7. Maximum Power Dissipation versus Ambient Temperature for the Various Packages and PCB Heat Sink Configurations.

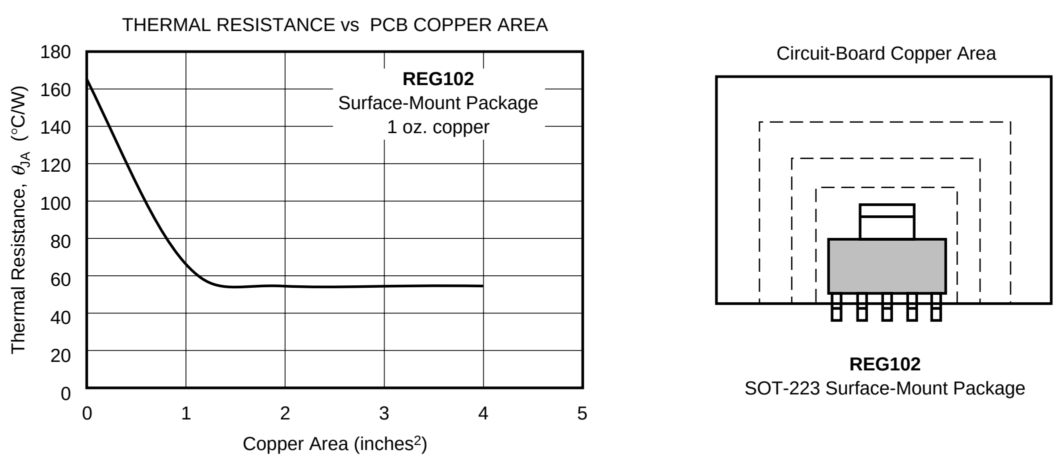
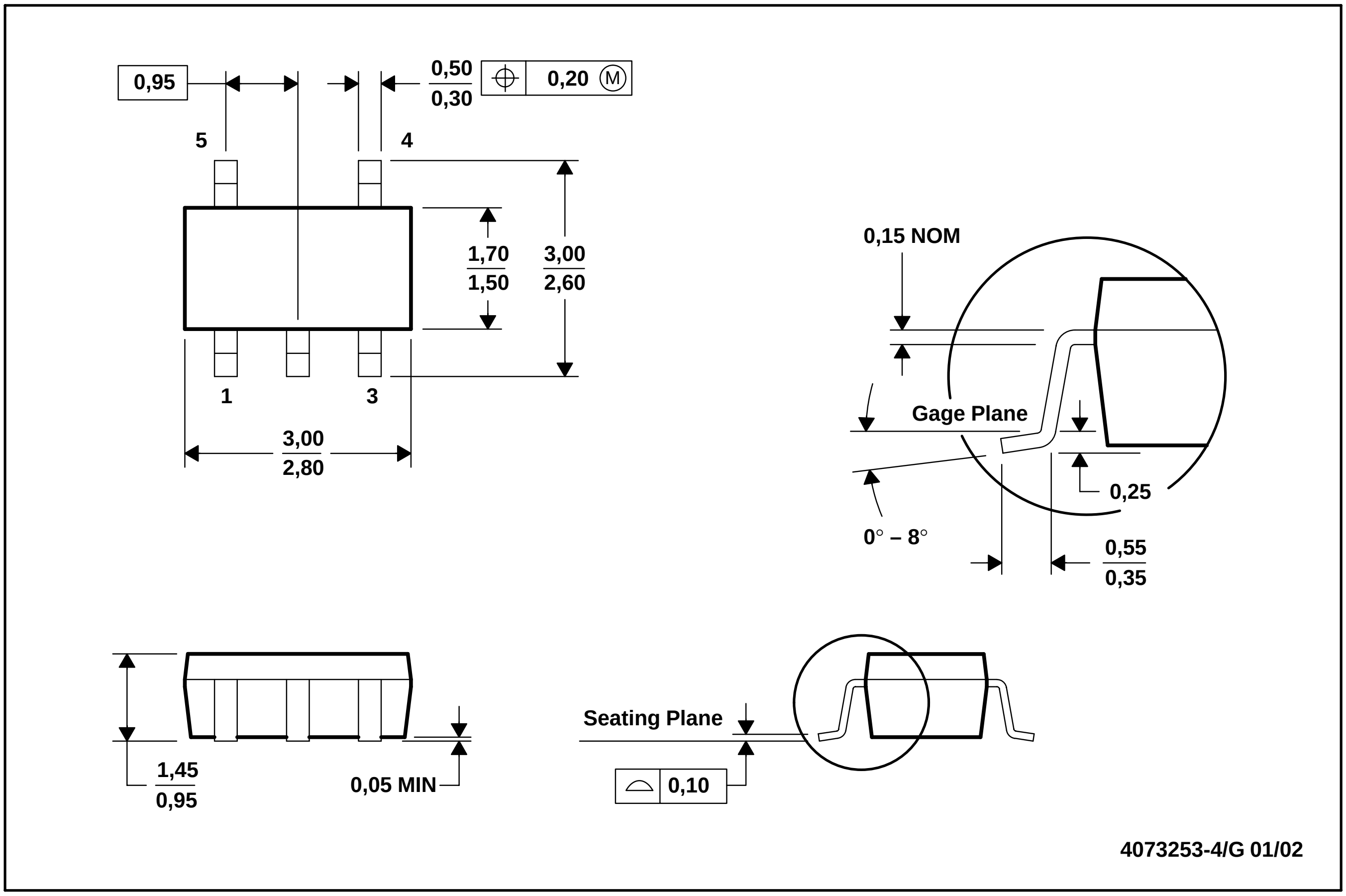


FIGURE 8. Thermal Resistance versus PCB Area for the Five Lead SOT-223.

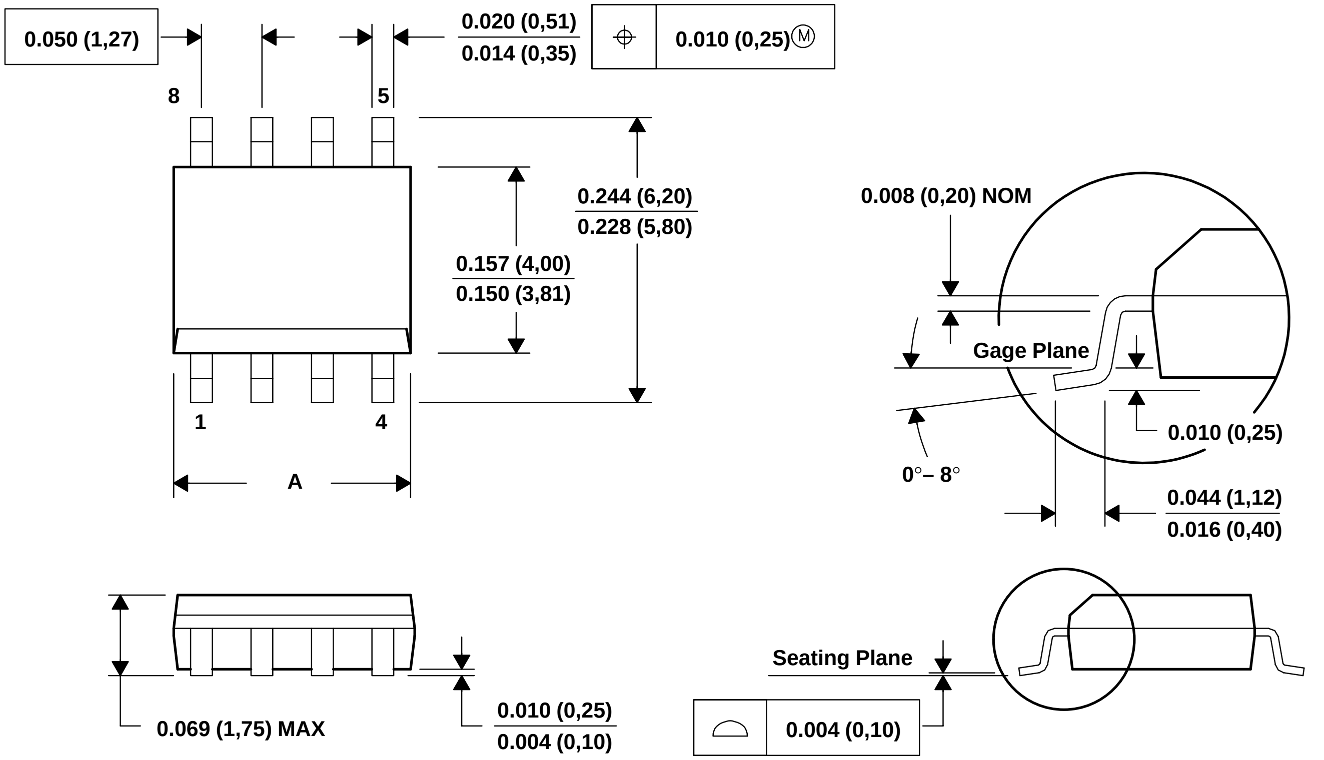
DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

D (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

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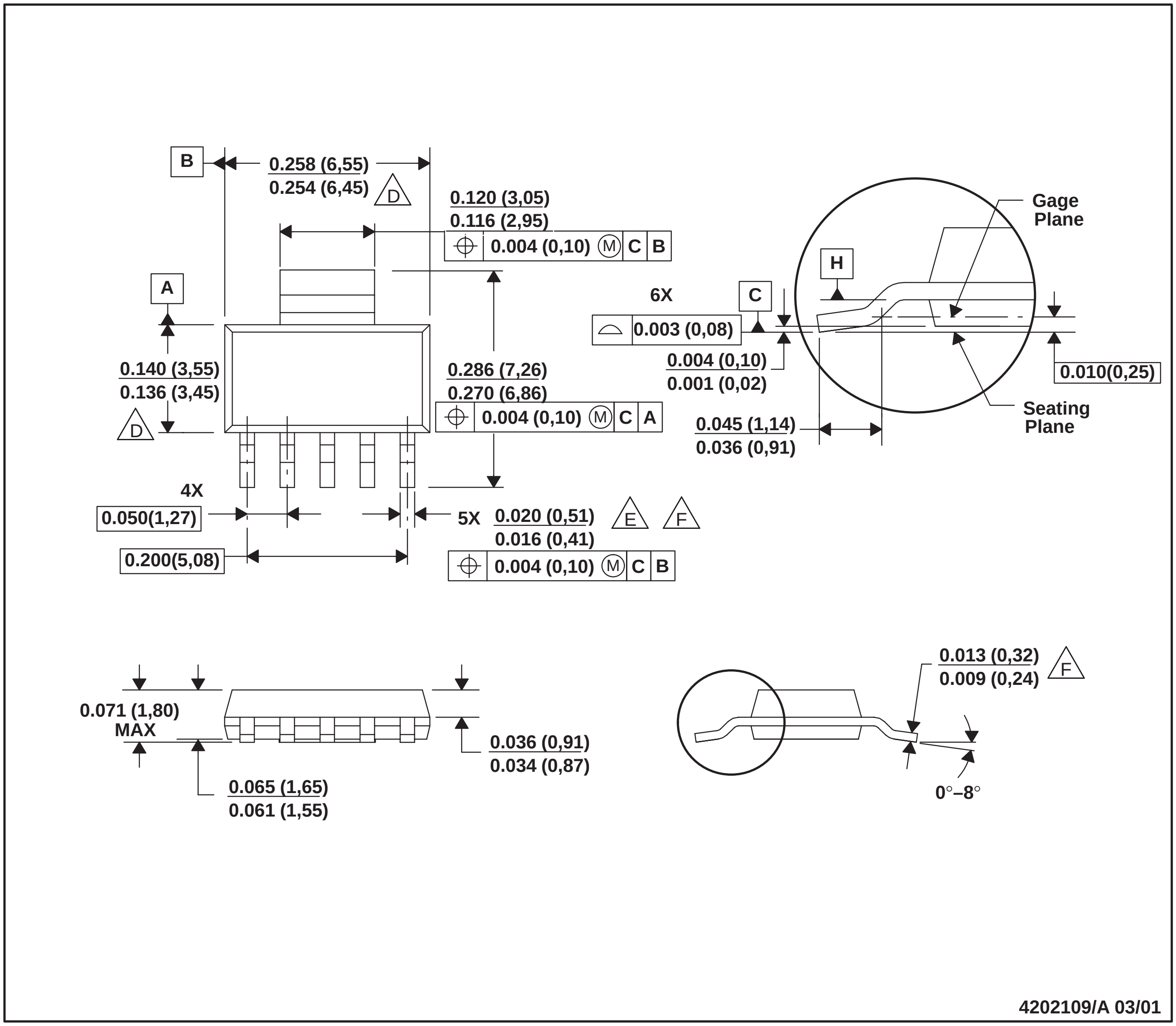
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DCQ (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.
- J. Package dimensions per JEDEC outline drawing TO–261, issue B, dated Feb. 1999. This variation is not yet included.

IMPORTANT NOTICE

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