Infineon Specialty DRAMs

Reduced Latency DRAM

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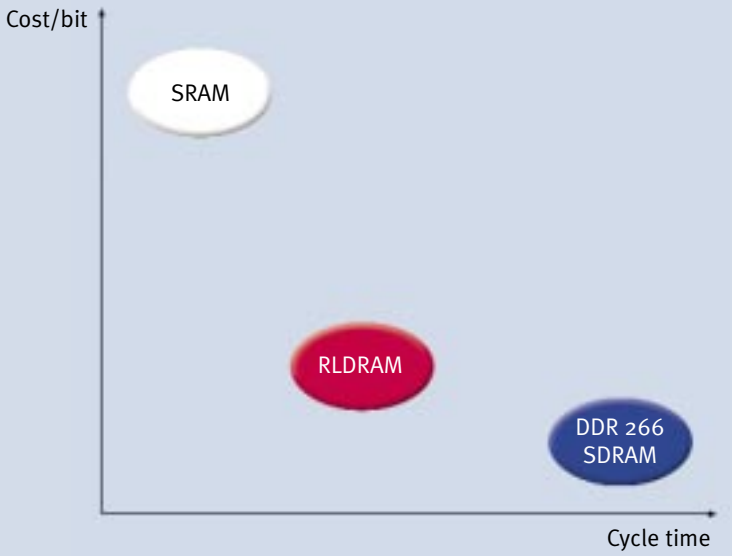
Infineon technologies

Never stop thinking.

RLDRAM – Closing the Gap between SRAM and DRAM

Infineon introduces a new type of high performance memory: the Reduced Latency DRAM (RLDRAM). It combines performance-critical features especially needed in networking and cache applications, such as high density (256M), high bandwidth (2.4 Gbyte/s), and fast SRAM-like random access.

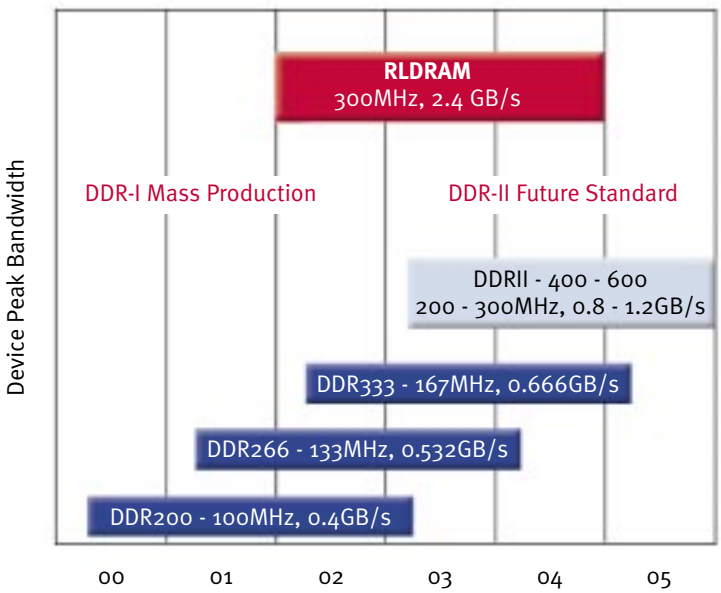
The RLDRAM is a high performance SDRAM operating at 300 MHz clock frequency and using a Double Data Rate (DDR) interface. It is based on a new internal memory architecture which provides for an ultra-fast random access at row cycle times down to 25 ns. Standard DDR SDRAMs operate at row cycle times of 65 ns.



Cost/Performance Comparison

In addition the RLDRAM uses an innovative circuit design to minimize latency. This is the time from the beginning of the access cycle to the availability of the first data. The RLDRAM offers a latency half of the 45 ns for standard DDR SDRAMs.

Minimized latency and reduced row cycle time are ideal for all applications with critical response times and very fast random accesses. All these applications now have an alternative to using Static RAMs: RLDRAM – the ideal solution, combining the speed advantage of SRAM with the cost-efficiency of SDRAM.



RLDRAM: Extremely high Bandwidth

RLDRAM – Innovative Architecture

RLDRAM provides a density of 256Mbit and is offered in two organizations: 8M x 32 and 16M x 16. Its advanced memory architecture and ultra-high operating clock of 300 MHz result in a reduction of latency and row cycle times to less than half of conventional DRAM memories.

By accessing the 8 internal banks in a sequential manner, RLDRAM provides a sustained bandwidth of 2.4 Gbyte/s while still allowing full random access within each bank.

This is primarily achieved by employing an innovative circuit design and doubling the number of internal banks compared to conventional DDR memories.

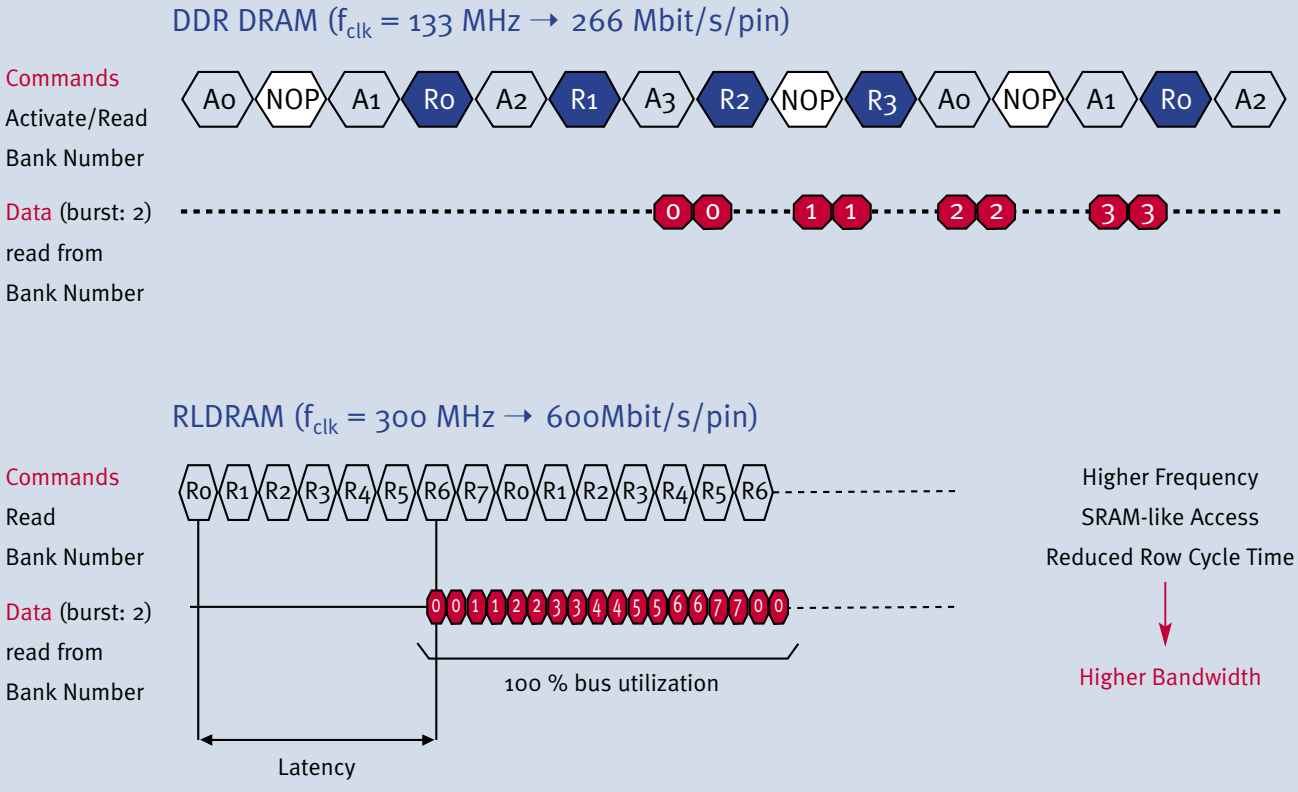
Furthermore RLDRAM offers SRAM-like access: simple read/write commands are issued while the complete address word is asserted at the same time. There is no address multiplexing which saves the usual RAS-CAS delay time of conventional SDRAMs.

The Read Latency can be adjusted for maximum random access speed, which is particularly useful when the RLDRAM is operated at frequencies below 300 MHz.

RLDRAM
REDUCED LATENCY DRAM

- High bandwidth
- Low row cycle time
- Fast random access
- Reduced latency

Random Multi - Bank Access

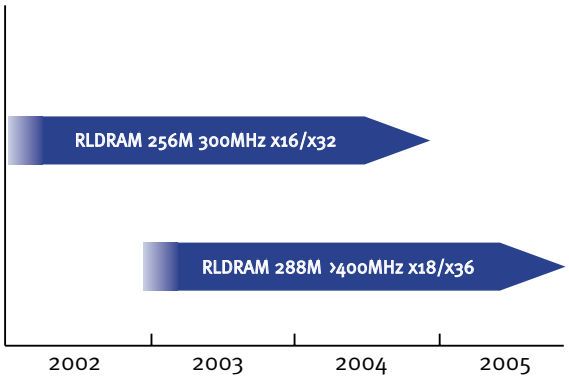


Comparison of random multi-bank Read Accesses between DDR SDRAM and RLDRAM

RLDRAM – Product Portfolio and Roadmap

The 256M RLDRAM will be available in 8M x 32 and 16M x 16 configurations. Volume production will start to ramp early 2002. The next generation RLDRAM will be a 288M device in x18/x36 organizations which will support error-checking applications and operate at clock speeds in excess of 400MHz.

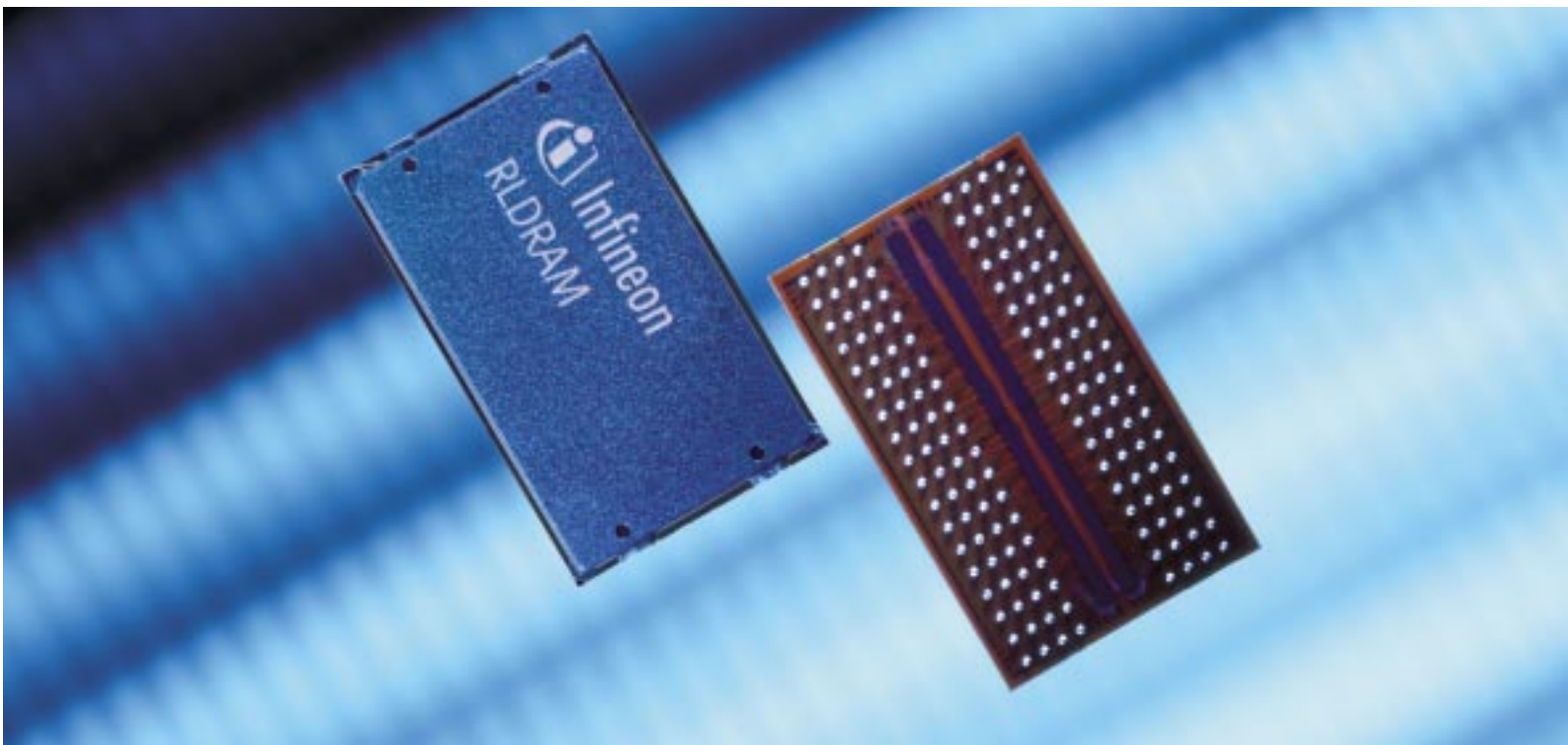
The first RLDRAM will be manufactured using a highly stable 0.17 µm CMOS process. For the next generation RLDRAM, an advanced 0.14 µm process will be used to further push out the performance limits.



RLDRAM Product Roadmap

RLDRAM – Multiple Sources

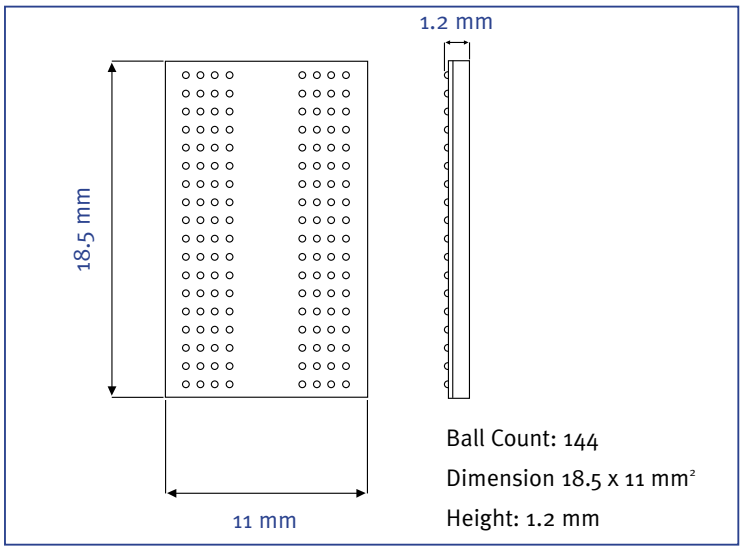
The RLDRAM architecture is a de-facto standard: Infineon Technologies and Micron Technology have committed to the co-development of the RLDRAM product line including a multitude of future generations. Both companies, within the top 5 of the world's DRAM companies, collectively represent the most advanced technologies and a large share of the DRAM market. Infineon and Micron will provide pin- and function-compatible products thus ensuring alternative supply from independent manufacturers.



RLDRAM — Packaging

Infineon has developed a Thin Fine-pitch Ball Grid Array (T-FBGA 144) package that offers reduced parasitics for high frequency operation as well as low thermal resistance for an optimum heat transfer to the printed circuit board and the ambient air.

The footprint of the package is 22% less than that of a standard TSOP 66 package.



T-FBGA 144 Package

RLDRAM — Summary of Key Features

- Density: 256Mbit, organized 8M x 32 and 16M x 16
- 300 MHz Double Data Rate operation (600 Mbit/s/pin)
- Sustained data bandwidth 2.4 Gbyte/s at fully random access
- 8 internal memory banks
- Row cycle time down to 25 ns
- Latency down to 24 ns
- SRAM type interface, non-multiplexed addresses
- Differential echo clocks synchronized with data out
- Programmable read latency for maximum random access speed
- Data Valid signal activated when Read Data available
- Data Mask signals masking write data during first and second part of burst
- Programmable burst length of 2 and 4
- 1.8 V / 2.5V core and 1.8 V I/O
- 144 pin T-FBGA package
- IEEE 1149.1 compatible JTAG boundary scan

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