Rockwell Science Center

RDA014

12 Bit 1 GS/s SiGe DAC

Features

- 12 Bit D/A converter with 1 Gsample/s conversion rate
- 45GHz f_T SiGe BiCMOS process
- Differential output analog
- Power Supply: -3.3V(AVEE, DVEE)
- Input code format: Binary
- Output Spurious Free Dynamic Range: > 65 dB (f_o = 333 MHz, f_{clk} = 1GHz)
- Output Swing: 316 mV @ 50 Ω termination
- Output Power: 0dBm
- ECL Compatible Data Inputs
- 10-bit static linearity
- Fast Settling Time: <1ns 0.1% (+/- 2LSB), switching from code 1536 to 2560 (quarter scale)
- Reference output/input pin for accurate full-scale adjustment.

Product Description

The new current steered 12-bit DAC offers unprecedented performance in terms of both static and dynamic linearity. The DAC uses SiGe BiCMOS process and can be clocked up to 1 GHz. It has been optimized for ultra-high speed and low power performance.

The DAC utilizes a segmented current source to reduce the glitch energy and to achieve high linearity performance. It also uses BiCMOS current switch structure to eliminate beta effect of HBT transistor. For best dynamic performance, the DAC outputs are internally terminated with 50-Ω resistance, and outputs nominal full-scale current of 6.3 mA when terminated with external 50-Ω resistors.

Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, Note	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		12			Bits
Differential Nonlinearity	DNL		-1		1	LSB
Integral Nonlinearity	INL		-2		2	LSB
ANALOG OUTPUTS						
Full-Scale Output Range	V_{FSRS}	Single ended @ 50 Ω	280	316	350	mV
Full-Scale Output Range	V_{FSRD}	Differential @ 50 Ω	560	632	700	mV
Output Current	I_{OUT}		5.6	6.32	7	mA
CLOCK INPUTS						
Type		Differential sine wave				
Clock Input Resistance	R_{CLK}		45	50	55	Ω
Maximum Frequency	FI_{MAX}		500	750	1000	MHz
DATA INPUTS						
Type		Differential ECL				
POWER SUPPLY						
Analog Supply	AVEE	Supply voltage for analog	-3.0	-3.3	-3.6	V
Digital Supply	DVEE	Supply voltage for digital	-3.0	-3.3	-3.6	V
Power Dissipation	P_D		500	750	1000	mW
Output Power	P_O	Single ended @ 50 Ω	-1.06	0	0.88	dBm
OPERATING RANGE			-20		70	°C

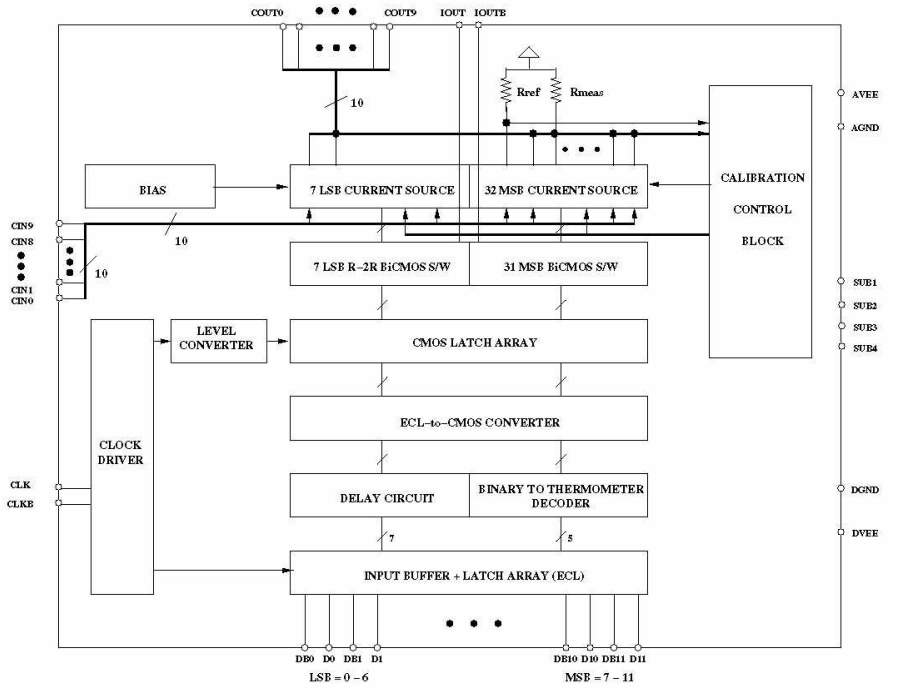
Pad Description

P/I/O	NAME	FUNCTION	P/I/O	NAME	FUNCTION
P	AGND	Analog ground	P	AVEE	-3.3V analog supply
P	DGND	Digital ground	P	DVEE	-3.3V digital supply
P	SUB1	Digital substrate ground	P	SUB2	Analog substrate ground
P	SUB3	Analog substrate ground	P	SUB4	Analog substrate ground
I	D(11:0)	Digital inputs, ECL	I	DB(11:0)	Complementary digital inputs, ECL
I	CLK	Clock input, sine wave	I	CLKB	Complementary clock input, sine wave
O	IOUT	Analog output	O	IOUTB	Complementary analog output
I	CIN(9:0)	Analog input pin for calibration	O	COUT(9:0)	Analog output pin for current monitoring

Theory of Operation

For low power consumption, best dynamic and static performance, the DAC is designed with both CMOS and SIC(Selectively Implanted Collector) SiGe HBT, which is employing 5-bit segmentation. The ECL-compatible 12-bit digital data inputs are latched by a master-slave flip-flop immediately after the input buffer to reduce the data skew. 5 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 7 LSB data bits are transported through a delay equalizer block. The digital data are synchronized again by second master slave flip-flops to reduce the switching glitch. The decoded 5 MSB data drives 31 identical current switches, and the 7 LSB data drives 7 current switches. The output nodes from the LSB current switches are connected to the analog output through R-2R ladder to generate the binary output. Automatic trimming technique is used, so that it can operate in the background continuously to track changing environmental conditions as well as to correct the systematic and random component variations within the chip

Block Diagram



Typical Operating Circuit