Rockwell Science Center

RDA012M4

12-Bit, 1.3 Gsample/s MUX DAC

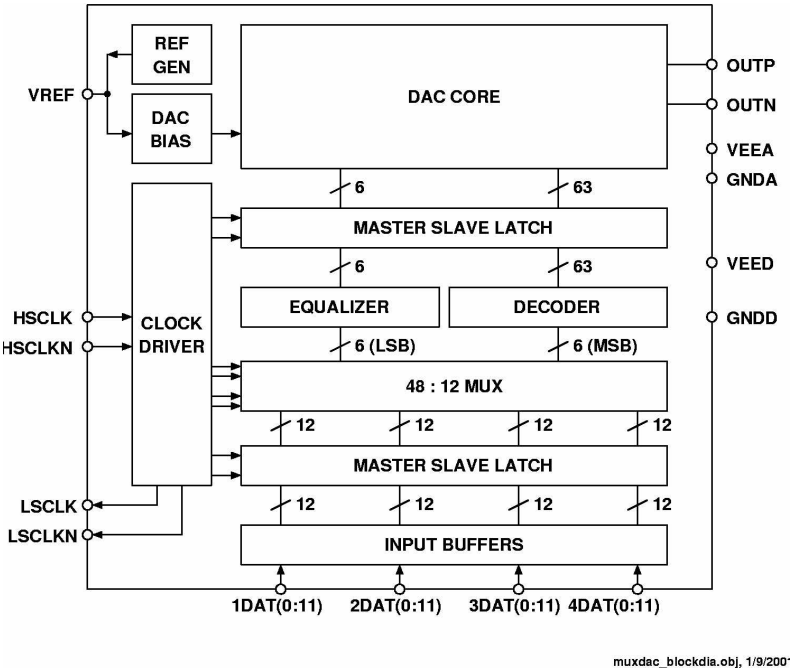
Features

- 12-Bit D/A converter with 1.3 Gsample/s conversion rate
- 80GHz f_T GaAs HBT process
- Differential Analog Output
- Power Supplies: -5.2V ± 0.3V, 3.3 ± 0.3V
- Input code format: Offset Binary
- 4:1 Input Multiplexer
- Output Swing: 600 mV @ 50 Ω termination
- 3.3V NMOS-Compatible Data Inputs
- Differential ECL or Sinusoidal Clock Input
- LVDS Compatible Clock Output
- 10-bit static linearity
- Fast Settling Time: <1ns 0.1% (+/- 2LSB), switching from code 1536 to 2560 (quarter scale)
- Reference output/input pin for accurate full-scale adjustment.

Product Description

The RDA012M4 is a 12-bit GaAs MUX DAC with a data update rate over 1Gsample/s. It has been optimized for ultra-high speed applications. The DAC utilizes a segmented current source to reduce the glitch energy and to achieve high linearity performance. For best dynamic performance, the DAC outputs are internally terminated with 50-Ω resistance, and outputs a nominal full-scale current of 12mA when terminated with external 50-Ω resistors. For a convenient interface with most CMOS ICs, a 48:12 multiplexer is integrated, and the digital data inputs are low voltage NMOS compatible.

Block Diagram



Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, Note	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution	RES		12			Bits
Differential Nonlinearity	DNL		-1		1	LSB
Integral Nonlinearity	INL		-2.5		2.5	LSB
Spurious Free Dynamic Ranges (See note1)						
	SFDR1	F_{clk} = 650MHz	65			dBc
	SFDR2	F_{clk} = 800MHz	60	65		dBc
	SFDR3	F_{clk} = 1000MHz	55			dBc
	SFDR4	F_{clk} = 1300MHz	50			dBc
ANALOG OUTPUT						
Full-Scale Output Range	V_{FSRS}	Single ended @ 50 Ω		600		mV_{p-p}
Full-Scale Output Range	V_{FSRD}	Differential @ 50 Ω		1200		mV_{p-p}
Output Current	I_{OUT}	See notes 2, 3	11.4	12.0	12.6	mA
CLOCK INPUTS (HSCLK)						
Type		Differential ECL or differential sinusoidal				
Clock Input Common Mode Voltage	$V_{IC,CLK}$	Differential ECL or differential sinusoidal	-0.8	-1.5	-2.0	V
Clock Input Differential Voltage	$V_{ID,CLK}$	Differential ECL or differential sinusoidal	0.4	0.6	0.8	V
Clock Input Resistance	R_{CLK}	Individual termination resistance to the VTT pin	45	50	55	Ω
Maximum Frequency	FI_{MAX}		1300			MHz
Minimum Frequency	FI_{MIN}				1	MHz
CLOCK OUTPUT (LSCLK)						
Type		LVDS compliant				
Clock Output Common Mode Voltage	$V_{OC,CLK}$	RL = 100 Ω	0.9	1.2	1.5	V
Clock Output Differential Voltage	$V_{OD,CLK}$	RL = 100 Ω	±0.25	±0.35	±0.45	V
Maximum Frequency	FO_{MAX}		325			MHz
Minimum Frequency	FO_{MIN}				0.25	MHz
DATA INPUTS						
Data Input Level		3.3V NMOS compliant				
Input High Voltage	V_{IH}		+1.4	+2.0	+3.5	V
Input Low Voltage	V_{IL}		-0.4	0	+0.4	V
Data Input Setup Time	t_s	See note 4	300			ps
Data Input Hold Time	t_h	See note 4	-50			ps
POWER SUPPLY						
Positive Supply	VCC		+3.14	+3.3	+3.47	V
Negative Supply	VEED, VEEA		-5.46	-5.2	-4.94	V
Power Dissipation, Positive Supply	P_{VCC}			300		mW
Power Dissipation, Negative Supply	P_{VEE}			3100		mW
OPERATING RANGE	T_A	See note 5	-40		85	°C

Note 1. The measured spurious free dynamic range is defined as maximum spurious for a single output measured over the frequency band 1/8 f_{clk} - 3/8 f_{clk} with the output frequency equal to 1/4 or 1/3 f_{clk} + 5MHz, with internal reference.

2. The DAC current is generated from an internal reference that is both temperature and supply dependent. Internal reference can change up to ±2% by changing the supply voltage within the specified range, and also can change up to ±5% according to operating temperature changes.
3. The change in temperature and supply can be minimized by using a precision external voltage reference source with an additional pin. Refer the operating diagram in page 5.
4. Setup and hold time are measured with respect to the LSCLK signal at the driver side. Refer to the signal description section in page 6.
5. The part is designed to function within -55 ~ 125°C temperature range. For the best performance, operation within the specified temperature range with a proper heat sink attached to the device is recommended.

Pin Description

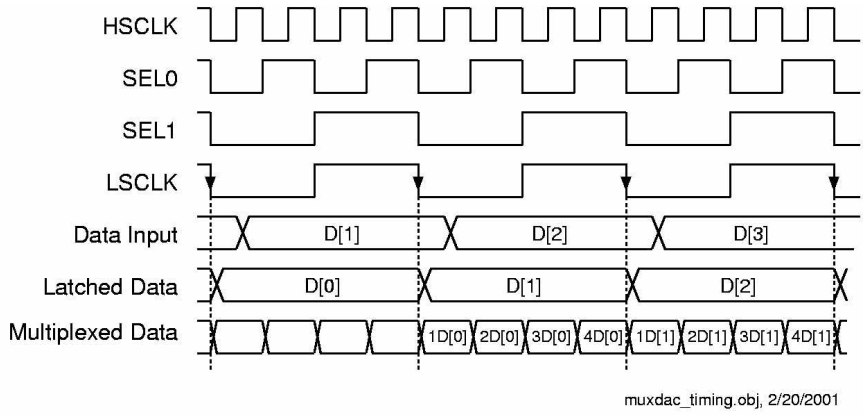
P/I/O	NAME	FUNCTION	P/I/O	NAME	FUNCTION
P	GNDA	Analog ground.	P	VEEA	-5.2V analog supply
P	GNDD	Digital ground.	P	VEED	-5.2V digital supply
I	HSCLK	DAC clock input, LVDS / ECL	I	HSCLKN	Complementary DAC clock input, LVDS/ECL
O	LSCLK	Data clock output, LVDS	O	LSCLKN	Complementary data clock output, LVDS
I/O	VREF	-2V Reference voltage input / bypass pin.	I	VTT	Termination node for HSCLK and HSCLKN
I	1DAT(0:11)	Digital data, 1st channel. 1DAT(11) is the MSB, 1DAT(0) is the LSB.	I	2DAT(0:11)	Digital data, 2nd channel. 2DAT(11) is the MSB, 2DAT(0) is the LSB.
I	3DAT(0:11)	Digital data, 3rd channel. 3DAT(11) is the MSB, 3DAT(0) is the LSB.	I	4DAT(0:11)	Digital data, 4th channel. 4DAT(11) is the MSB, 4DAT(0) is the LSB.
O	OUT	Analog output	O	OUTN	Complementary analog output

Theory of Operation

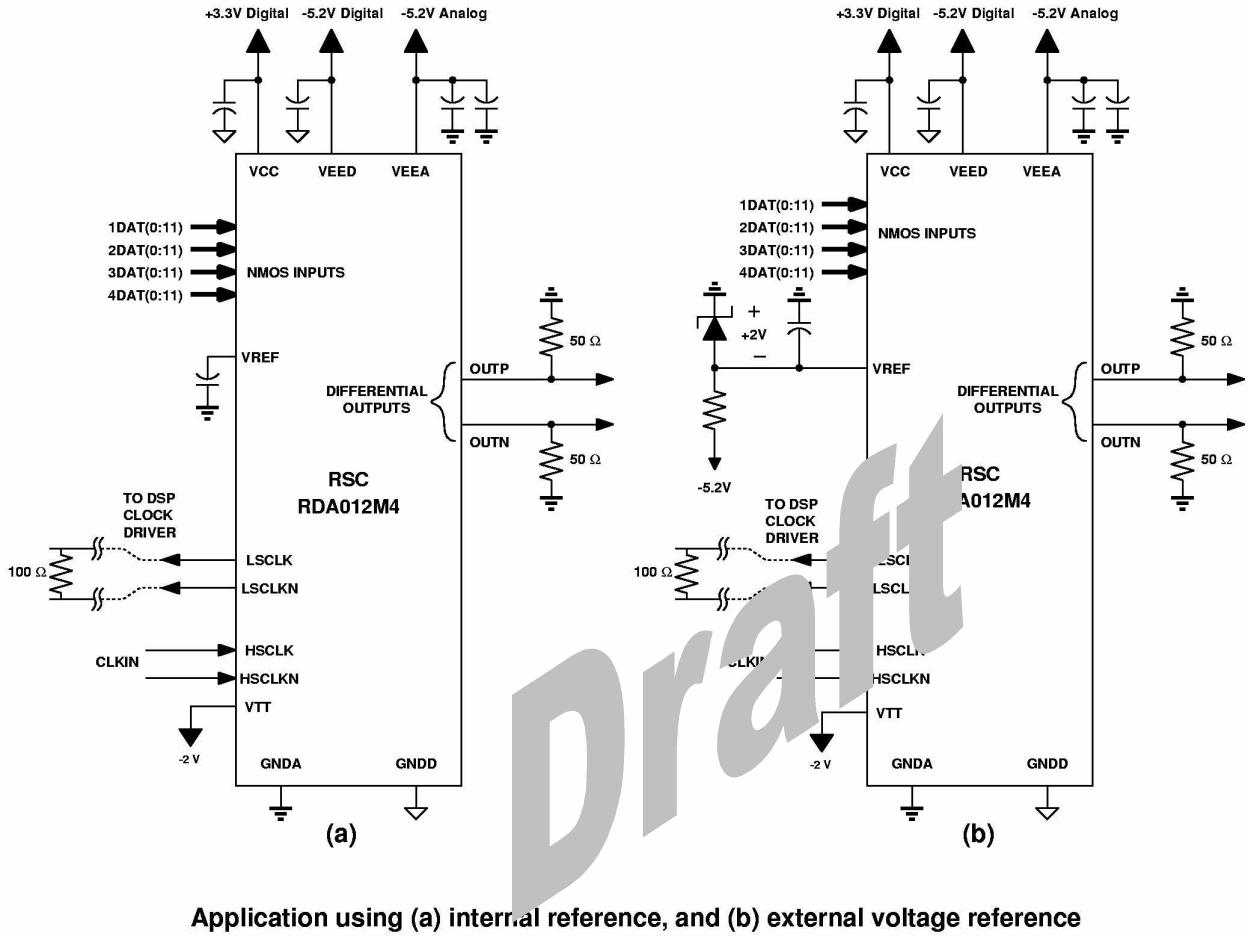
For best dynamic and static performance, the DAC employs 6-bit segmentation. The 3.3V NMOS compatible 12-bit digital data inputs are latched by master-slave flip-flop immediately after the input buffer to reduce the data skew. The four-channel data are combined together by the 48:12 MUX and latched again. 6 MSB data bits are decoded into thermometer code by a two-stage decoding block, and the 6 LSB data bits are transported through the delay equalizer block. The digital data are synchronized again by a second master slave flip-flop to reduce the switching glitch. The decoded 6 MSB data drives 63 identical current switches, and the 6 LSB data drives 6 current switches. The output nodes from the LSB current switches are connected to the analog output through R-2R ladder to generate the binary output.

The DAC output full-scale voltage follows the relationship $V_{FS} = 0.3xV_{REF.}$ An internal reference circuit with approximately -10dB supply rejection is integrated on chip for application convenience, and the reference pin is provided for monitoring and for bypass purposes. To band-limit the noise on the reference voltage, the reference pin should be bypassed to the GNDA node with capacitance > 100pF. The VREF pin can also be used to override the internal reference with an accurate, temperature-compensated external voltage reference.

The timing diagram is shown in the figure below. The 1.3GHz external clock (HSCLK) is divided by 2 and 4 resulting in the MUX selection signal SEL0 and SEL1. A low-speed clock (LSCLK) is provided to drive the external digital. The four-channel data input are latched with an internal clock that is synchronized with the LSCLK. Controlled by the SEL0 and SEL1, input data are fed to the 1.3GS/s DAC in the order shown.



Typical Operating Circuit



Application using (a) internal reference, and (b) external voltage reference

Signal Descriptions

INPUT CLOCK

The RDA012M4 clock inputs can be driven from typical ECL circuits. Also a differential sinusoidal clock can be used to drive the DAC. A differential clock should be provided to the HSCLK and HSCLKN inputs, which are internally terminated with 50 Ω. The VTT pin is the termination node for both HSCLK and HSCLKN, and should be connected to a well de-coupled –2.0 volt supply. Since the DAC's output phase noise is directly related to the input clock noise and jitter, a low-jitter clock source should be used to drive the clock input. The internal clock driver generates very little added jitter (~100fs) to the internal clock, and the incoming clock signal's spectral purity needs to be guaranteed to take advantage of the low-noise clock driver circuit inside. A 500MHz DAC output demands a white noise induced clock jitter of less than 250fs for a 10-bit equivalent, 62dB SNDR.

DATA INPUT

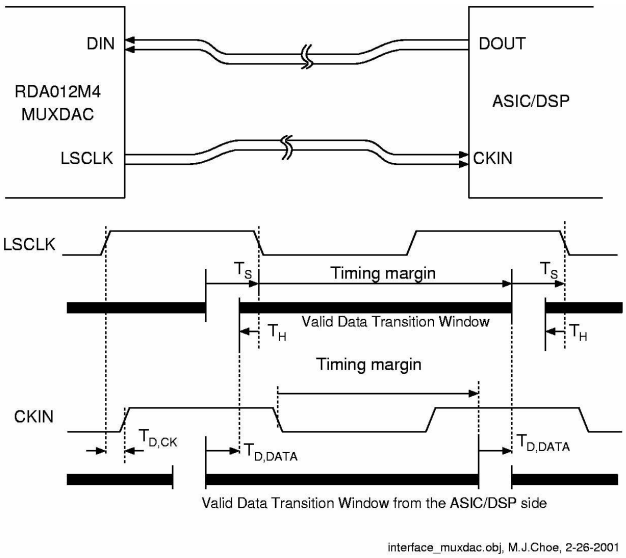
The data inputs are 3.3V NMOS-compatible. Four-channel input needs to be provided to the DAC in subsequent order. 1DAT(0:11) is taken first, and 4DAC(0:11) is taken last.

OUTPUT CLOCK

Output clock LSCLK and LSCLKN are supplied for the DSP and other application ICs that provides the digital input for the DAC. It is LVDS compliant and needs to be terminated with a 100Ω resistor in front of the clock driver for the ASIC/DSP.

For application convenience, the data input's setup- and hold time is specified with respect to the LSCLK. It should be noted that LSCLK and LSCLKN are driven by the MUXDAC and the waveforms of these signals are better defined at the receiver end; that is, near the ASIC/DSP chip that provides the input data for the MUXDAC. The system designer should consider of the delay associated with the signal routing in the system's timing budget.

In the following example, the setup and hold time of the LSCLK to data transition are defined at the MUXDAC side. Data transitions of the data input have to occur during the "Valid Data Transition Window." The timing margin seen from the MUXDAC is T_P-T_S where T_P is the LSCLK period and T_S is the setup time, assuming that the ASIC chip takes LSCLK as the clock input and its outputs are latched at the falling edge of the clock. However from the ASIC/DSP end, the timing margin is decreased by the amount equal to the sum of the data delay and clock delay between the two chips, as noted in the lower part of the diagram.



ANALOG OUTPUT

The outputs OUT and OUTN should both be connected though a 50 Ω resistor to ground. This will give a full-scale amplitude of 0.6 volt (both outputs must be terminated), 1.2 volt differentially. Output common mode can be changed by terminating the load resistors to a different voltage. However, the device is optimized to perform best when connected to a voltage between 0 and 1 volt. Also, for reliable operation, the output termination voltage should not exceed 3 volts.

REFERENCE

VREF is provided for added control over the full-scale of the DAC. The internal reference circuit is designed to provide -2.0 volt, which can change up to ±5% as the supply voltage and/or operating temperature changes. If the user prefers accurate absolute full-scale, one can use external voltage reference with low output impedance to override the internal reference. Note that the DAC is optimized to have the best performance with a reference voltage of -2.0 volt. The output resistance of the reference node is 560 Ω ±10%.