

# RC7315

## Three-State ATE Pin Electronics Driver

### Features

- High output slew rate (1.8 V/ns typical)
- Wide output voltage range (-2.5V to +7V), and up to 9.5 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (20 mV typical) and output offset drift (0.1 mV/°C typical).
- Low leakage (10 nA typical) and low output capacitance (3 pF typical) in high impedance inhibit mode
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- 100 mA typical dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC
- Packaged parts available in unterminated configurations

### Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

### Description

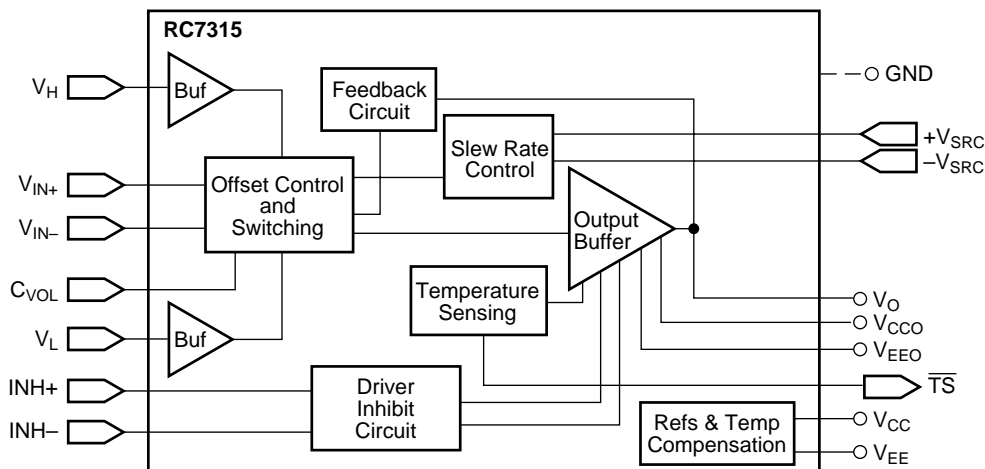
The RC7315 Pin Electronics Driver is designed for use in all high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7315 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 1.8 V/ns and repetition rate of over 250 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -2.5V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins  $V_H$  and  $V_L$ , respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The  $V_H$  and  $V_L$  inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7315 is used on an I/O pin, it may be forced into the high impedance state through the  $INH+$  and  $INH-$  differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

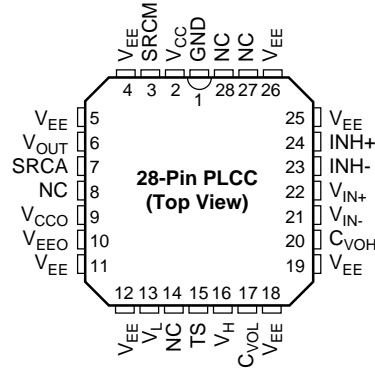
The RC7315 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is fed to the appropriate threshold value.

The RC7315 is implemented using Fairchild Semiconductor's high frequency complementary bipolar process.

### Block Diagram



## Pin Assignments



## Pin Description

Name	Pin Number	Function
$C_{VOL}$ , $C_{VOH}$	17	<b>Bypass capacitor for <math>V_{OH}</math> and <math>V_{OL}</math> respectively.</b> Pins $C_{VOL}$ and $C_{VOH}$ should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1	<b>Chip ground.</b> Should be connected to the printed circuit board's ground plane at the pin.
INH+ INH-	23, 24	<b>Differential digital inputs.</b> When INH is true (i.e. $INH+ > INH-$ ) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
SRCA	7	<b>Slew rate control for both edges.</b> Slew rate of both rising and falling edges decreases as the control current is changed from 0 mA to -0.5 mA. SRC can be programmed with a current DAC or set to a fixed value using a resistor.
SRCM	3	Increases the speed of the falling edge to match the rising edge.
$\overline{TS}$	15	<b>Active low output notifies thermal shutdown has occurred.</b> In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{TS}$ is an open collector output capable of driving two standard TTL loads. The $\overline{TS}$ pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
$V_{CC}$	2	<b>Quiet positive supply.</b> The nominal value is 10V $\pm$ 3%. For output high voltage levels ( $V_{OH}$ ) greater than the nominal value of +7V, $V_{CC}$ should be raised 3V above the maximum value of $V_{OH}$ . Whenever $V_{EE}$ is lowered to provide margin at the output low level, $V_{CC}$ should also be lowered by the same amount. $V_{CC}$ should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
$V_{CCO}$	9	<b>Positive supply for the RC7315 output stage.</b> This supply is brought out separately to minimize the supply noise generated when the output switches. $V_{CCO}$ should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to $V_{CC}$ .
$V_{EE}$	4, 5, 11, 12, 18, 19, 25, 26	<b>Quiet negative supply.</b> The nominal value is -5.2V $\pm$ 5%. For output low voltage levels ( $V_{OL}$ ) less than the nominal value of -2.2V, $V_{EE}$ should be lowered 3V below the minimum value of $V_{OL}$ . Whenever $V_{CC}$ is raised to provide margin at the output high level, $V_{EE}$ should also be raised by the same amount. $V_{EE}$ should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.

## Pin Descriptions (continued)

Name	Pin Number	Function
V <sub>EE0</sub>	10	<b>Negative supply for the RC7315 output stage.</b> This supply is brought out separately to minimize the supply noise generated when the output switches. V <sub>EE0</sub> should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V <sub>EE</sub> .
V <sub>H</sub>	16	Analog program input that sets the output high level (V <sub>OH</sub> ). The transfer characteristic from V <sub>H</sub> to V <sub>OH</sub> is nominally unity gain.
V <sub>IN+</sub> , V <sub>IN-</sub>	21, 22	<b>Differential digital inputs.</b> The output will toggle between the two levels dictated by V <sub>H</sub> and V <sub>L</sub> as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V <sub>L</sub>	13	Analog program input that sets the output low level (V <sub>OL</sub> ). The transfer characteristic from V <sub>L</sub> to V <sub>OL</sub> is nominally unity gain.
V <sub>O</sub>		<b>Driver output on RC7315.</b> The output impedance is 8Ω ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω ±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8W to sustain the short circuit current of the output.
NC	8, 14, 27, 28	<b>No connection.</b>

## Absolute Maximum Ratings<sup>1</sup>

Parameter	Min.	Max.	Units
Positive power supply, V <sub>CC</sub>		13	V
Negative power supply, V <sub>EE</sub>	-8.2		V
Difference between V <sub>CC</sub> and V <sub>EE</sub>		17	V
Input voltage at V <sub>IN+</sub> , V <sub>IN-</sub> , INH+, and INH-	V <sub>CC</sub> -12	V <sub>EE</sub> +12	V
Input Voltage at V <sub>H</sub> , V <sub>L</sub>	V <sub>CC</sub> -13	V <sub>EE</sub> +13	V
Differential input voltage,  V <sub>IN+</sub> - V <sub>IN-</sub>  ,  V <sub>INH+</sub> - V <sub>INH-</sub>		6	V
Difference between V <sub>H</sub> & V <sub>L</sub> ( V <sub>H</sub> - V <sub>L</sub>  )		11	V
Input voltage at SRCA	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V <sub>CC</sub> -13	V <sub>EE</sub> +13	V
Output voltage at $\overline{\text{TS}}$		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

## Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T <sub>C</sub>	Case operating temperature		25		°C
V <sub>CC</sub>	Positive supply voltage	9.7	10.0	10.3	°C
V <sub>EE</sub>	Negative supply voltage	-5.45	-5.2	-4.95	V
V <sub>CC</sub> -V <sub>EE</sub>	Difference between positive and negative supply		15.2	15.8	V
V <sub>OH</sub> , V <sub>OL</sub>	Range for output high level and output low level	-2.0		7.0	V
V <sub>OH</sub> -V <sub>OL</sub>	Output amplitude	0.1		10.0	V

## DC Electrical Characteristics

V<sub>CC</sub> = 10V ±3%, V<sub>EE</sub> = -5.2V ±5%, T<sub>A</sub> = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
<b>Differential Inputs V<sub>IN+</sub>, V<sub>IN-</sub>, V<sub>INH+</sub>, V<sub>INH-</sub></b>						
V <sub>IN+</sub> , V <sub>IN-</sub>	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V <sub>INH+</sub> , V <sub>INH-</sub>	Absolute Voltage @ Inhibit Inputs INH+, INH-		-2.0		+6.0	V
V <sub>ID</sub>	Differential Input Range	V <sub>IN+</sub> - V <sub>IN-</sub>	0.4	ECL	5.0	V
V <sub>DINH</sub>	Differential Inhibit Input Range	V <sub>INH+</sub> - V <sub>INH-</sub>	0.4	ECL	5.0	V
I <sub>IN+</sub> , I <sub>IN-</sub>	Input Bias Current @ Data Inputs	-2V ≤ V <sub>IN+</sub> , V <sub>IN-</sub> ≤ +6V		-100		μA
I <sub>INH+</sub> , I <sub>INH-</sub>	Input Bias Current @ Inhibit Inputs	-2V ≤ V <sub>INH+</sub> , V <sub>INH-</sub> ≤ +5V		-100		μA
<b>Absolute Slew Rate Control Input SRCA</b>						
V <sub>SRCA</sub>	Compliance Voltage Range		-2.0		+2.0	V
I <sub>SRCA</sub>	Control Current Range		-0.5		+0.5	V
<b>Matching Slew Rate Control Input SRCM</b>						
V <sub>SRCM</sub>	Compliance Voltage Range		-2.0		+2.0	V
I <sub>SRCM</sub>	Control Current Range		-0.5		+0.5	V
<b>Voltage Program Inputs V<sub>H</sub>, V<sub>L</sub></b>						
V <sub>H</sub>	V <sub>H</sub> Range	V <sub>CC</sub> = 10V; V <sub>EE</sub> = -5.2V	-2.0		+7.0	V
		V <sub>CC</sub> = 12V; V <sub>EE</sub> = -3.2V	0		+9.0	V
		V <sub>CC</sub> = 8V; V <sub>EE</sub> = -7.2V	-4.0		+5.0	V
V <sub>L</sub>	V <sub>L</sub> Range	V <sub>CC</sub> = 10V; V <sub>EE</sub> = -5.2V	-2.5		+6.0	V
		V <sub>CC</sub> = 12V; V <sub>EE</sub> = -3.2V	-0.5		+8.0	V
		V <sub>CC</sub> = 8V; V <sub>EE</sub> = -7.2V	-4.5		+4.0	V
I <sub>H</sub>	Bias Current @ V <sub>H</sub>	-1V ≤ V <sub>H</sub> ≤ +7V; V <sub>L</sub> = -2.0V		-1		μA
I <sub>L</sub>	Bias Current @ V <sub>L</sub>	-2V ≤ V <sub>L</sub> ≤ +5V; V <sub>H</sub> = 6.0V		-1		μA
TCI <sub>H</sub>	Temperature Drift in I <sub>H</sub>	V <sub>H</sub> = 7.0V; 25°C ≤ T <sub>C</sub> ≤ 70°C output not switching			0.1	μA/°C
TCI <sub>L</sub>	Temperature Drift in I <sub>L</sub>	V <sub>L</sub> = -2.0V; 25°C ≤ T <sub>C</sub> ≤ 70°C output not switching			0.1	μA/°C
V <sub>H,L</sub> BW	-3 dB bandwidth from V <sub>H</sub> or V <sub>L</sub> to the output	-1V ≤ V <sub>H</sub> ≤ +7V; -2V ≤ V <sub>L</sub> ≤ +6V; V <sub>H</sub> -V <sub>L</sub> = 2.0V		50		kHz

**DC Electrical Characteristics** (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
<b>Signal Output <math>V_O</math>, <math>V_{OTERM}</math></b>						
$V_O$	Output Voltage Range	$V_{CC} = 10V$ ; $V_{EE} = -5.2V$ $V_{CC} = 12V$ ; $V_{EE} = -3.2V$ $V_{CC} = 8V$ ; $V_{EE} = -7.2V$	-2.5 -0.5 -4.5		+7.0 +9.0 +5.0	V V V
$V_A$	Amplitude	$ V_{OH} - V_{OL} $	0.3		9.5	V
$\delta V_{OH}$	Offset to Output High Level	$V_H = 0$ , no load; $V_L = -2V$ $\delta V_{OH} =  V_H - V_{OH} $		$\pm 30$		mV
$\delta V_{OL}$	Offset to Output Low Level	$V_H = 0$ , no load; $V_H = +7V$ $\delta V_{OL} =  V_L - V_{OL} $		$\pm 30$		mV
VTC	Output Voltage Drift	$-1V \leq V_{OH} \leq +7V$ ;		0.1		mV/°C
		$-2V \leq V_{OL} \leq +6V$ ;		0.1		
$\varepsilon_G$	Gain Error	$-1V \leq V_{OH} \leq +7V$ ;		1	2	% $V_{SET}$
		$-2V \leq V_{OL} \leq +6V$		1		
$\varepsilon_L$	Linearity Error	$-2V \leq V_{OUTPUT} \leq +7$		0.7		% $V_{SET}$
$Z_{OUT}$	Output Impedance $I_{OUT} 50\text{ mA}$	$V_O$		8		$\Omega$
$I_{ZL}$	Output Leakage Current in Inhibit Mode	$-2.0V \leq V_O \leq +7V$		0.5	2	$\mu A$
$I_{DC}$	DC Current Drive		50			mA
$I_{AC}$	AC Current Drive		70	100		mA
<b>Thermal Shutdown Output (TS)</b>						
$I_{CL}$	Short Circuit Current Limit				145	mA
VTS	TS Flag Output Level	$I_{OL} = 4\text{ mA}$			0.5	V
$T_{TS}$	Shutdown Die Temperature			145		°C
<b>Other</b>						
$V_{S\text{ MAX}}$	Maximum Rail to Rail Supply Voltage	$V_{CC} - V_{EE}$			16	V
$V_{CC}$	Positive Supply		+8.0	+10.0	+12.0	V
$V_{EE}$	Negative Supply		-7.2	-5.2	-3.2	V
$I_{CC}$	Positive Supply Current			85		mA
$I_{EE}$	Negative Supply Current			90		mA
PSRV <sub>O</sub>	Output Level Power Supply Rejection Ratio	$V_{CC}$ ; $\Delta V_{CC} = \pm 2.5\%$	40			dB
		$V_{EE}$ ; $\Delta V_{EE} = \pm 2.5\%$	40			dB
PSRV <sub>SL</sub>	Output Slew Rate Power Supply Rejection Ratio @ $V_{CC}$ @ $V_{EE}$	$V_H = 5V$ and $V_L = 0V$		4 4		%
		$\Delta V_{CC} = \pm 200\text{ mV}$ $\Delta V_{EE} = \pm 200\text{ mV}$				
$T_A$	Operating Temperature Range	Still Air	0	25	40	°C
		Air Flow > 300 l <sub>fpm</sub>	0	25	70	°C

## AC Electrical Characteristics

$V_{CC} = 10V \pm 3\%$ ,  $V_{EE} = -5.2V \pm 5\%$ ,  $T_A = 25^\circ C$  (still air) and the load is a  $50\Omega$  transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in  $50\Omega$  ( $\pm 5\%$ ) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 k $\Omega$ .

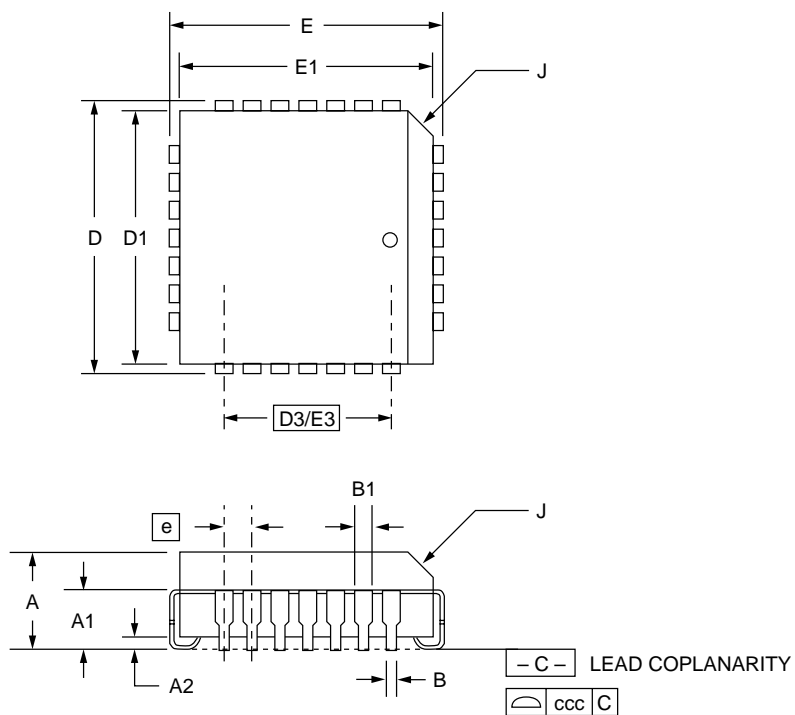
Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate (Slew rate not adjusted)	$V_H - V_L = 5V$ ; Measured between 20% and 80% points. With probe only as load	1.3	1.8		V/ns
		With probe and transmission line	1.2	1.7		V/ns
$t_R$ , $t_F$	Rise Time, and Fall Time (Slew rate not adjusted)	Load is Probe Only;				
		$V_A = 1V$ (20% to 80%)		0.6		ns
		$V_A = 3V$ (10% to 90%)		1.6		ns
f	Toggle Rate	$V_A = 5V$ (10% to 90%)		2.5		ns
		Amplitude = 0.8 Vp-p	250			MHz
$t_{PLH}$	Low to High Propagation Delay	Amplitude = 5.0 Vp-p	125			MHz
		f = 10 MHz; $V_{OH} = +0.4V$ ; $V_{OL} = -0.4V$		1.6		ns
$t_{PHL}$	High to Low Propagation Delay	f = 10 MHz; $V_{OH} = +0.4V$ ; $V_{OL} = -0.4V$		1.4		ns
$\Delta t_p$	Propagation Delay Match	$ t_{PLH} - t_{PHL} $		200		ps
$t_{pTC}$	Propagation Delay Temperature Coefficient			2		ps/ $^\circ C$
$t_{PW_{min}}$	Minimum Pulse Width	$V_H - V_L = 2.0V$ ; pulsewidth at which amplitude drops by 50 mV, measured between 50% points.		2.0		ns
$\Delta t_{pPW}$	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; $V_{OH} = +0.4V$ ; $V_{OL} = -0.4V$		$\pm 75$		ps
$t_{PS}$	Preshoot	$0.5V < V_A < 5.0V$			15mV + 3% of $V_A$	
$t_{OS}$	Overshoot	$0.5V < V_A < 5.0V$			50mV + 4% of $V_A$	
$t_S$	Output Settling Time	$V_A < 5V$ ; To within 3% of $V_A$		8		ns
		To within 1% of $V_A$		10		ns
$t_{PHZ}$	Propagation Delay from Logic High to Inhibit Mode	$V_{OH} = 1V$ ; $V_{OL} = -1V$ Load = 100 $\Omega$ // 15pF		2.9		ns
$t_{PLZ}$	Propagation Delay from Logic Low to Inhibit Mode	Propagation delay is measured to the point at which voltage has changed by 200 mV.		2.9		ns
$t_{PZH}$	Propagation Delay from Inhibit Mode from Logic High			2.9		ns
$t_{PZL}$	Propagation Delay from Inhibit Mode to Logic Low			2.9		ns
$C_Z$	Output capacitance in Inhibit Mode			3		pF

## Mechanical Dimensions — 28-pin PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

### Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)



## Ordering Information

Part Number	Package	Operating Temperature Range
RC7315QF	28-pin PLCC	0°C to +70°C

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.