FAIRCHILD SEMICONDUCTOR TM

RFP15N08L

Data Sheet | **June 1999** | **File Number 2840.1**

15A, 80V, 0.140 Ohm, Logic Level, N-Channel Power MOSFET

The RFP15N08L is an N-Channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

Formerly developmental type TA09804.

Ordering Information

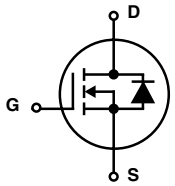
PART NUMBER	PACKAGE	BRAND
RFP15N08L	TO-220AB	RFP15N08L

NOTE: When ordering, use the entire part number.

Features

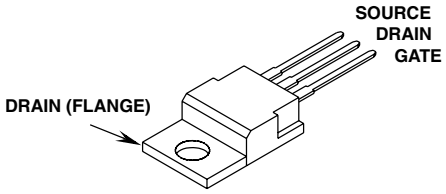
- 15A, 80V
- $r_{DS(ON)} = 0.140\Omega$
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly from Q-MOS, N-MOS, TTL Circuits
- SOA is Power Dissipation Limited
- $175^{o}C$ Rated Junction Temperature
- Logic Level Gate
- High Input Impedance
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFP15N08L	UNITS
Drain to Source Breakdown Voltage (Note 1)	V_{DS}	80	V
Drain to Gate Voltage (Note 1)	V_{DGR}	80	V
Gate to Source Voltage	V_{GS}	±10	V
Continuous Drain Current	I_D	15	A
Pulsed Drain Current (Note 3)	I_{DM}	40	A
Maximum Power Dissipation	P_D	72	W
Derated above 25^oC		0.48	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 1mA, V_{GS} = 0V		80	-	-	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 1mA		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$T_C = 25^oC$, V_{DS} = 65V, V_{GS} = 0V		-	-	1	µA
		$T_C = 125^oC$, V_{DS} = 65V, V_{GS} = 0V		-	-	50	µA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±10V, V_{DS} = 0V		-	-	±100	nA
Drain to Source On Voltage	$V_{DS(ON)}$	I_D = 7.5A, V_{GS} = 5V		-	-	1.05	V
		I_D = 15A, V_{GS} = 5V		-	-	3.0	V
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 7.5A, V_{GS} = 5V		-	-	0.140	Ω
Forward Transconductance	$V_{(plateau)}$	V_{DS} = 15V, I_D = 15A		-	-	4.5	V
Turn-On Delay Time	$t_{d(ON)}$	V_{DD} = 40V, I_D = 7.5A, R_{GS} = 6.25Ω, V_{GS} = 5V		-	-	40	ns
Rise Time	t_r			-	-	325	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	325	ns
Fall Time	t_f			-	-	325	ns
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	V_{GS} = 0-10V	V_{DD} = 64V, I_D = 15A, R_L = 4.27Ω	-	-	80	nC
Gate Charge at 5V	$Q_{g(5)}$	V_{GS} = 0-5V		-	-	45	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0-1V		-	-	3	nC
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	2.083	$^oC/W$

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 7.5A	-	-	1.4	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 4A, dI_{SD}/dt = 100A/µs	-	225	-	ns

NOTES:

2. Pulsed: pulse duration = ≤ 300µs maximum, duty cycle = ≤ 2%.
3. Repititive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

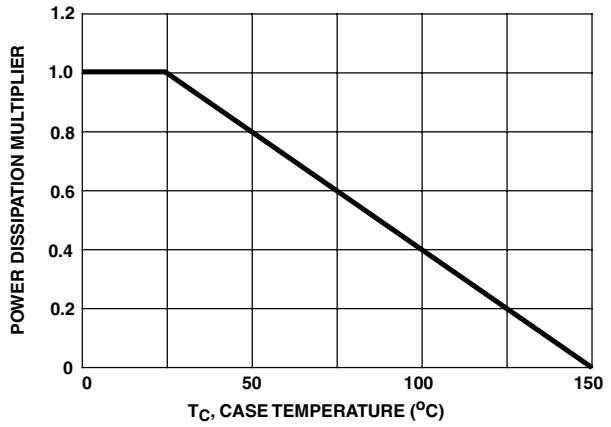


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

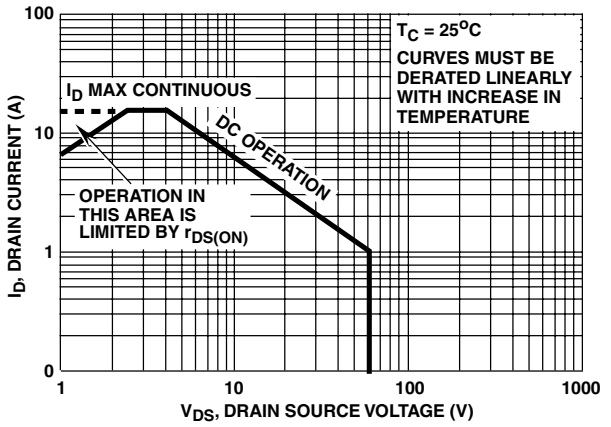


FIGURE 2. FORWARD BIAS SAFE OPERATING AREA

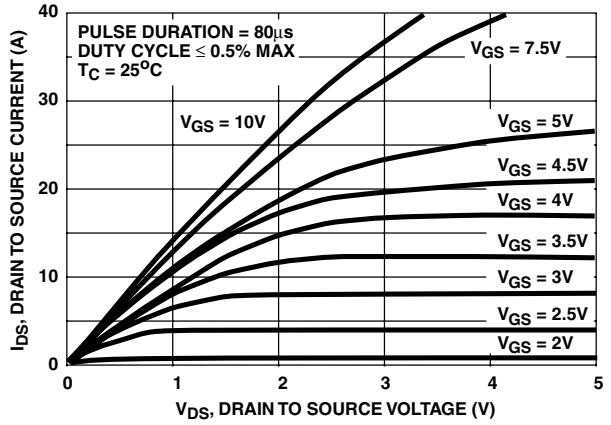


FIGURE 3. SATURATION CHARACTERISTICS

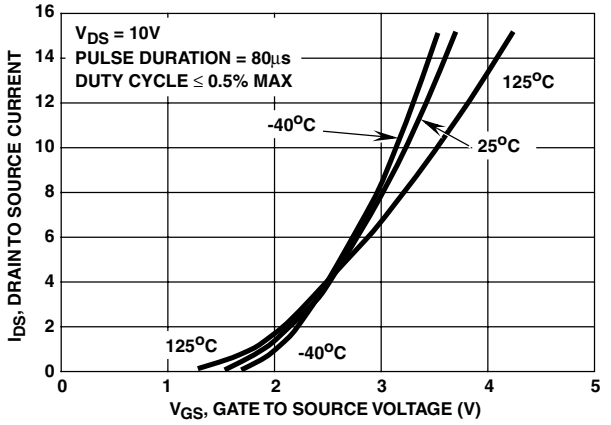


FIGURE 4. TRANSFER CHARACTERISTICS

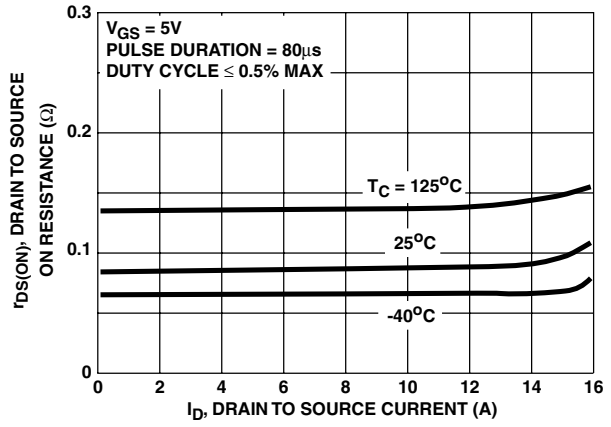


FIGURE 5. DRAIN TO SOURCE ON RESISTANCE vs DRAIN CURRENT

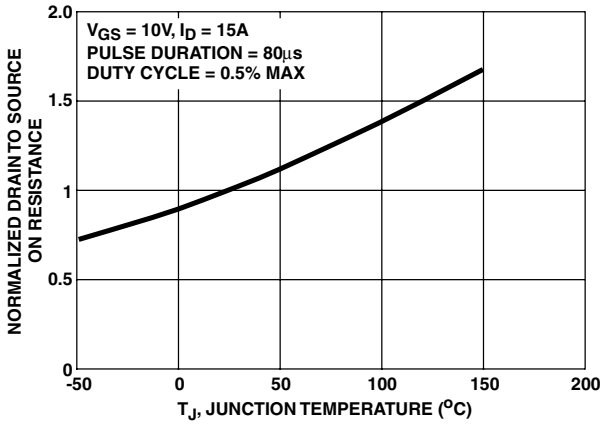


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

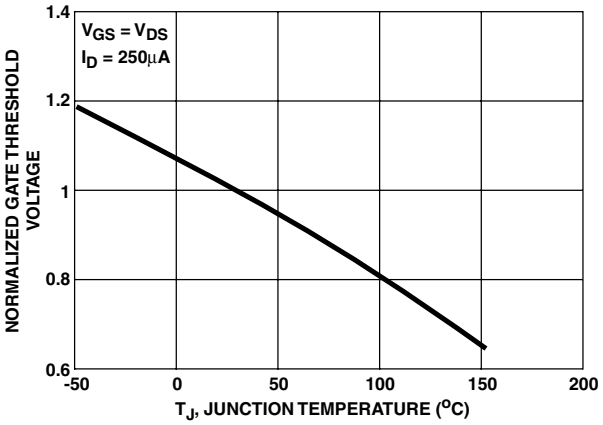


FIGURE 7. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

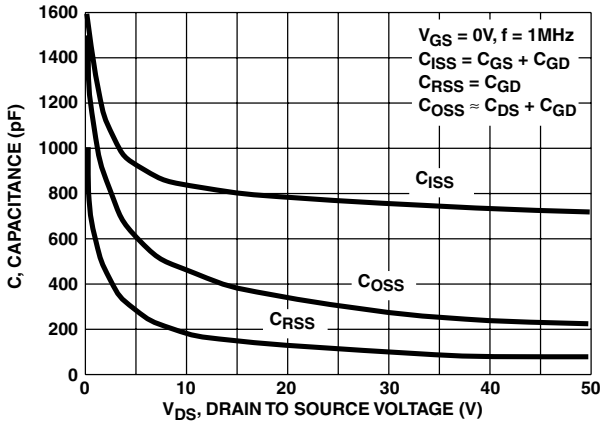
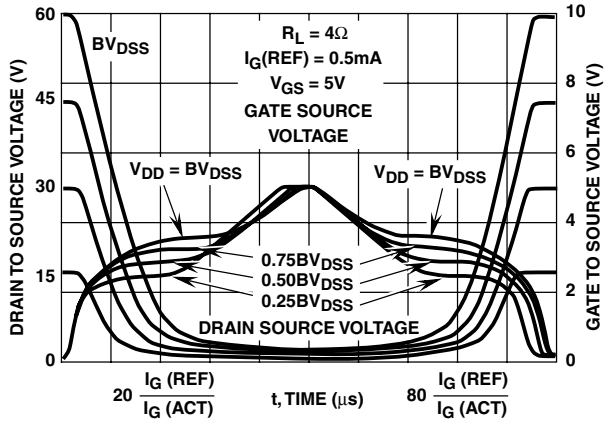


FIGURE 8. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 9. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

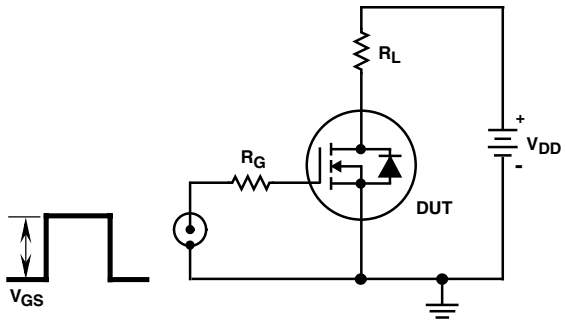


FIGURE 10. SWITCHING TIME TEST CIRCUIT

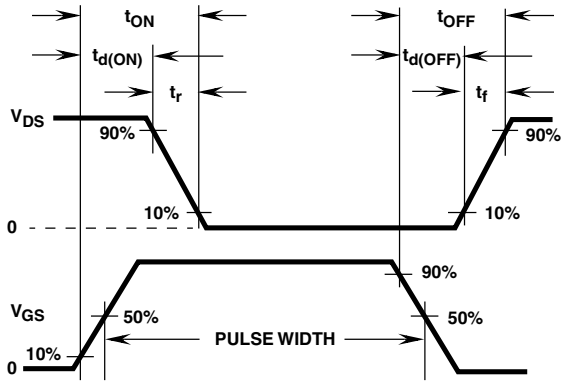


FIGURE 11. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

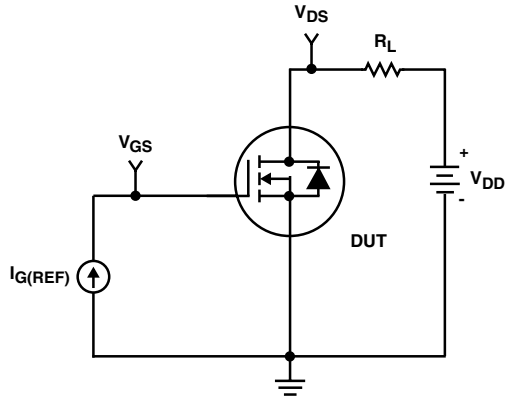


FIGURE 12. GATE CHARGE TEST CIRCUIT

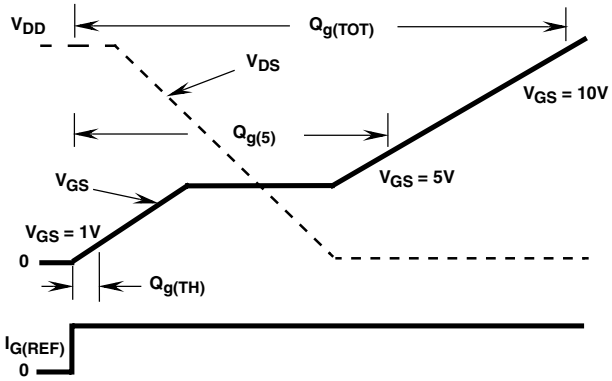


FIGURE 13. GATE CHARGE WAVEFORMS

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