25A, 60V, 0.025 Ohm, N-Channel Power MOSFET

The RFF70N06 N-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Reliability screening is available as either commercial or TX/TXV equivalent of MIL-S-19500. Contact Intersil Corporation High-Reliability Marketing group for any desired deviations from the data sheet.

Formerly developmental type TA49007.

Ordering Information

PART NUMBER	PACKAGE	BRAND
RFF70N06	TO-254AA	RFF70N06

NOTE: When ordering, use the entire part number.

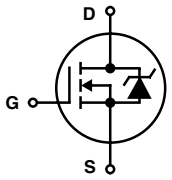
Commercial Version: RFG70N06.

Features

- 25A†, 60V
- $r_{DS(ON)} = 0.025\Omega$
- Temperature Compensating PSPICE™ Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 150^{o}C Operating Temperature
- Reliability Screened

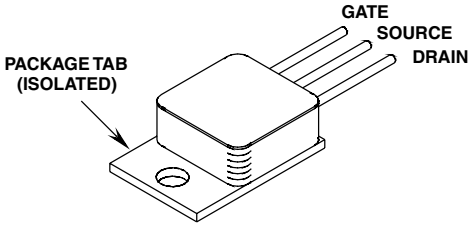
† Current is limited by the package capability.

Symbol



Packaging

JEDEC TO-254AA



CAUTION: Berylia Warning per MIL-S-19500.
Refer to package specifications.

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RFF70N06	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	60	V
Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	V_{DGR}	60	V
Gate to Source Voltage	V_{GS}	±20	V
Continuous Drain Current (Note 2)	I_D	25 (Note 2)	A
Pulsed Drain Current (Note 4) (Figure 5)	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating (Figure 6)	E_{AS}	Refer to UIS Curve	
Power Dissipation	P_D	100	W
Linear Derating Factor		0.80	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150	^{o}C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10s	T_L	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 125^oC.
2. Current is limited by the package capability.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2.0	3.0	4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Rated BV_{DSS}, V_{GS} = 0V		-	-	25	μA
		V_{DS} = 0.8 x Rated BV_{DSS}, V_{GS} = 0V, $T_C = 125^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, $T_C = 125^oC$		-	-	±100	μA
Drain to Source On Resistance (Note 3)	$r_{DS(ON)}$	I_D = 25A, V_{GS} = 10V		-	-	0.025	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, $I_D \approx$ 25A, R_L = 1.2Ω, V_{GS} = 10V, R_{GS} = 2.35Ω (Figures 13, 16, 17)		-	-	240	ns
Turn-On Delay Time	$t_{d(ON)}$			-	25	70	ns
Rise Time	t_r			-	70	170	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	60	150	ns
Fall Time	t_f			-	25	65	ns
Turn-Off Time	t_{OFF}			-	-	215	ns
Total Gate Charge	$Q_{g(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 30V, I_D = 25A, R_L = 1.2Ω, $I_{G(REF)}$ = 1.0mA (Figures 18, 19)	-	-	260	nC
Gate Charge at 10V	$Q_{g(10)}$	V_{GS} = 0 to 10V		-	-	145	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0 to 2V		-	-	7	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	3100	-	pF
Output Capacitance	C_{OSS}			-	900	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	300	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.25	^{o}C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	48	^{o}C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 25A	-	1.1	1.5	V
Diode Reverse Recovery Time	t_{rr}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	190	300	ns

NOTES:

3. Pulse test: pulse width ≤ 300ms, duty cycle ≤ 2%.
4. Repetitive rating: pulse width is limited by maximum junction temperature. See Transient Thermal Impedance curve Figure 3).

Typical Performance Curves Unless Otherwise Specified

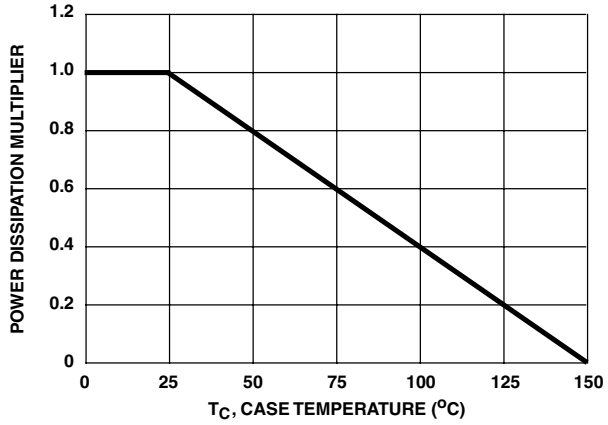


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

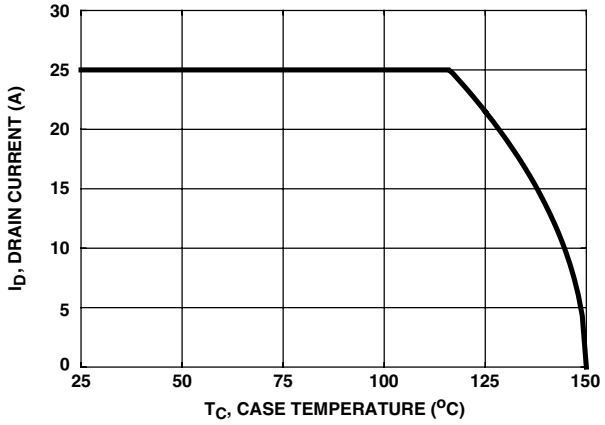


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

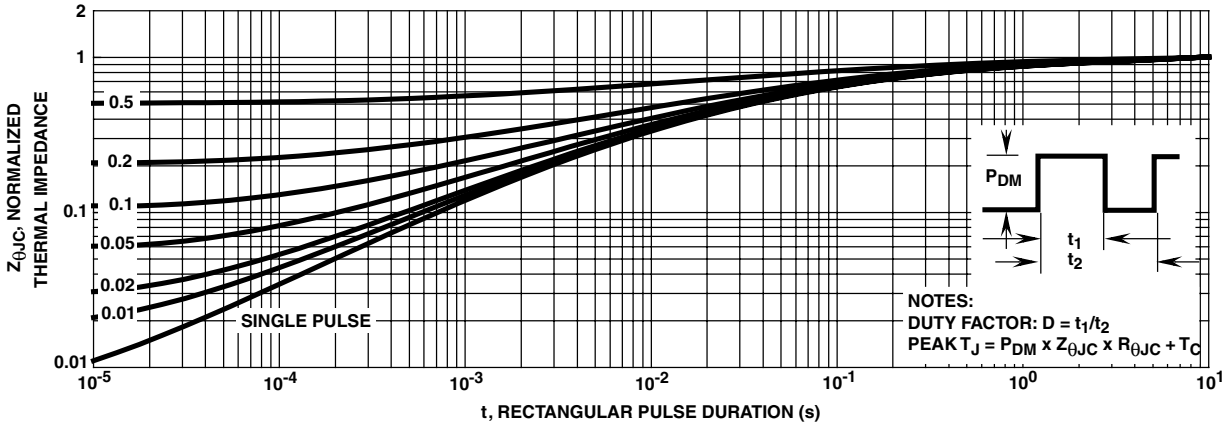


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

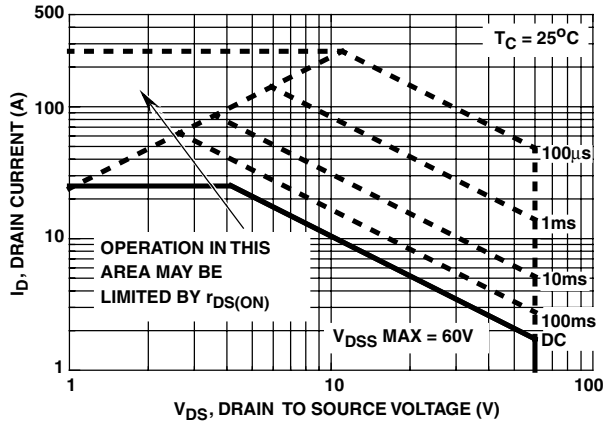


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

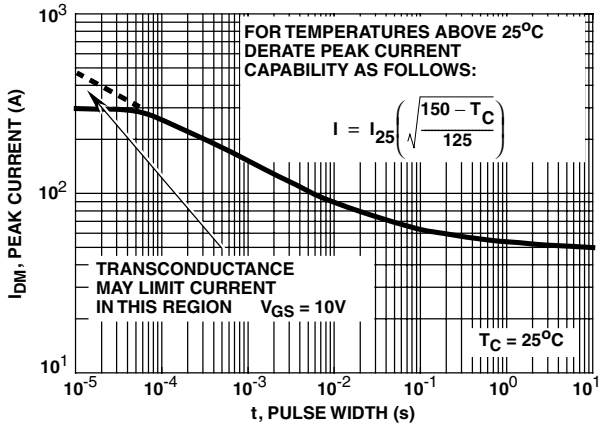
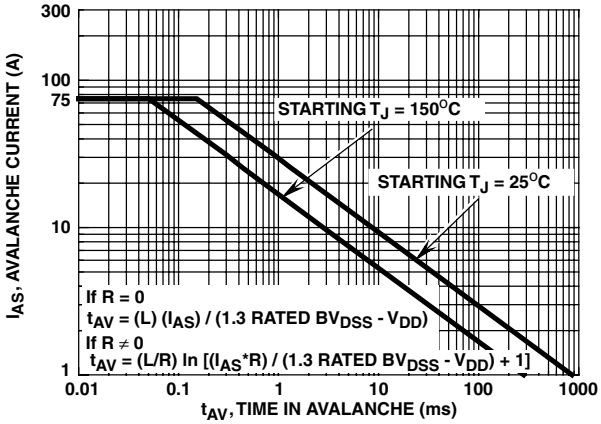


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

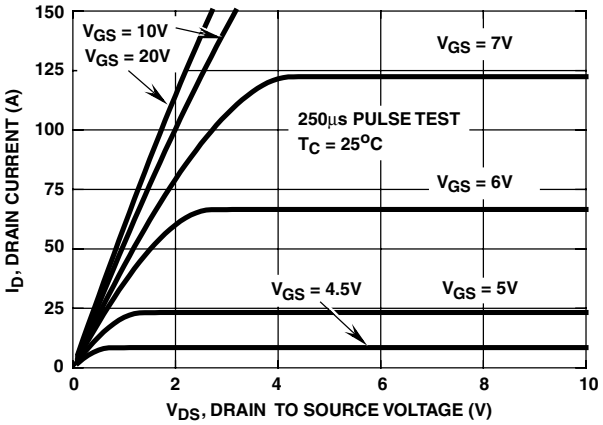


FIGURE 7. SATURATION CHARACTERISTICS

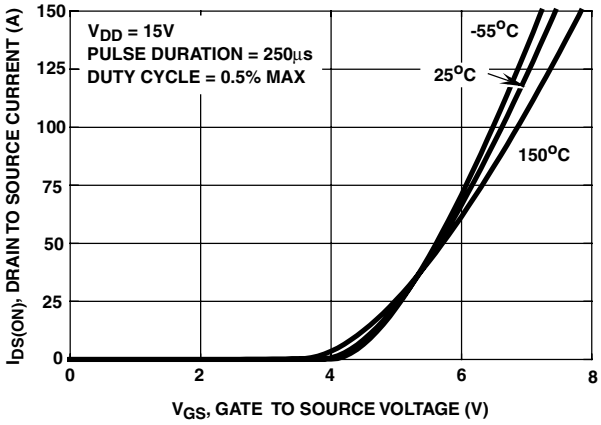


FIGURE 8. TRANSFER CHARACTERISTICS

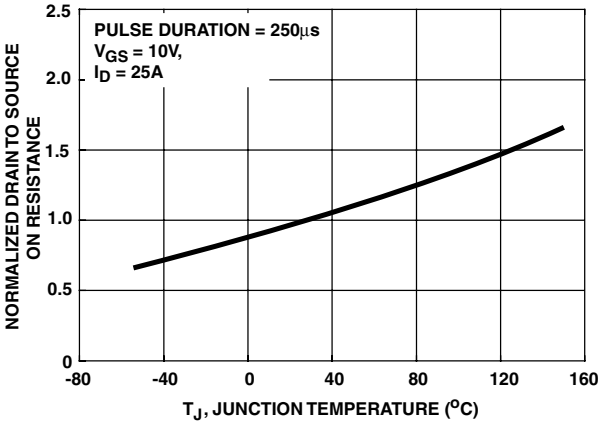


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

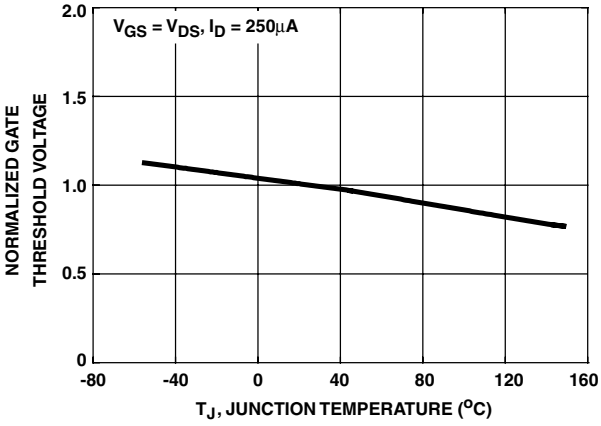


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

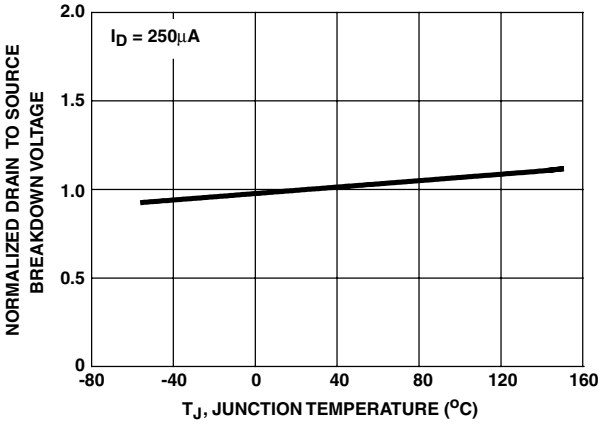


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

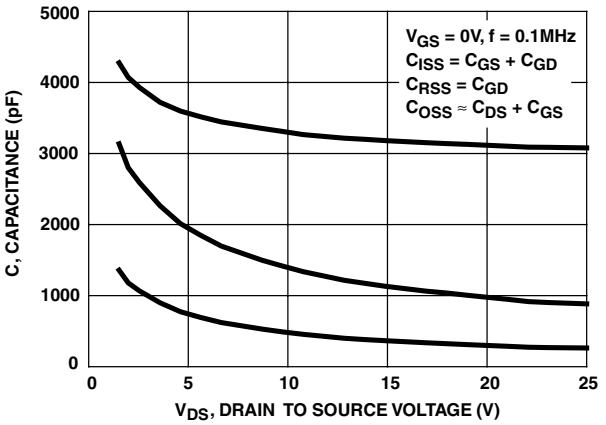
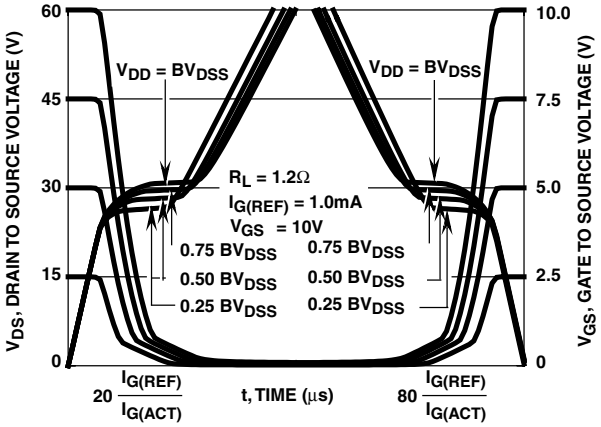


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

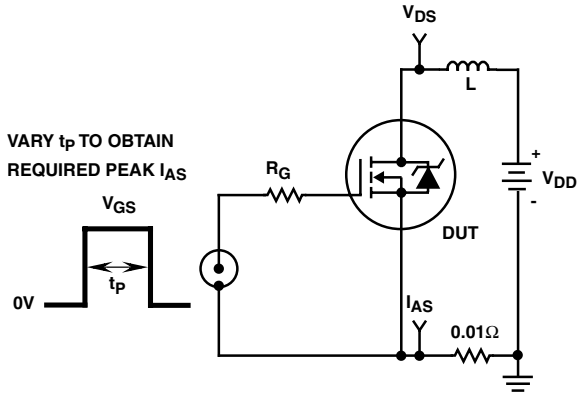


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

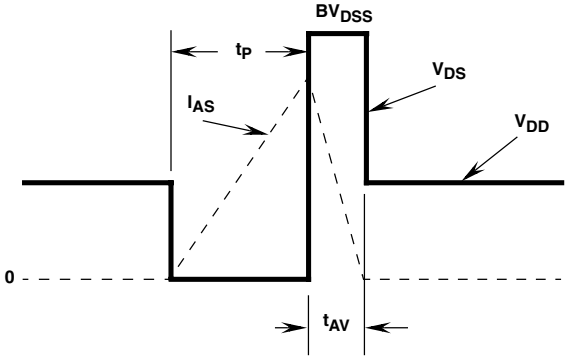


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

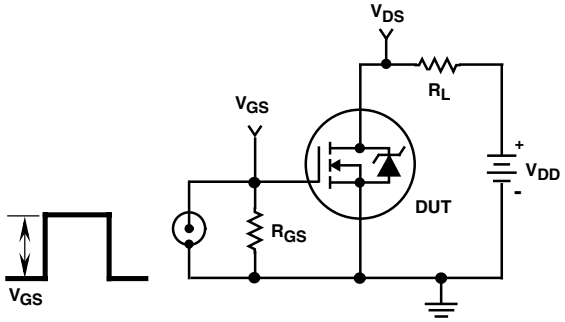


FIGURE 16. SWITCHING TIME TEST CIRCUIT

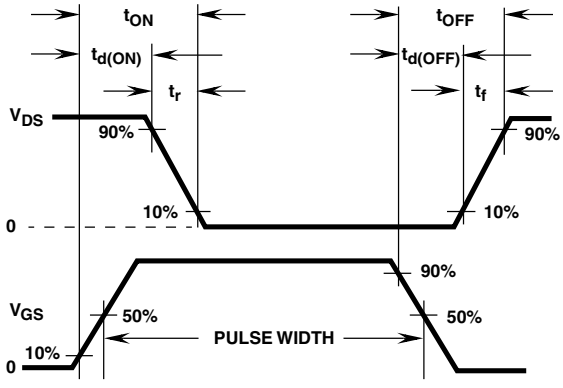


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

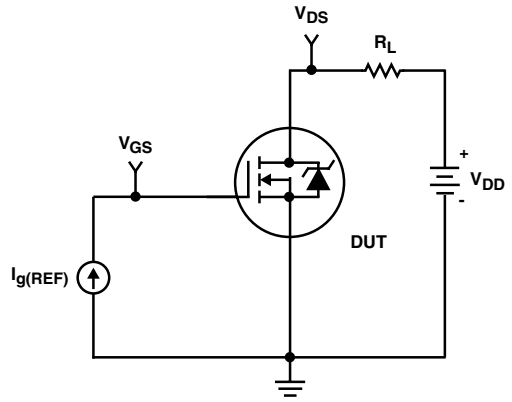


FIGURE 18. GATE CHARGE TEST CIRCUIT

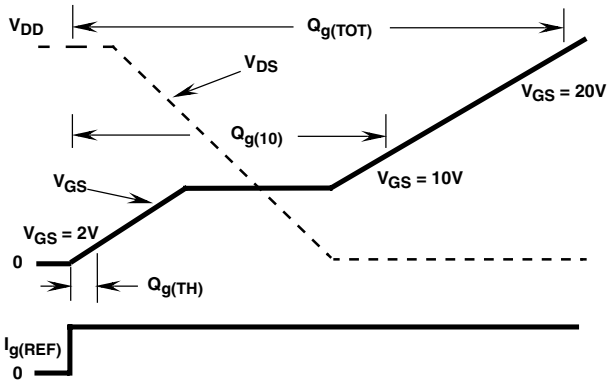


FIGURE 19. GATE CHARGE WAVEFORMS

Data Packages - Intersil Power Transistors

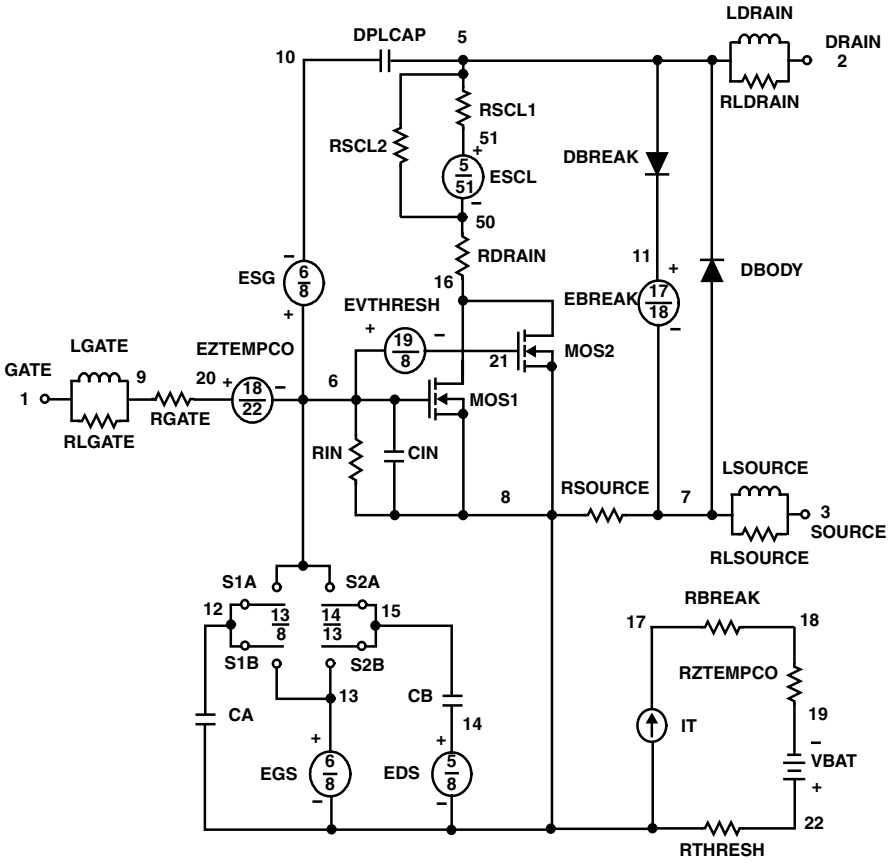
TX and TXV Equivalents

1. TX/TXV Equivalent - Standard Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning - Attributes Data Sheet
   - D. Group A - Attributes Data Sheet
   - E. Group B - Attributes Data Sheet
   - F. Group C - Attributes Data Sheet
2. TX/TXV Equivalent - Optional Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning
     - Attributes Data Sheet
     - Precondition Lot Traveler
     - Pre and Post Burn-In Read and Record Data
   - D. Group A
     - Attributes Data Sheet
     - Group A Lot Traveler
   - E. Group B
     - Attributes Data Sheet
     - Group B Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
     - Bond Strength Data (Subgroup B3)
     - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
   - F. Group C
     - Attributes Data Sheet
     - Group C Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
     - Bond Strength Data (Subgroup C6)

PSPICE Electrical Model

SUBCKT RFF70N06 2 1 3 ; rev 5/29/95

```
CA 12 8 5.20e-9
CB 15 14 5.20e-9
CIN 6 8 2.80e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 68.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRESH 6 21 19 8 1
EZTEMPCO 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 6.04e-9
LSOURCE 3 7 2.24e-9

MOS1 16 6 8 8 MSTRONG M = 0.99
MOS2 16 21 8 8 MWEAK M = 0.01

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 8.03e-3
RGATE 9 20 1
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 60.4
RLSOURCE 3 7 22.4
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 7.20e-3
RTHRESH 22 8 RTHRESMOD 1
RZTEMPCO 18 19 RZTEMPCOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),3))}

.MODEL DBDMOD D (IS = 1e-12 RS = 11.01e-3 TRS1 = 1.75e-3 TRS2 = -0.06e-6 CJO = 2.70e-9 TT = 7.82e-8 M = 0.45)
.MODEL DBREAKMOD D (RS = 88e-3 TRS1 = 1.50e-3 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 2.60e-9 IS = 1e-30 N = 10 M=0.7)
.MODEL MSTRONG NMOS (VTO = 3.85 KP = 47.2 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL MWEAK NMOS (VTO = 3.09 KP = 47.2 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 1e-3 TC2 = 0)
.MODEL RDRAINMOD RES (TC1 = 7e-3 TC2 = 1.90e-5)
.MODEL RDSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RSCLMOD RES (TC1 = 0 TC2 = 0)
.MODEL RTHRESHMOD RES (TC1 = -3.10e-3 TC2 = -1e-5)
.MODEL RZTEMPCOMOD RES (TC1 = -2.25e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF= -4.0)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF= -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF= 2.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.0 VOFF= -2.0)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table)

Delta Tests and Limits (JANTX/JANTXV Equivalent)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20V, T_C = 25°C	±20 (Note 5)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value, T_C = 25°C	±25 (Note 5)	μA
On Resistance	$r_{DS(ON)}$	T_C = 125°C at Rated I_D	±20% (Note 6)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1.0mA, T_C = 25°C	±20% (Note 6)	V

NOTES:

5. Or 100% of Initial Reading (whichever is greater).
6. Of Initial Reading.

Screening Information

TEST	JANTX/JANTXV EQUIVALENT
Gate Stress	V_{GS} = 30V, t = 250μs
Pind	Optional
PDA	10%
Pre Burn-In Test (Note 7)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, T_A = 150°C, Time = 48 hours
Interim Electrical Tests (Note 7)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, T_A = 150°C, Time = 168 hours
Final Electrical Tests (Note 7)	MIL-S-19500, Group A, Subgroup 2

NOTE:

7. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	V_{DS} = 48V, t = 10ms	4.8	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)}$ = 15V, L = 0.1mH	75	A
Thermal Response	ΔV_{SD}	t_H = 100ms; V_H = 25V, I_H = 4A	220	mV
Thermal Impedance	ΔV_{SD}	t_H = 500ms; V_H = 25V, I_H = 4A	330	mV

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Bottomless™	FASTr™	POP™	SuperSOT™-6
CoolFET™	GlobalOptoisolator™	PowerTrench ®	SuperSOT™-8
CROSSVOLT™	GTO™	QFET™	SyncFET™
DenseTrench™	HiSeC™	QS™	TinyLogic™
DOME™	ISOPLANAR™	QT Optoelectronics™	UHC™
EcoSPARK™	LittleFET™	Quiet Series™	UltraFET™
E^2CMOS^{TM}	MicroFET™	SILENT SWITCHER ®	VCX™
EnSigna™	MICROWIRE™	SMART START™	
FACT™	OPTOLOGIC™	Star* Power™	
FACT Quiet Series™	OPTOPLANAR™	Stealth™	

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.