

**14A, 60V, 0.100 Ohm, Logic Level,
N-Channel Power MOSFETs**

These are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA09870.

Ordering Information

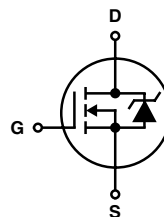
PART NUMBER	PACKAGE	BRAND
RFD14N06L	TO-251AA	14N06L
RFD14N06LSM	TO-252AA	14N06L
RFP14N06L	TO-220AB	FP14N06L

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD14N06LSM9A.

Features

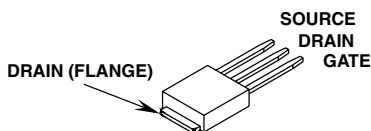
- 14A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- Temperature Compensating PSPICE® Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature
- Related Literature
 - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol

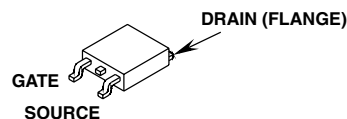


Packaging

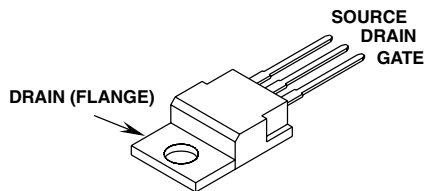
JEDEC TO-251AA



JEDEC TO-252AA



JEDEC TO-220AB



RFD14N06L, RFD14N06LSM, RFP14N06LS

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	RFD14N06L, RFD14N06LSM, RFP14N06LS	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	V
Gate to Source Voltage	V_{GS}	V
Drain Current Continuous	I_D	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve
Power Dissipation	P_D	W
Derate Above 25°C	0.32	W/ $^\circ\text{C}$
Operating and Storage Temperature	T_J, T_{STG}	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 150°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V, Figure 13		60	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA, Figure 12		1	-	2	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 48V, V _{GS} = 0V	T _C = 25°C	-	-	1	μA
			T _C = 150°C	-	-	50	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±10V		-	-	100	nA
On Resistance	r _{DS(ON)}	I _D = 14A, V _{GS} = 5V		-	-	0.100	Ω
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 7A, R _L = 4.28Ω, V _{GS} = 5V, R _{GS} = 0.6Ω Figures 10, 18, 19		-	-	60	ns
Turn-On Delay Time	t _{d(ON)}			-	13	-	ns
Rise Time	t _r			-	24	-	ns
Turn-Off Delay Time	t _{d(OFF)}			-	42	-	ns
Fall Time	t _f			-	16	-	ns
Turn-Off Time	t _{OFF}			-	-	100	ns
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 48V, I _D = 14A, R _L = 3.43Ω Figures 20, 21	-	-	40	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	-	25	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	-	1.5	nC
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz Figure 14		-	670	-	pF
Output Capacitance	C _{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C _{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	R _{θJC}			-	-	3.125	°C/W
Thermal Resistance Junction-to-Ambient	R _{θJA}	TO-251 and TO-252		-	-	100	°C/W
		TO-220		-	-	80	°C/W

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 14\text{A}$	-	-	1.5	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 14\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	125	ns

Typical Performance Curves Unless Otherwise Specified

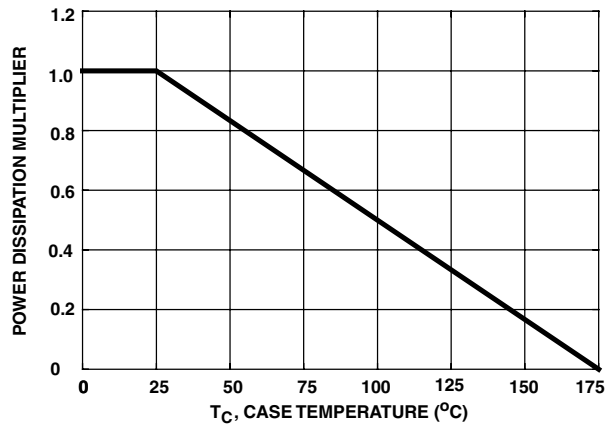


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

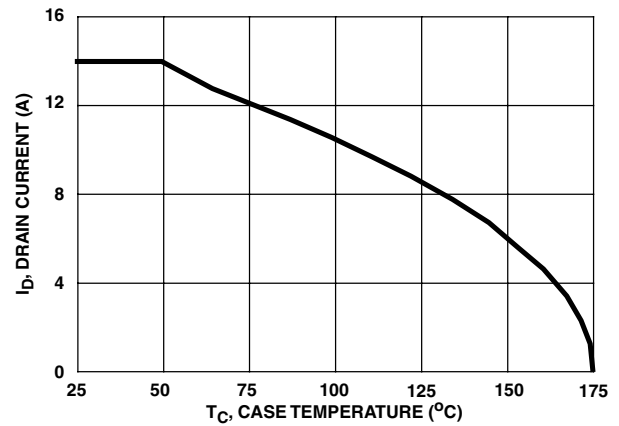


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

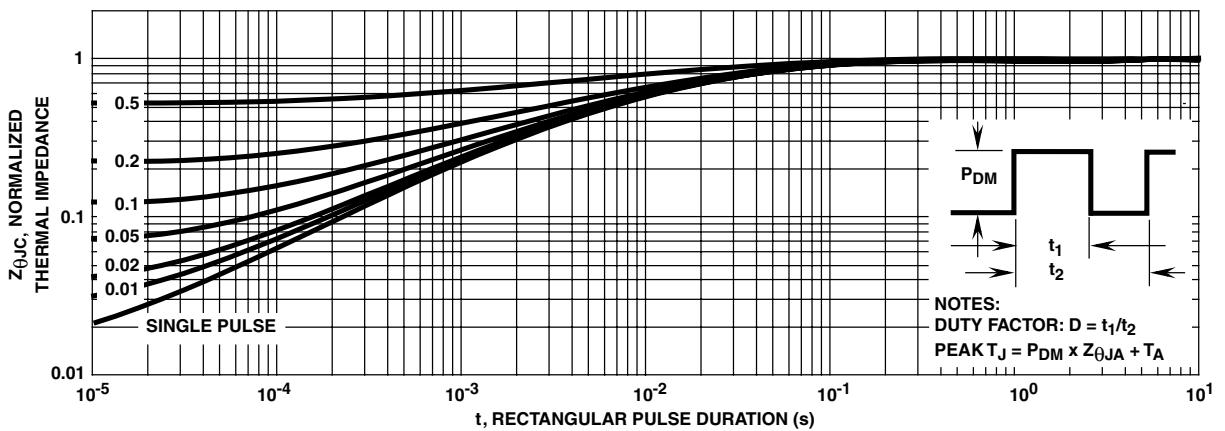


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

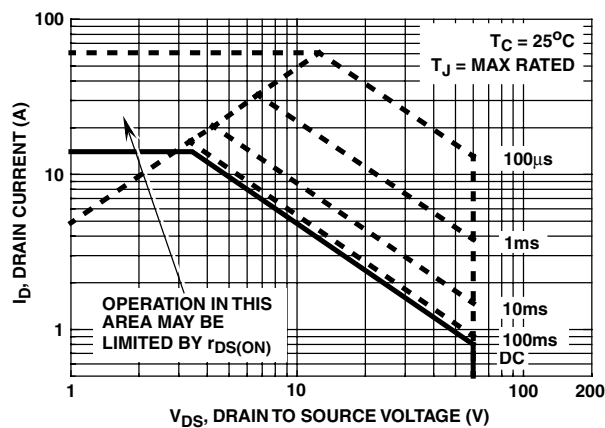


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

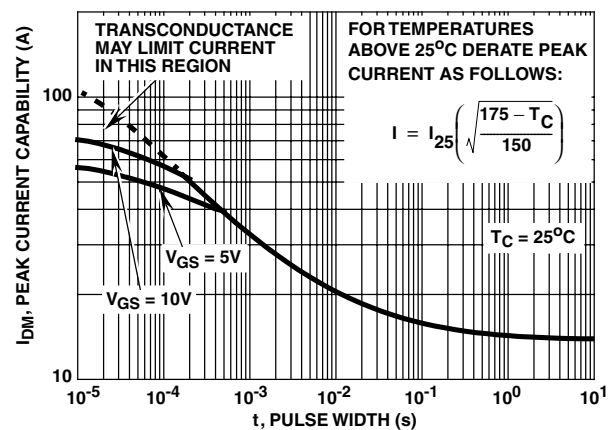
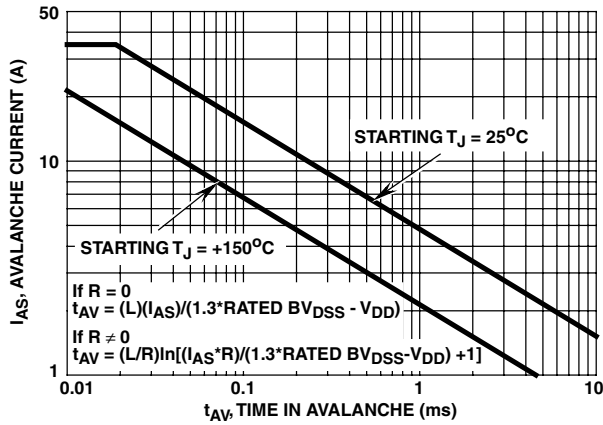


FIGURE 5. PEAK CURRENT CAPABILITY

Typical Performance Curves Unless Otherwise Specified (Continued)



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

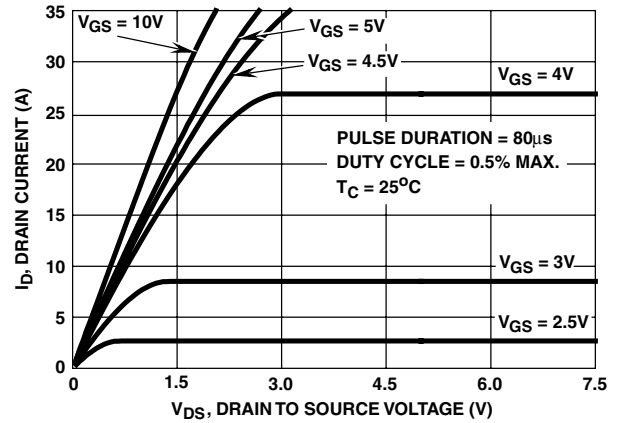


FIGURE 7. SATURATION CHARACTERISTICS

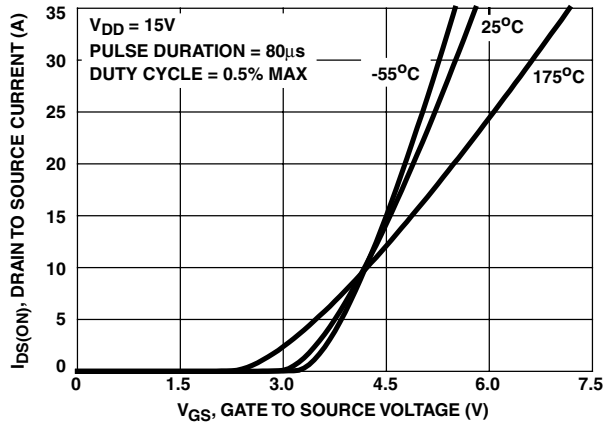


FIGURE 8. TRANSFER CHARACTERISTICS

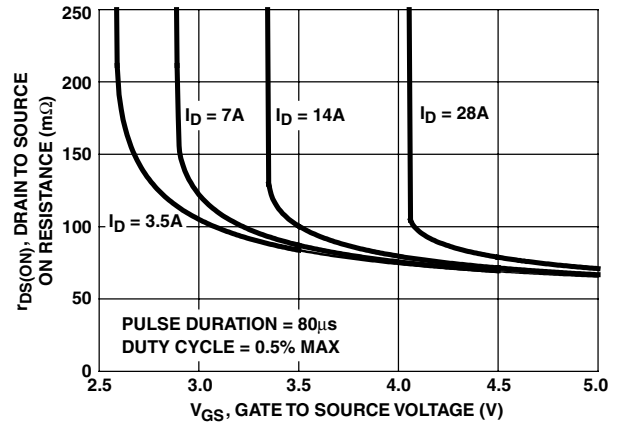


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

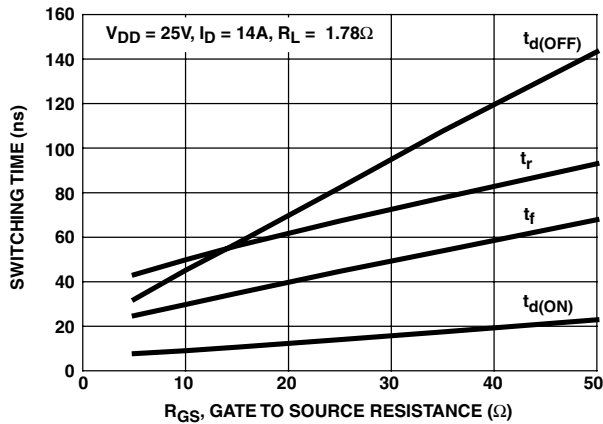


FIGURE 10. SWITCHING TIME vs GATE TO SOURCE RESISTANCE

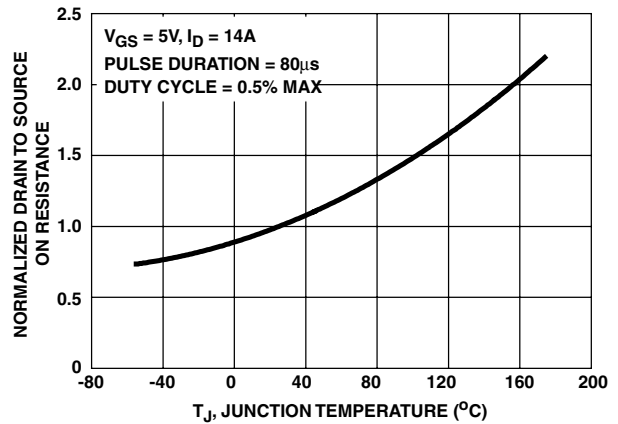


FIGURE 11. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

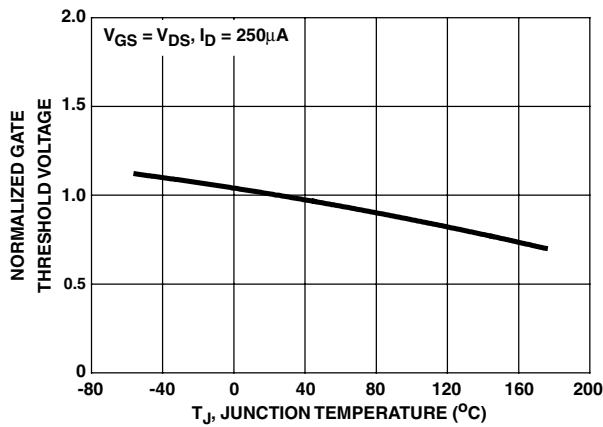


FIGURE 12. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

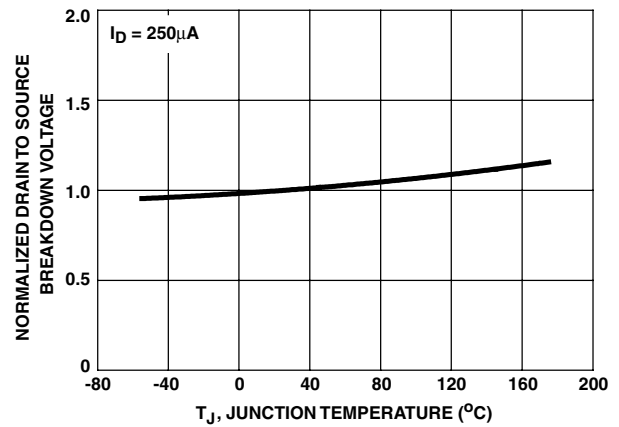


FIGURE 13. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

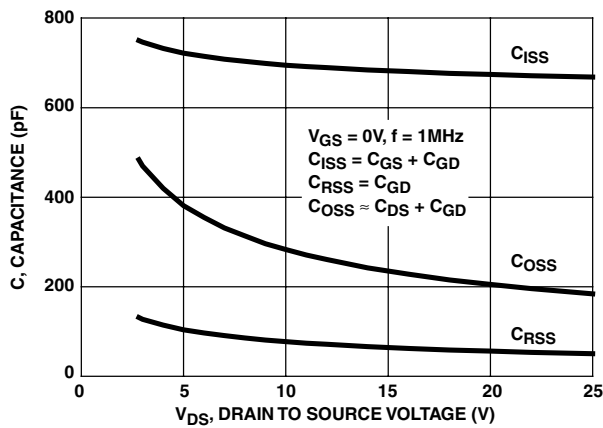
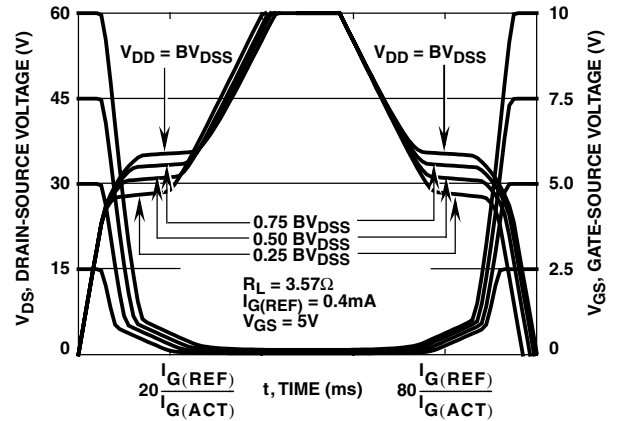


FIGURE 14. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 15. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

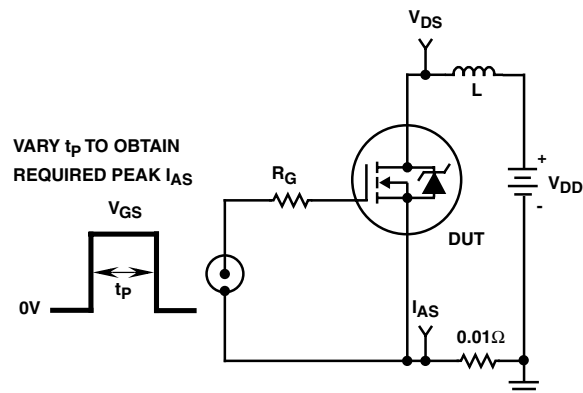


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

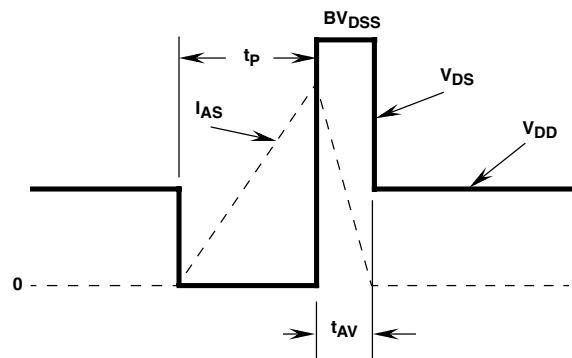


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

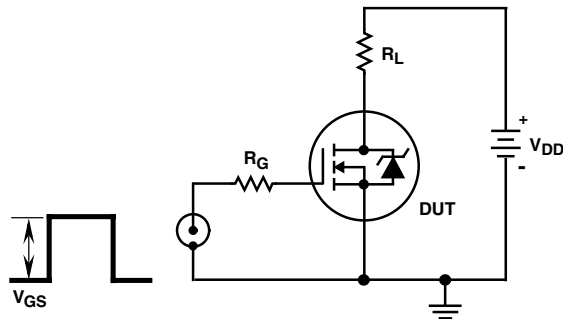


FIGURE 18. SWITCHING TIME TEST CIRCUIT

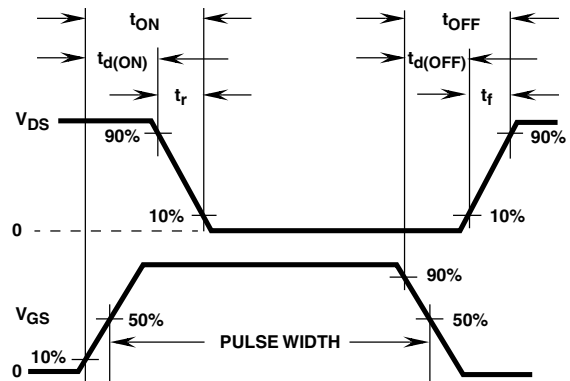


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

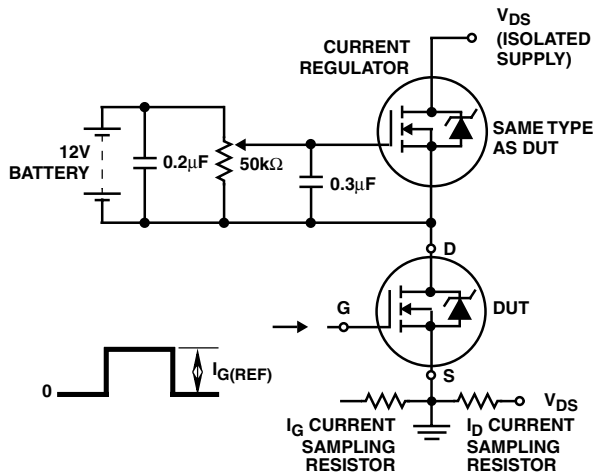


FIGURE 20. GATE CHARGE TEST CIRCUIT

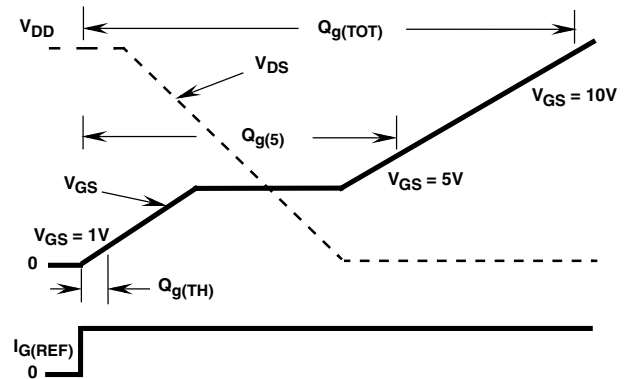


FIGURE 21. GATE CHARGE WAVEFORMS

RFD14N06L, RFD14N06LSM, RFP14N06L

PSPICE Electrical Model

```
.SUBCKT RFP14N06L 2 1 3 ;    rev 9/15/94
CA 12 8 1.464e-9
CB 15 14 1.64e-9
CIN 6 8 6.17e-10
```

```
DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD
```

```
EBREAK 11 7 17 18 65.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1
```

```
IT 8 17 1
```

```
LDRAIN 2 5 1e-9
LGATE 1 9 5.68e-9
LSOURCE 3 7 5.35e-9
```

```
MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01
```

```
RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 33.1e-3
RGATE 9 20 5.85
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 14.3e-3
RVTO 18 19 RVTOMOD 1
```

```
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD
```

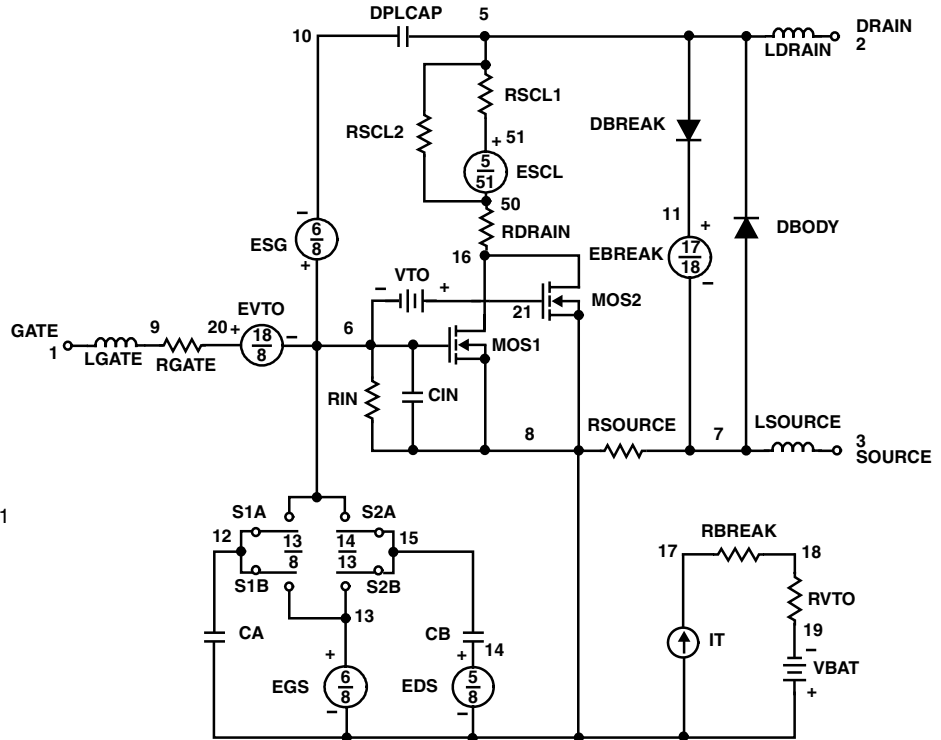
```
VBAT 8 19 DC 1
VTO 21 6 0.485
```

```
ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/46,7))}
```

```
.MODEL DBDMOD D (IS = 2.23e-13 RS = 1.15e-2 TRS1 = 1.64e-3 TRS2 = 7.89e-6 CJO = 6.83e-10 TT = 3.68e-8)
.MODEL DBKMOD D (RS = 3.8e-1 TRS1 = 1.89e-3 TRS2 = 1.13e-5)
.MODEL DPLCAPMOD D (CJO = 25.7e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.935 KP = 18.89 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.18e-4 TC2 = 1.53e-6)
.MODEL RDSMOD RES (TC1 = 4.45e-3 TC2 = 2.9e-5)
.MODEL RSCLMOD RES (TC1 = 2.8e-3 TC2 = 6.0e-6)
.MODEL RVTOMOD RES (TC1 = -1.7e-3 TC2 = -2.0e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.55 VOFF = -1.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.55 VOFF = -3.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF = 2.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.45 VOFF = -2.55)
```

```
.ENDS
```

NOTE: For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; authored by William J. Hepp and C. Frank Wheatley.



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FACT [™]	OPTOLOGIC [™]	Star* Power [™]	
FACT Quiet Series [™]	OPTOPLANAR [™]	Stealth [™]	

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
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