Data Sheet July 1999 File Number 2839.4

1A, 55V, 0.750 Ohm,Voltage Clamping, Current Limited, N-Channel Power MOSFET

The RLP1N06CLE is an intelligent monolithic power circuit which incorporates a lateral bipolar transistor, resistors, zener diodes, and a PowerMOS transistor. The current limiting of this device allows it to be used safely in circuits where it is anticipated that a shorted load condition may be encountered. The drain to source voltage clamping offers precision control of the circuit voltage when switching inductive loads. Logic level gates allow this device to be fully biased on with only 5V from gate to source. Input protection is provided for ESD up to 2kV.

Formerly developmental type TA09880.

Ordering Information

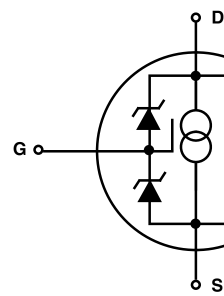
PART NUMBER	PACKAGE	BRAND
RLP1N06CLE	TO-220AB	L1N06CLE

NOTE: When ordering, use the entire part number.

Features

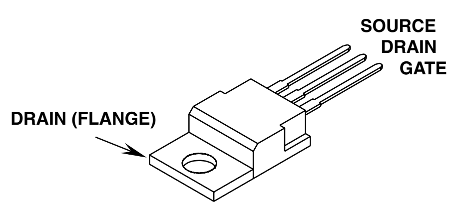
- 1A, 55V
- $r_{DS(ON)} = 0.750\Omega$
- I_{LIMIT} at 150°C = 1.1A to 1.5A Maximum
- Built-in Voltage Clamp
- Built-in Current Limiting
- ESD Protected, 2kV Minimum
- Controlled Switching Limits EMI and RFI
- 175°C Rated Junction Temperature
- Logic Level Gate
- Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

Symbol



Packaging

JEDEC TO-220AB



Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		RLP1N06CLE	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	55	V
Drain to Gate Voltage (R_{GS} = 20kΩ, Note 1)	V_{DGR}	55	V
Electrostatic Voltage at $T_C = 25^oC$	ESD	2	kV
Continuous Drain Current	I_D	Self Limited	
Gate to Source Voltage (Reverse Voltage Gate Bias Not Allowed)	V_{GS}	5.5	V
Maximum Power Dissipation	P_D	36	W
Power Dissipation Derating		0.24	$W/^oC$
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^oC
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300	^oC
Package Body for 10s, See Techbrief 334	T_{pkg}	260	^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^oC$ to 150^oC.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 20mA, V_{GS} = 0V (Figure 7)		55	-	70	V
Gate to Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250μA (Figure 8)		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V, V_{GS} = 0V	TC = 25^oC	-	-	5	μA
			TC = 150^oC	-	-	20	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = 5V	TC = 25^oC	-	-	5	μA
			$T_C = 150^oC$	-	-	20	μA
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	I_D = 1A, V_{GS} = 5V (Figure 6)	TC = 25^oC	-	-	0.750	Ω
			$T_C = 150^oC$	-	-	1.500	Ω
Limiting Current	$I_{DS(LIM)}$	V_{DS} = 15V, V_{GS} = 5V (Figure 2)	TC = 25^oC	1.8	-	3	A
			$T_C = 150^oC$	0.9	-	1.5	A
Turn-On Time	$t_{(ON)}$	V_{DD} = 30V, I_D = 1A, V_{GS} = 5V, R_{GS} = 25Ω R_L = 30Ω		-	-	6.5	μs
Turn-On Delay Time	$t_{d(ON)}$			-	-	1.5	μs
Rise Time	t_r			1	-	5	μs
Turn-Off Delay Time	$t_{d(OFF)}$			-	-	7.5	μs
Fall Time	t_f			1	-	5	μs
Turn-Off Time	$t_{(OFF)}$			-	-	12.5	μs
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	4.17	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220AA		-	-	62	$^oC/W$
Electrostatic Voltage	ESD	Human Model (100pF, 1.5kΩ) MIL-STD-883B (Category B2)		2000	-	-	V

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage (Note 2)	V_{SD}	I_{SD} = 1A	-	-	1.5	V
Reverse Recovery Time	t_{rr}	I_{SD} = 1A	-	-	1	ms

NOTES:

2. Pulsed: pulse duration = 80μs maximum, duty cycle = 2%.
3. Repetitive rating: pulse width limited by maximum junction temperature.

Typical Performance Curves Unless Otherwise Specified

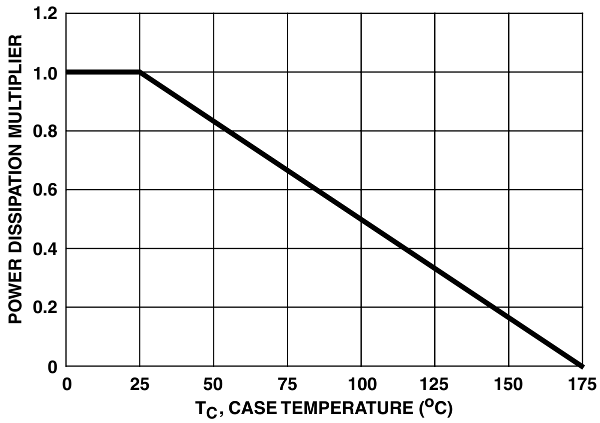


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

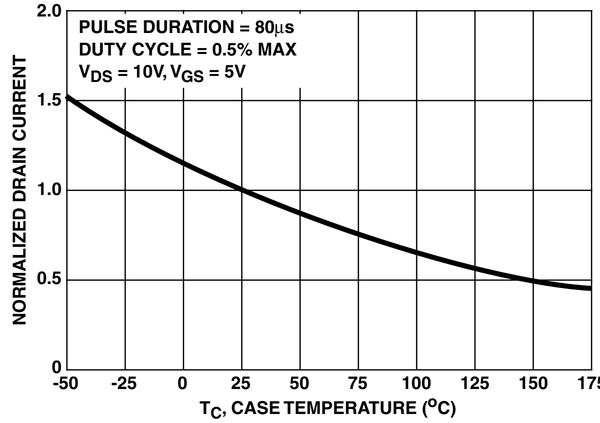


FIGURE 2. NORMALIZED CURRENT LIMIT vs CASE TEMPERATURE

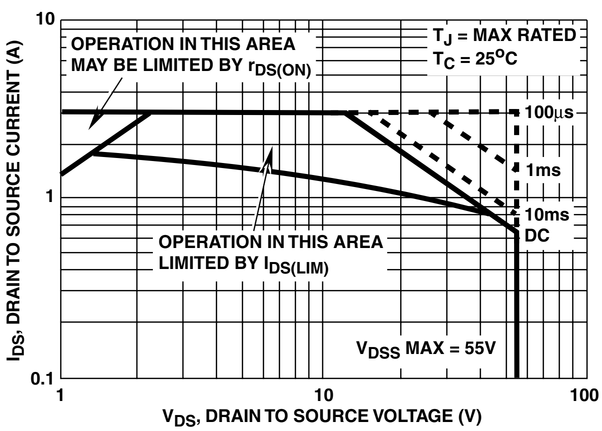


FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

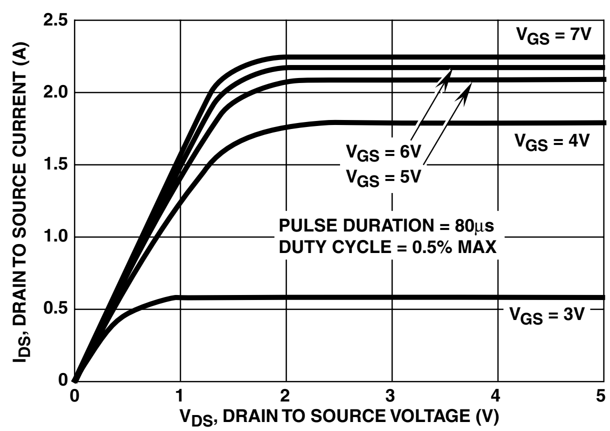


FIGURE 4. SATURATION CHARACTERISTICS

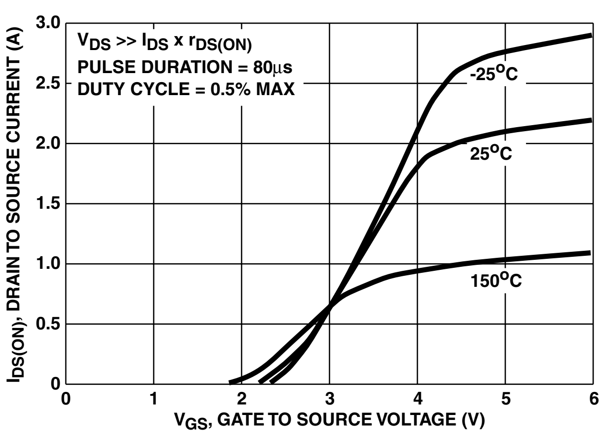


FIGURE 5. TRANSFER CHARACTERISTICS

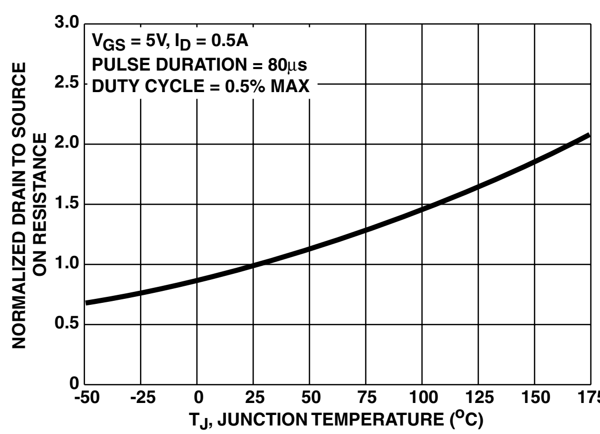


FIGURE 6. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified **(Continued)**

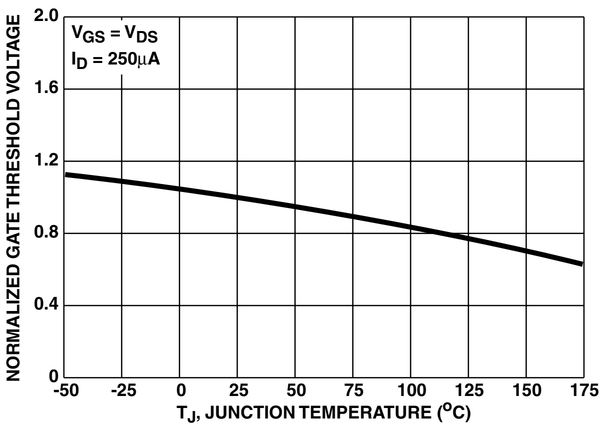


FIGURE 7. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

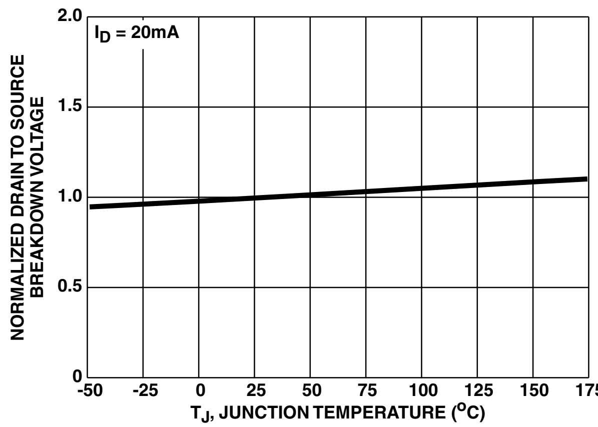


FIGURE 8. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

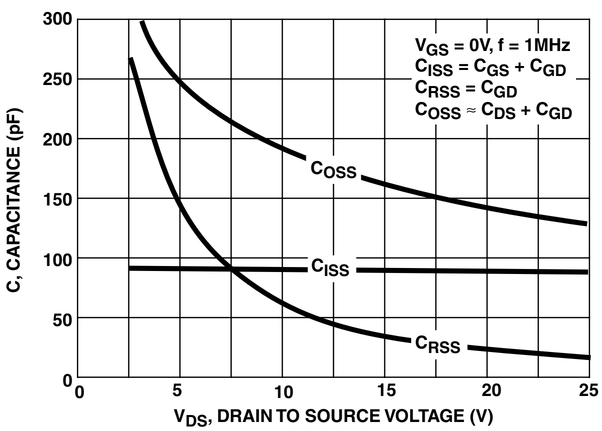


FIGURE 9. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

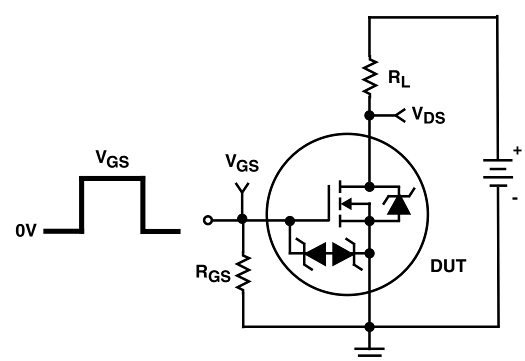


FIGURE 10. SWITCHING TEST CIRCUIT

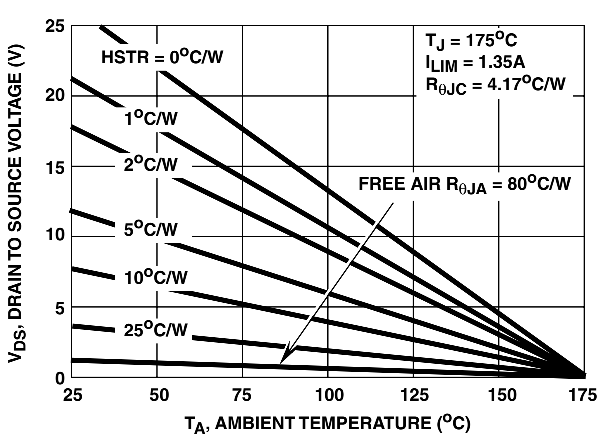
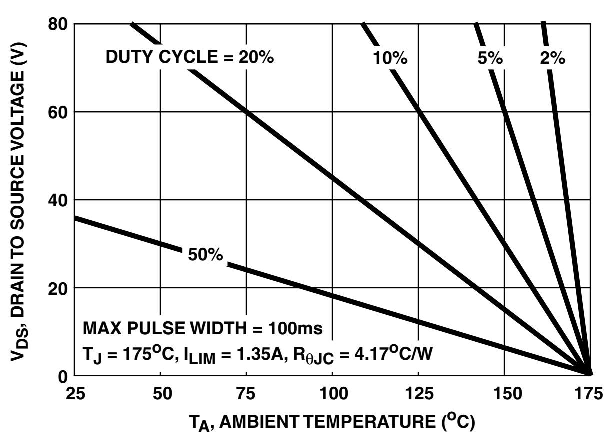


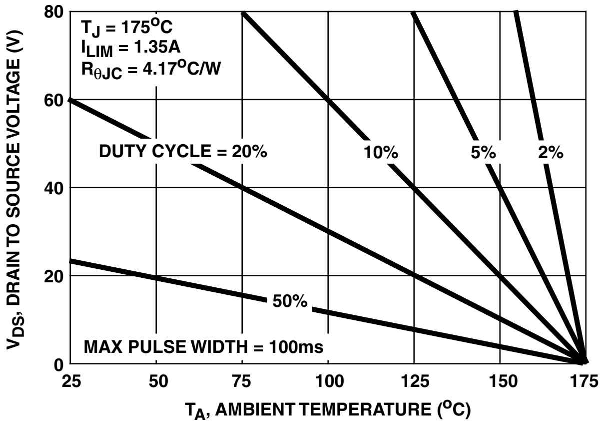
FIGURE 11. DC OPERATION IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = $2^oC/W$

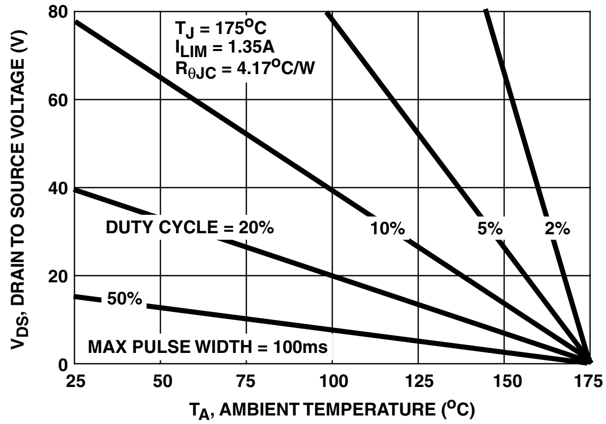
FIGURE 12. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING

Typical Performance Curves Unless Otherwise Specified (Continued)



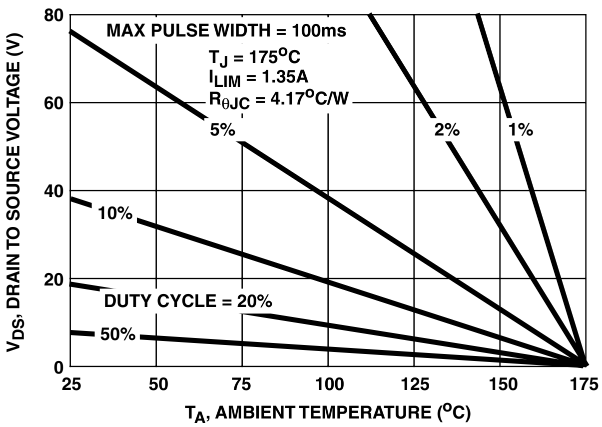
NOTE: Heatsink thermal resistance = $5^oC/W$

FIGURE 13. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



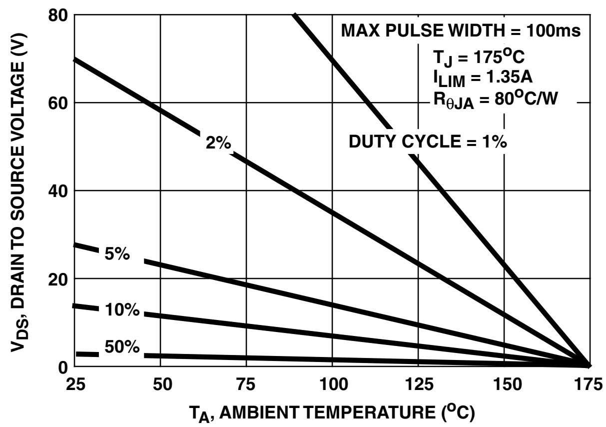
NOTE: Heatsink thermal resistance = $10^oC/W$

FIGURE 14. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



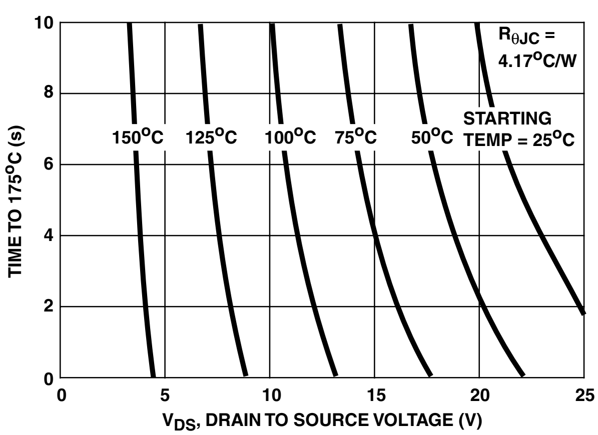
NOTE: Heatsink thermal resistance = $25^oC/W$

FIGURE 15. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



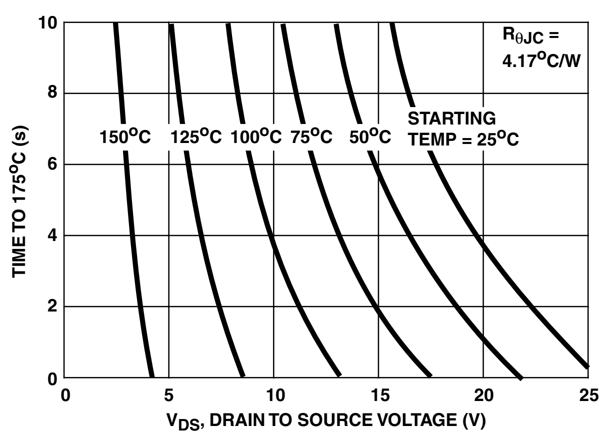
NOTE: No external heatsink

FIGURE 16. MAXIMUM V_{DS} vs T_A IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = $2^oC/W$
Heatsink thermal capacitance = $4j/^oC$

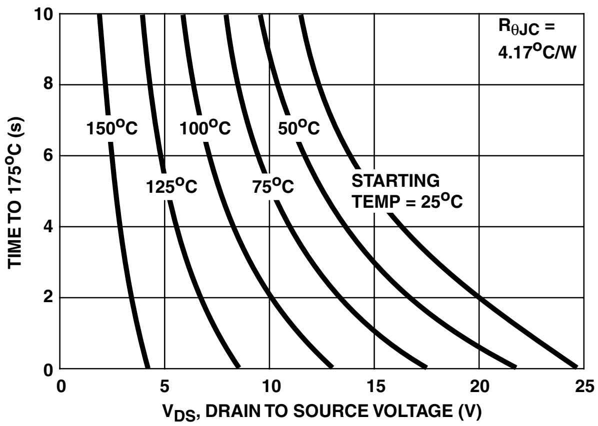
FIGURE 17. TIME TO 175^oC IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = $5^oC/W$
Heatsink thermal capacitance = $2j/^oC$

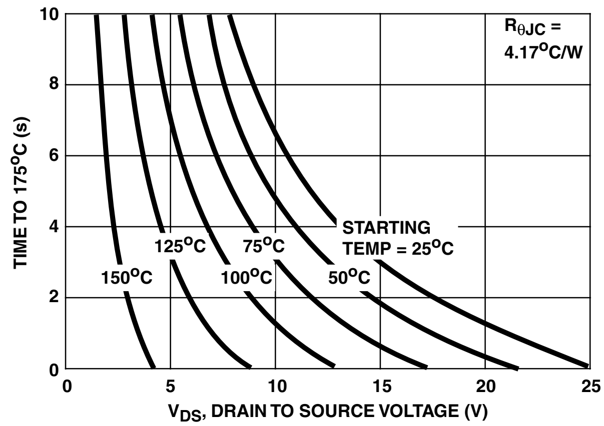
FIGURE 18. TIME TO 175^oC IN CURRENT LIMITING

Typical Performance Curves Unless Otherwise Specified **(Continued)**



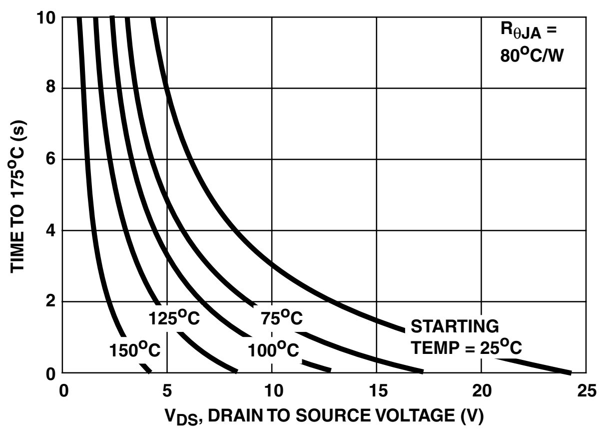
NOTE: Heatsink thermal resistance = 10°C/W
Heatsink thermal capacitance = 1j/°C

FIGURE 19. TIME TO 175°C IN CURRENT LIMITING



NOTE: Heatsink thermal resistance = 25°C/W
Heatsink thermal capacitance = 0.5j/°C

FIGURE 20. TIME TO 175°C IN CURRENT LIMITING



NOTE: No external heatsink

FIGURE 21. TIME TO 175°C IN CURRENT LIMITING

Detailed Description

Temperature Dependence of Current Limiting and Switching Speed

The RLP1N06CLE is a monolithic power device which incorporates a logic level PowerMOS transistor with a resistor in series with the source. The base and emitter of a lateral bipolar transistor is connected across this resistor, and the collector of the bipolar transistor is connected to the gate of the PowerMOS transistor. When the voltage across the resistor reaches the value required to forward bias the emitter base junction of the bipolar transistor, the bipolar transistor “turns on”. A series resistor is incorporated in series with the gate of the PowerMOS transistor allowing the bipolar transistor to drive the gate of the PowerMOS transistors to a voltage which just maintains a constant current in the PowerMOS transistor. Since both the resistance of the resistor in series with the PowerMOS transistor source and voltage required to forward bias the base emitter junction of the bipolar transistor vary with the temperature, the current at which the device limits is a function of temperature. This dependence is shown in figure 2.

The resistor in series with the gate of the PowerMOS transistor results in much slower switching than in most PowerMOS transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable, and a minimum as well as maximum fall time is given in the device characteristics for this type.

DC Operation of the RLP1N06CLE

The limit of the drain to source voltage for operation in current limiting on a steady state (DC) basis is shown as Figure 11. The dissipation in the device is simply the applied drain to source voltage multiplied by the limiting current. This device, like most Power MOSFET devices today, is limited to 175°C. The maximum voltage allowable can, therefore be expressed as:

$$V_{DS} = \frac{(175^{o}C - T_{AMBIENT})}{I_{LIM} \times (R_{\theta JC} + R_{\theta CA})} \quad \text{(EQ. 1)}$$

Duty Cycle Operation of the RLP1N06CLE

In many applications either the drain to source voltage or the gate drive is not available 100% of the time. The copper header on which the RLP1N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less than 100 milliseconds, the temperature of the header can be considered a constant case temperature calculated simply as:

$$T_C = (V_{DS} \times I_D \times D \times R_{\theta CA}) + T_{AMBIENT} \quad \text{(EQ. 2)}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 175°C and using the T_C calculated above, the expression for maximum V_{DS} under duty cycle operation is:

$$V_{DS} = \frac{175 - T_C}{I_{LIM} \times D \times R_{\theta JC}} \quad \text{(EQ. 3)}$$

These values are plotted as Figures 12 thru 16.

Limited Time Operations of the RLP1N06CLE

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 milliseconds and the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as figures 17 thru 21 give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST ®	PACMAN™	SuperSOT™-3
Bottomless™	FASTr™	POP™	SuperSOT™-6
CoolFET™	GlobalOptoisolator™	PowerTrench ®	SuperSOT™-8
CROSSVOLT™	GTO™	QFET™	SyncFET™
DenseTrench™	HiSeC™	QS™	TinyLogic™
DOME™	ISOPLANAR™	QT Optoelectronics™	UHC™
EcoSPARK™	LittleFET™	Quiet Series™	UltraFET™
E^2CMOS™	MicroFET™	SILENT SWITCHER ®	VCX™
EnSigna™	MICROWIRE™	SMART START™	
FACT™	OPTOLOGIC™	Star* Power™	
FACT Quiet Series™	OPTOPLANAR™	Stealth™	

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H