RC6100

Horizontal Genlock

Features

- High speed tracking sync separator easily follows hum or average picture level (APL) fluctuations
- Glitch remover for operation in high impulse noise environment
- On chip phase-locked loop
- Locks and follows VCR sync
- Compatible with NTSC and PAL systems
- Choice of eight output frequencies
- Field ID output
- Internal VCO

Applications

- Digital video signal processing
- Digital television receivers and VCRs
- Video conferencing equipment
- Multimedia computers

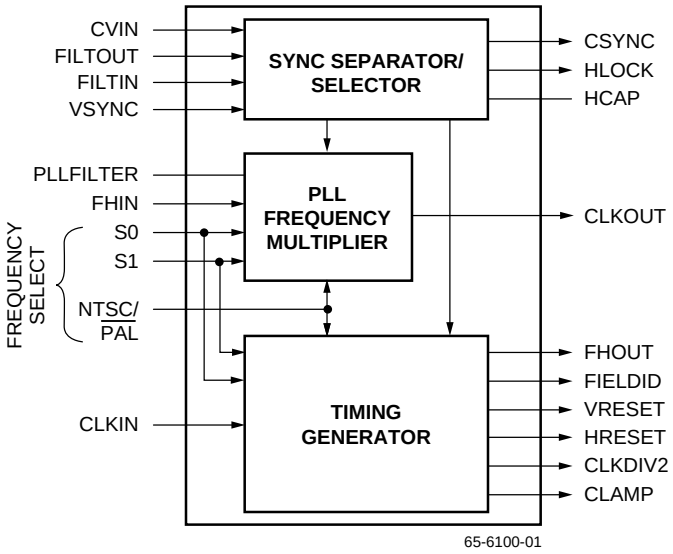
Description

The RC6100 contains a phase-locked loop (PLL) in a frequency multiplier configuration to generate a high-frequency clock as required for video A/D converter and digital video signal processing.

The device accepts composite video, composite sync or component sync signals as input. The output signals generated are: clamp gate, composite sync, horizontal sync, vertical sync, field ID, lock detector output, oscillator output (Clock), and Clock/2.

The NTSC output frequency choices are: 27.0, 25.175, 14.318, 13.5, 12.588, 12.273, 7.159, and 6.137 MHz. The PAL frequencies generated are: 27.0, 17.734, 15.0, 14.75, 13.5, 8.867, 7.5, and 7.375 MHz.

Logic Symbol



Block Diagram

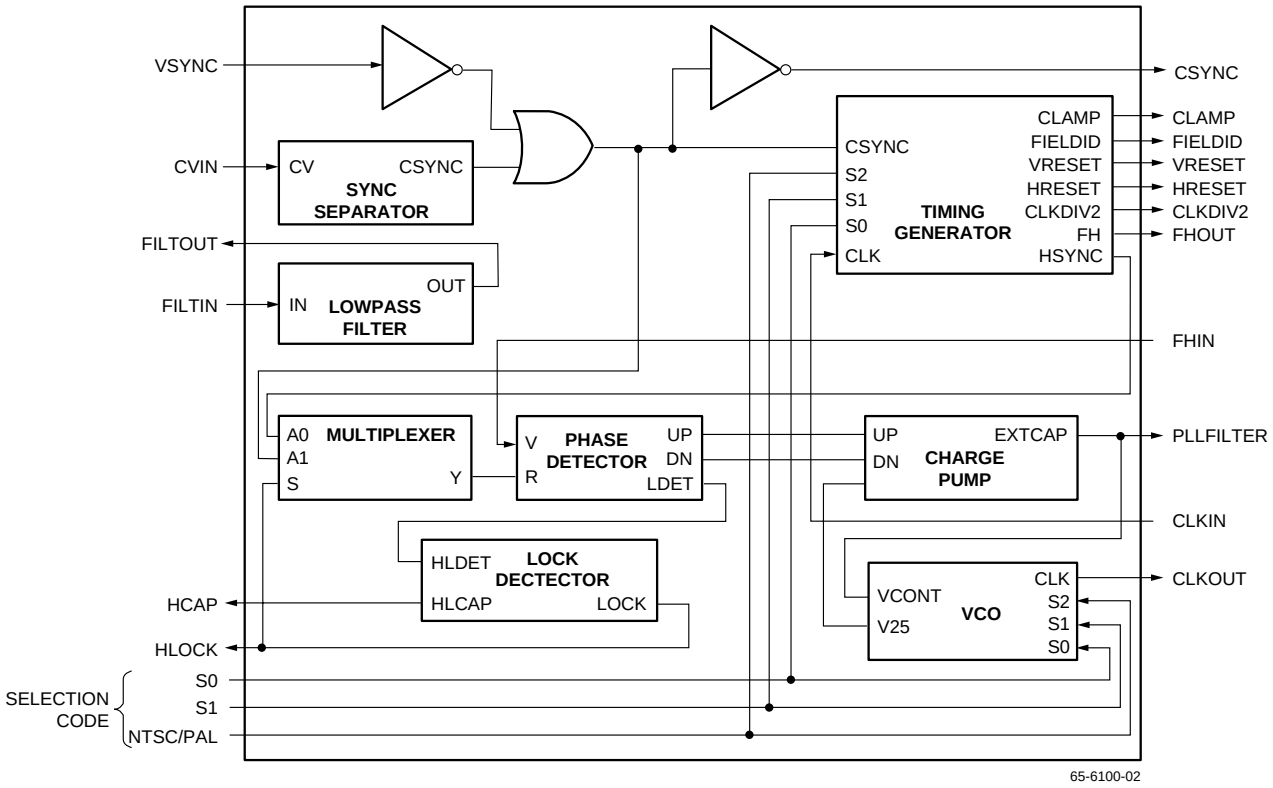


Figure 1.

Functional Description

The RC6100 block diagram is shown in Figure 1. Baseband composite video may be applied to either the FILTIN or CVIN input, depending upon whether the lowpass filter circuit function is desired. Use of the lowpass filter is desirable whenever the input video signal contains impulse noise or glitches that can cause jitter on the sync and clock output signals. Signals that require lowpass filtering should be input at FILTIN and the lowpass filter output (FILTOUT) should be connected to the CVIN input. However, video signals that do not require noise filtering should be input directly at CVIN to optimize performance. The FILTIN and CVIN inputs can also receive composite sync or horizontal sync signals at CMOS or TTL levels.

The input VSYNC is intended for those applications in which the horizontal and vertical sync signals have already been separated. In this mode, horizontal sync should be applied to CVIN and vertical sync applied to VSYNC. These two signals will be combined to form CSYNC and used by the timing generator to form HRESET, VRESET, and the other timing control signals. The VSYNC input is active low and is held at logic high via an internal bias network. If VSYNC is left open, there is no effect on signal processing.

The sync separator extracts a composite sync signal from the composite video, or creates composite sync from separate horizontal and vertical sync inputs. This signal is available at the CSYNC output. Composite sync is also used to control the timing generator, which is the workhorse function of the RC6100.

The timing generator contains programmable dividers for generating and controlling the pixel clock. The selection of pixel clock frequencies is controlled via logic inputs NTSC/PAL, S0, and S1. Table 1 shows the states of these inputs and the corresponding clock frequencies. The timing generator also provides the following output signals: CLAMP, VRESET, FIELDID, HRESET, FHOUT, and CLKDIV2. The CLAMP output is an active-low rectangular pulse of about 4 μs duration, the origination of which is timed by the rising-edge of CSYNC; the pulse is active during the horizontal back-porch interval, as shown in Figure 2. The CLAMP output is also active during the vertical blanking interval. The VRESET output is a short vertical sync signal that is logic low for the duration of the scan line that follows the first serration pulse of the vertical interval, as shown in Figure 3. HRESET is a horizontal sync signal that is set to logic low for one period of the pixel clock (CLKOUT); it is also phase coherent with the pixel clock. FHOUT is a clock signal at the horizontal frequency. It is normally connected to FHIN and used as the VCO (feedback) input to the loop phase comparator. The timing of HRESET relative to FHOUT is shown in Figure 4. (Note: the drawing exaggerates delays t1 and t2.) The FIELDID output goes to logic low immediately after the

VRESET pulse for RS170 Field 1 (the odd field) and toggles to logic high at the same time in the next field (see Figure 3). CLOCKDIV2 is the half-frequency pixel clock output; it is a 50-percent duty-cycle waveform. The Selection Codes of Table 1 (NTSC/PAL, S0, and S1) are input to the RC6100 to select the desired clock frequency to be output. The divisors shown in Table 1 indicate on-half the number of pixel clocks in each horizontal line. The pixel clock generator circuit (Figure 5) is formed by the Phase Detector, Charge Pump, external Loop Filter, and the VCO. The loop filter requires only a simple RC lag-lead network. When the PLL is locked, the VCO provides a pixel clock that is equal to $2*N*f_H$, (two times the horizontal scan frequency where N is the frequency divisor value). CLKOUT is normally connected to CLKIN, the clock input of the timing generator function. Note that a half-frequency pixel clock (CLKDIV2) is also generated. Both pixel clock outputs are 50-percent duty-cycle waveforms.

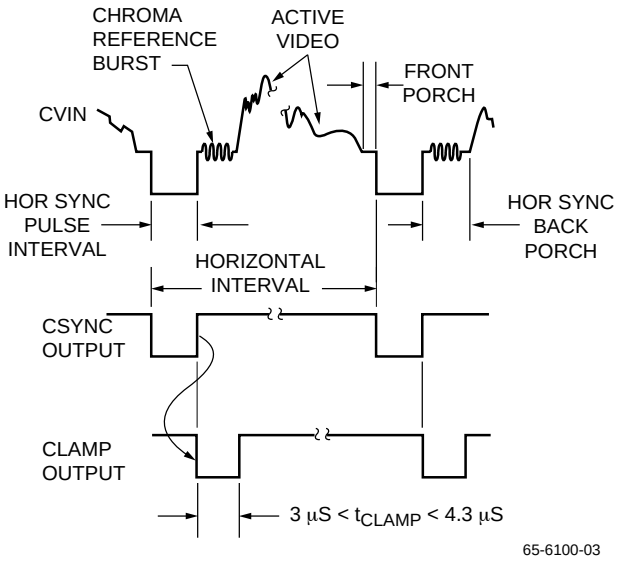
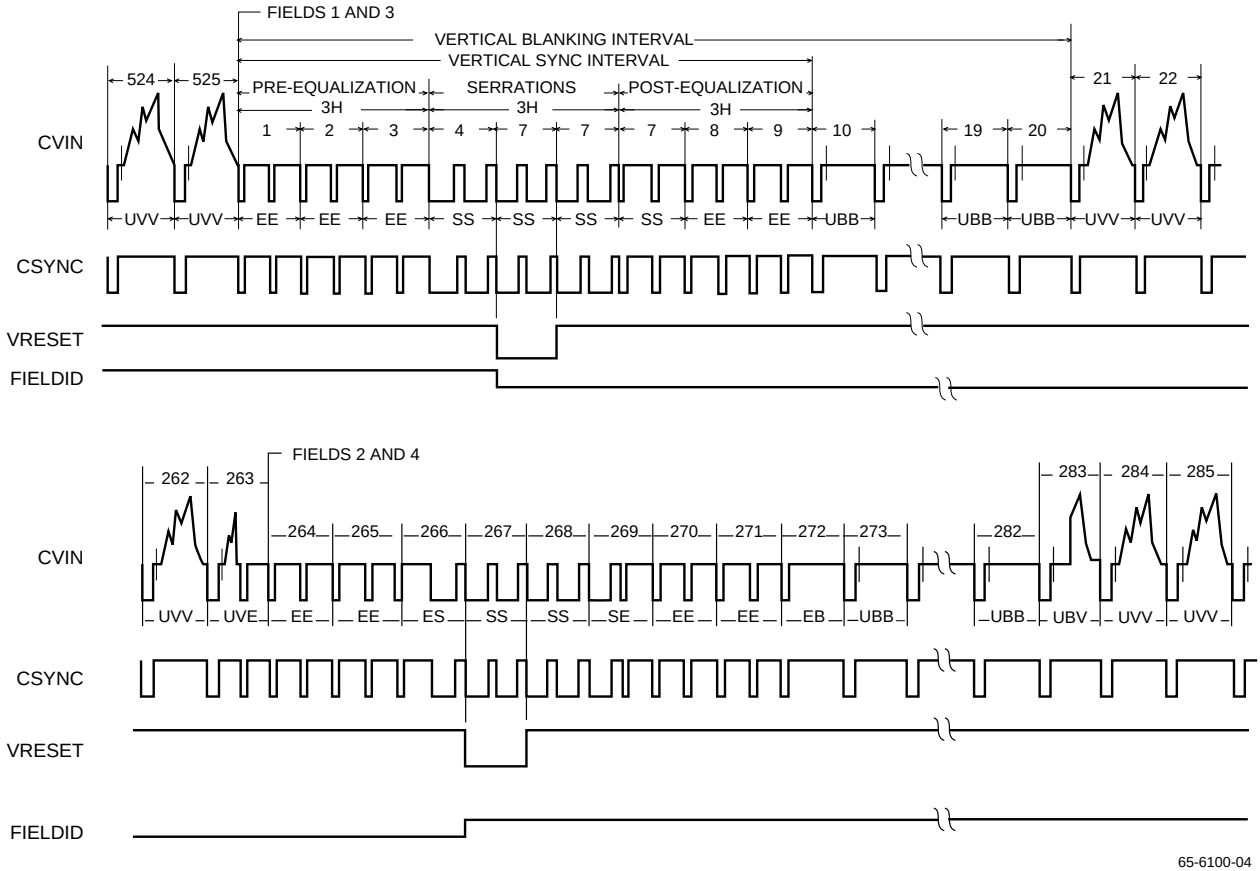


Figure 2. CLAMP Output Timing



Definitions:

UVV: active video
UVE: half-line video, half-line equalization pulse
EE: equalization pulse
EB: equalization broad pulse
SS: vertical sync pulse with serrations
ES: half-line equalization pulse, half-line vertical sync pulse
SE: half-line vertical sync pulse, half-line equalization pulse
UBV: half-line black, half-line video
UBB: black burst

Figure 3. VRESET Output TIming

Table 1. Clock Frequency Selection

Selection Codes			Frequencies (MHz) and Divisors (N)			
NTSC/ PAL	S1	S0	System	Clock Out	Clock/2 Out	Divide by N
1	0	0	NTSC (CCIR601)	27.0	13.5	858
1	0	1	NTSC (VGA)	25.175	12.588	800
1	1	0	NTSC (4fSC/Studio)	14.318	7.159	455
1	1	1	NTSC (Sq. Pixel)	12.273	6.137	390
0	0	0	PAL (CCIR601)	27.0	13.5	864
0	0	1	PAL (4fSC/Studio)	17.734	8.867	567.5
0	1	0	PAL	15.0	7.5	480
0	1	1	PAL (Sq. Pixel)	14.75	7.375	472

The timing performance of the phase lock is controlled by an external RC filter, the CSYNC signal, and internally-generated horizontal sync signals. When the PLL is not locked, CSYNC is selected as the reference input to the phase detector. CSYNC is derived directly from the composite video input, which contains the required horizontal edge information, and is not dependent upon the loop being locked. When the loop is locked, an internally generated horizontal sync signal from the timing generator is used for this reference input. CSYNC is only used as the loop reference input in the unlocked condition, because it contains serration pulses that would contribute undesirable jitter to the VCO output.

The lock-detect output signal (HLOCK) indicates when the phase reference and VCO inputs of the phase detector are locked. The response time of the lock detector is controlled by an external capacitor (C3) and, when lock is established, the HLOCK output goes low and the MUX makes the appropriate reference signal choice. The value of C3 was chosen to provide a lock-indication response time that is approximately 15 horizontal lines in duration, and an unlock-indication response time of approximately three horizontal lines in duration. Increasing the value of C3 would result in increasing both the lock and unlock response times.

The PLL consists of the phase detector, charge pump, loop filter, VCO, and divide-by-N counter. The phase detector is essentially a control loop summing junction. The charge pump, loop filter, and VCO are in the forward path, and the divide-by-N counter forms the feedback path. Stabilizing this control system consists of choosing the proper component values for the loop filter, such that sufficient phase margin exists at the unity-gain crossover frequency. The filter is a lag-lead network formed by the charge pump, C1, R1, and C2. Increasing the value of C1 moves the pole of the lag network (low pass) closer to the origin (lower frequency). This

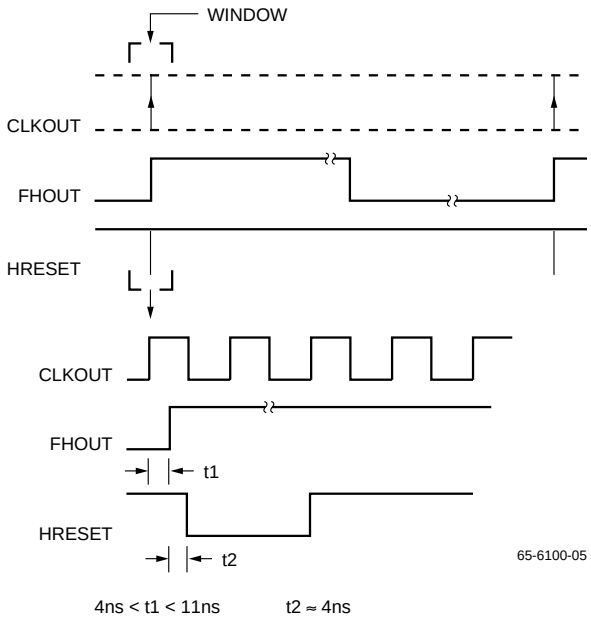


Figure 4. HRESET Output Timing

will reduce the loop bandwidth, which generally tends to reduce VCO jitter, but at a cost of settling (response) time and (in the extreme) stability. Table 2 shows values for R1, C1, and C2 for all input setings.

Increasing the value of either R1 or C2 moves the zero of the lead network (high pass) lower in frequency, which tends to increase loop gain at higher frequencies and can also result in poorer noise performance. The location of the zero is generally determined empirically to adjust the loop transfer function for adequate phase margin for a given desired bandwidth. The RC6100 loop settling time is approximately 400 μs, and lock detection requires about one millisecond.

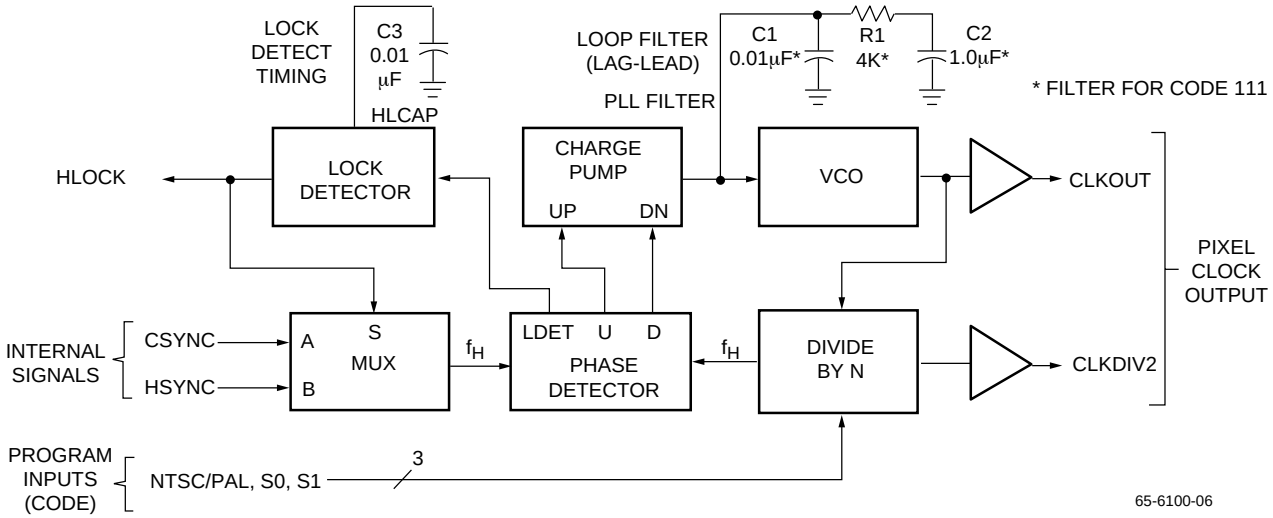


Figure 5. Pixel Clock Generator

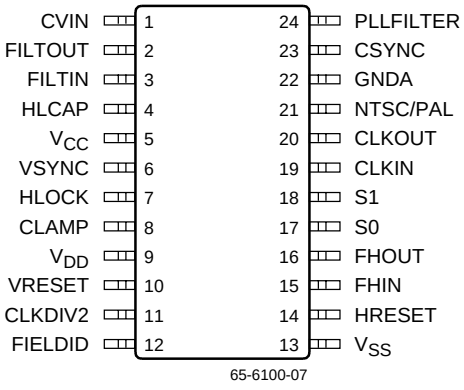
Table 2. PLL Filter Components

code	fin	fosc	Dividers		KVC0	KCP	R1	C2(K/20)	C1
			N	M					
100	15734	27.00E+06	1.00	858	2.66E+07	3.82E–05	4.17E+03	9.69E–07	9.69E–09
101	15734	25.18E+06	1.00	800	2.66E+07	3.82E–05	3.89E+03	1.04E–06	1.04E–08
110	15734	14.32E+06	2.00	455	2.51E+07	3.82E–05	4.68E+03	8.64E–07	8.64E–09
111	15734	12.27E+06	2.00	390	2.51E+07	3.82E–05	4.01E+03	1.01E–06	1.01E–08
000	15625	27.00E+06	1.00	864	2.66E+07	3.82E–05	4.17E+03	9.76E–07	9.76E–09
001	15625	17.73E+06	2.00	567.5	3.48E+07	3.82E–05	4.19E+03	9.72E–07	9.72E–09
010	15625	15.00E+06	2.00	480	2.48E+07	3.82E–05	4.97E+03	8.19E–07	8.19E–09
011	15625	14.75E	2.00	472	2.48E+07	3.82E–05	4.89E+03	8.33E–07	8.33E–09

Note:

1. Table values are ideal; actual values may vary by ±20% due to process variations.
2. Code: <NTSC/$\overline{\text{PAL}}$> <S1> <S0>

Pin Assignments



Pin Descriptions

Pin Name	Pin Number	Description
CVIN	1	This input accepts composite video.
FILTOUT	2	Output of low pass video input filter.
FILTIN	3	This input accepts either composite video, composite sync or horizontal sync signals. The input can be analog (1 Vpp) or TTL/CMOS logic levels.
HLCAP	4	Horizontal lock-detect timing capacitor.
V_{CC}	5	+5V power supply for analog circuits.
VSYNC	6	This input accepts vertical sync pulses for use when video input signals do not contain vertical sync components. This input is active low but remains high in normal operation. The input is TTL or CMOS compatible.
HLOCK	7	The locked-loop output indicates that the oscillator is phase-locked to the incoming horizontal sync. Sensitivity and delay time constant are set by an external capacitor. This output is CMOS or TTL compatible.
CLAMP	8	Clamp gate pulse output. This signal is approximately 4 μs in duration and is timed from the trailing edge of composite sync signal. The clamp gate is used by the video ADC and other video processing circuitry for DC restoration. This output is CMOS or TTL compatible.
V_{DD}	9	+5V power supply for digital circuits.
VRESET	10	Vertical sync signal output. This output is low during the line following the first serration pulse in the vertical sync interval. VRESET is CMOS or TTL compatible.
CLKDIV2	11	CLKOUT divided-by-two output frequency.
FIELDID	12	The field ID output signal is low following the VRESET pulse of RS170 field 1. This output is CMOS or TTL compatible.
V_{SS}	13	Digital ground.
HRESET	14	Horizontal reset signal is decoded from a programmable counter. This signal is coherent with the clock output and is one clock cycle in duration. This output is CMOS or TTL compatible.
FHIN	15	Horizontal frequency signal input; normally driven by FHOUT.
FHOUT	16	Horizontal frequency signal output.
S0, S1	17, 18	Frequency select inputs. They select one of four possible clock frequencies by providing the appropriate divide-by-N for the frequency-multiplying PLL. Table 1 shows the binary, frequency select codes. These inputs are TTL or CMOS compatible.
CLKIN	19	Clock input for internal timing functions; normally driven by CLKOUT.
CLKOUT	20	Buffered VCO output signal.
NTSC/PAL	21	This pin is used to select between NTSC or PAL frequencies of operation. A logic one selects the NTSC frequencies. See Table 1. These inputs are TTL or CMOS compatible.
GNDA	22	Analog ground.
CSYNC	23	Composite sync signal output. This signal is the sync separated from the video input, and is CMOS or TTL compatible.
PLLFILTER	24	PLL loop-compensation filter input.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Min.	Typ.	Max.	Units
Power Supply Voltage (V_{CC})			7	V
Input Voltage	V_{CC} + 0.3V ≥ V_{IN} ≥ GND – 0.3V			
Operating Temperature	0		70	°C
Storage Temperature	-40		125	°C
Junction Temperature			150	°C
Lead Soldering Temperature (10 sec)			300	°C

Note:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

Operating Conditions

Parameter		Min.	Typ.	Max.	Units
θ_{JA}	SO-24 thermal resistance		75		°C/W
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{CC}	Supply current		30	40	mA

DC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units
Logic Interface					
V_{IH}	Logic input high voltage	4			V
V_{IL}	Logic input low voltage			0.8	V
V_{OH}	Logic output high voltage	4			V
V_{OL}	Logic output low voltage			0.4	V
I_{IN}	Logic input current (V_{CC} ≥ VIN ≥ GND)			±30	μA
Analog Interface					
V_{IN}	Composite video signal (AC coupled)		1.0	2.0	V_{p-p}
I_{IN}	Input current (V_{IN} = V_{CC}–1V)			±700	μA
HLOCK	Lo @ 10mA		0.5	1.5	V
HLOCK	HI	3.5			V

AC Electrical Characteristics

V_{CC} = 5V, T_A = 0 to 70°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CS}	Composite sync amplitude	Maintains lock with horizontal rate jitter T_{HJ} of <10 ns	150		600	mV_{p-p}
V_{IN}	Impulse noise immunity	CVIN = 1 V_{p-p} + glitch; Glitch < 50 ns, Neg polarity, Voltage relative to blanking; Test for proper CSYNC output	0.3			V
f_{CLOCK}	Clock range		12.273		27.0	MHz
$\Delta HFOUT/\Delta V_{CC}$	VCO power supply rejection rate HFOUT = 27 MHz	4.5V < V_{CCA} < 5.5V			3.5	%/V
HFPULL	PLL Lock/Hold in Range	CVIN horizontal frequency	±500			Hz
	code 100	= 15734 Hz nominal		750		Hz
$t_{PD\ (VCS)}$	Video in to CSYNC delay			750		ns
$t_{PD\ (VHS)}$	Video in to HRESET delay			750		ns
$t_{PD\ (HCG)}$	H sync to CLAMPgate delay			300		ns
t_{DHS}	Duration of HRESET reset	fclk = 27 MHz	69	74	89	ns
t_{DCG}	Duration of CLAMPgate		3.0		4.5	µs
fclk jitter	DC=2.5v@PLL filter	2.5@VCOin code 100			1	ns
	Closed loop	CVin=15.734KHz, Code 100, fclk=27MHz		6	12	ns
	Capture Range	fin=15.734+500Hz to 15.625-500Hz	200			Hz
PLLFilter	Sink/source current		±150	240	±350	µA
CLDIV	VOL @ 4mA				0.8	V
	VOH		3.5			V

Typical Application

Figure 6 shows the RC6100 Horizontal Line Genlock used in a video signal-processing system. The part provides the clock that is required to synchronize the various elements of the system. Note that the clamp gate output of the RC6100 is applied to the convert input of the TMC1175 ADC.

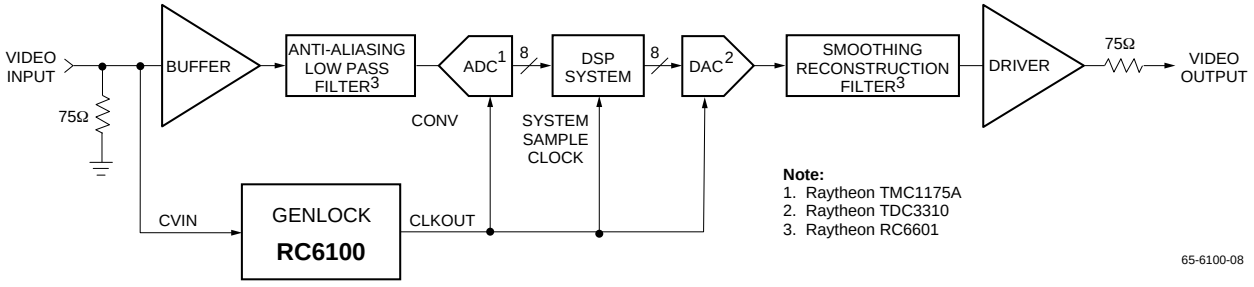
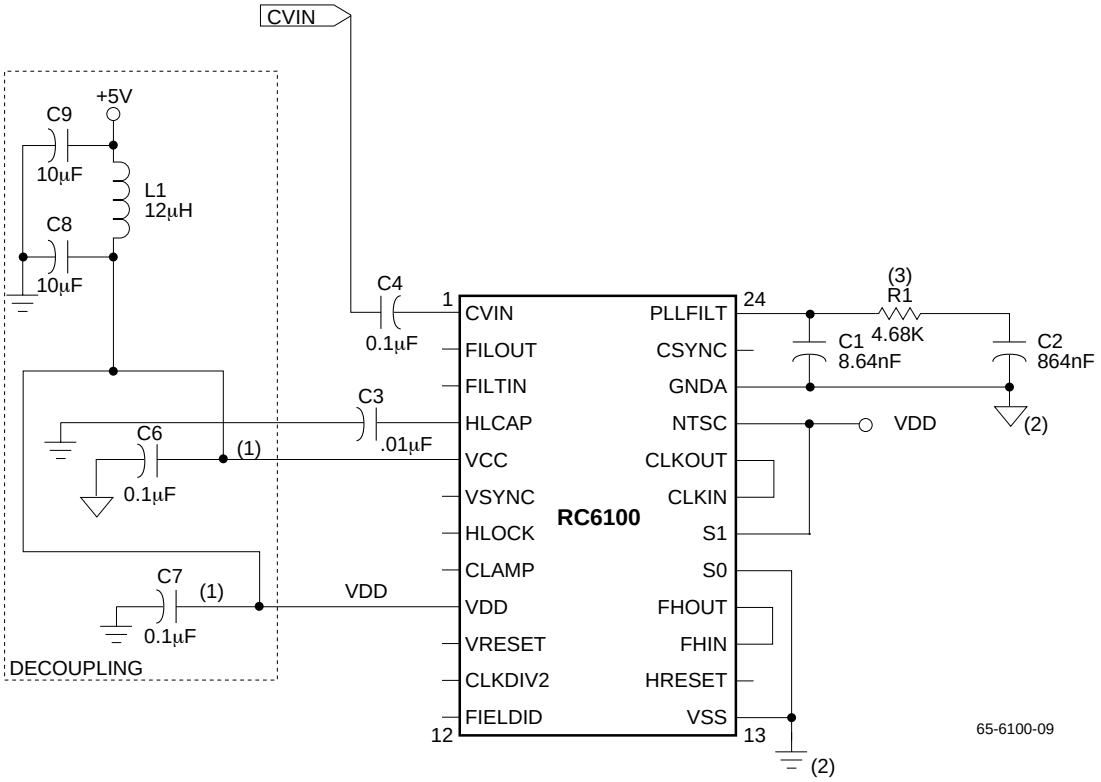


Figure 6. Application of RC6100 with TMC1175 and TDC3310 in Video Processing System

Application Circuit with Minimum Parts



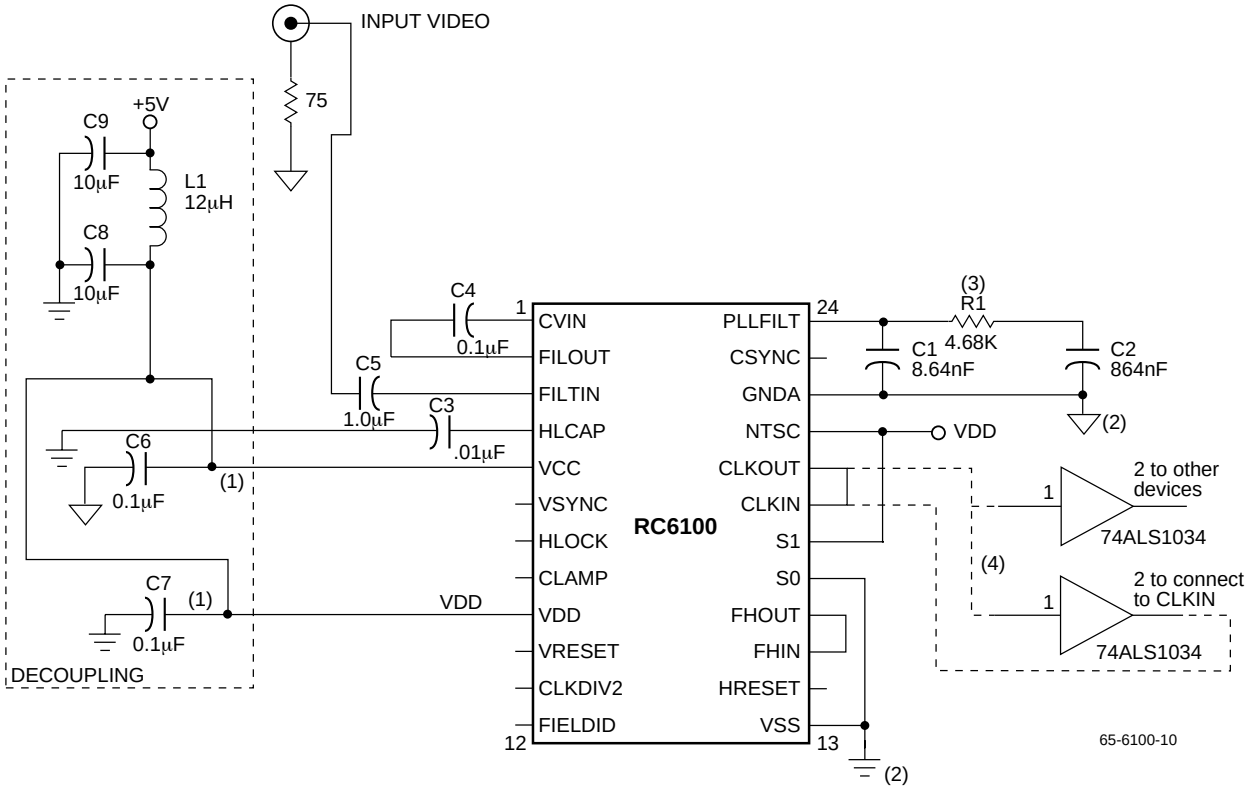
Notes:

1. Use a separate trace to each power pin and place capacitors C6 and C7 next to part.
2. Use separate ground plane for digital signals and PLL signals.

DIGITAL PLL

3. Place PLL filter components as close as possible to pin 24. Code 110.

Hook-up for Internal Filter



1. Use a separate trace to each power pin and place capacitors C6 and C7 next to part.
2. Use separate ground plane for digital signals and PLL signals.

DIGITAL PLL

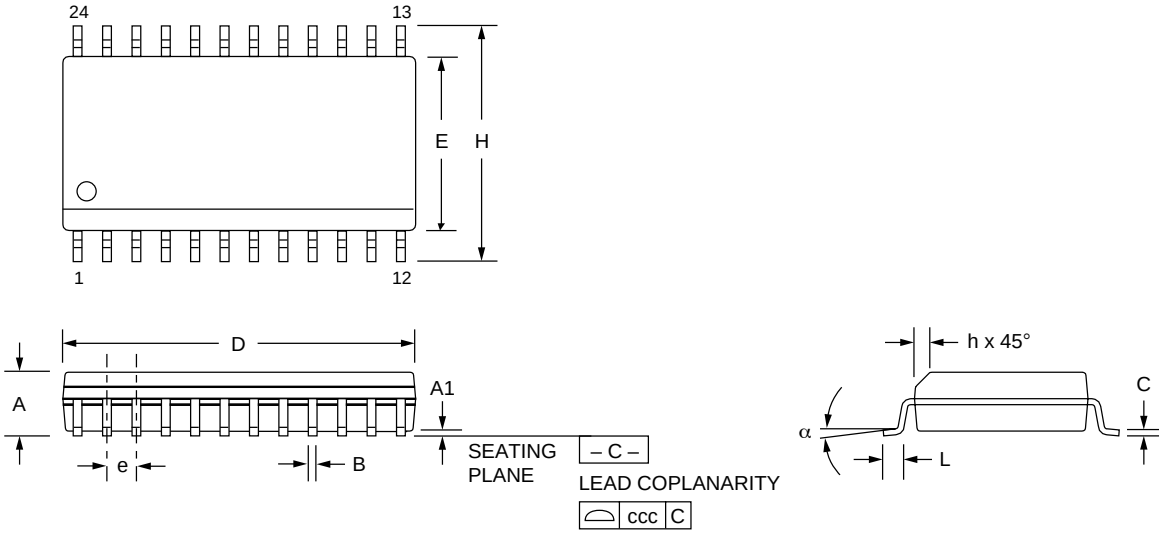
3. Place PLL filter components as close as possible to pin 24.
4. CLKOUT should be buffered for large trace runs or large fanout. Break CLKOUT, CLKIN, SHORT, and add buffers as shown.

Mechanical Dimensions – 24 Pin SOIC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.599	.614	15.20	15.60	2
E	.290	.299	7.36	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.020	0.25	0.51	
L	.016	.050	0.40	1.27	3
N	24		24		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
RC6100M	0°C to +70°C	Commercial	24 Pin Wide SOIC	RC6100M

5/20/98 0.0m 001
Stock#DS30006100