Application Bulletin AB-19

Layout Guideline for the RC7100 Motherboard System Clock

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Summary

The RC7100 is a motherboard frequency synthesizer that can generate clock frequencies from 66MHz to 100MHz. It contains 4 copies of the CPU clock and 8 copies of the PCI clock, 2 copies of the IOAPIC clock, 3 copies of the REF clock, and 2 copies of the 48MHz clock. Each clock source is capable of driving a 30pF load with an edge rate of 1.5V/nsec. When all clock outputs are enabled, there is no more than 250psec skew between each clock. Such high speed clocks generate noise on power supply lines of up to 300mV in amplitude, due to the high frequency and sharp edges driving heavy loads.

Unless proper isolation and a careful layout of the PC board are implemented, the power supply noise will propagate throughout the system, and may interfere with the proper operation of other devices, including that of the RC7100 itself. This Application Bulletin describes a suggested printed circuit board layout which will minimize clock jitter due to power supply noise, while reducing the component count of the overall system.

Board Layout Recommendations

At 100 MHz the parasitic capacitance effect of printed circuit boards becomes more significant than at lower frequencies. In particular, the high speed noise couples into power supplies via the board parasitic capacitance. Therefore, the power plane should not be directly below or above the signal traces. Instead, it should be *only* beneath the IC itself; this maximizes the effective distance between the power plane and signal, minimizing the capacitance.

Fairchild recommends the following techniques to minimize power supply noise.

1. The PCB should be at least two layers, with Power and Ground planes.

2. Minimize the distance between the VDD and GND planes to maximize the bypass capacitance.

3. Use multi-via pads for power and ground connections to reduce the effective impedance.

4. High Speed clock trace lengths should be as short as possible.

5. Both the 3.3V and 2.5V power planes should be isolated from the rest of the mother board through a filter; a specific filter is recommended below.

6. High Frequency bypass capacitors must be used at every VDD pin; specific values are recommended below.

7. Proper Termination should be used to minimize reflections.

8. Avoid sharp corners when routing high speed signals.

Additionally, for prototyping,

9. Sockets should not used for evaluating the RC7100.

Power Distribution Decoupling

Fairchild recommends placement of a 2.2nF high frequency bypass capacitor at *every* power pin to damp out power supply noise. A ceramic chip capacitor works fine here. Without the proper bypass capacitors, this power supply noise would feed back to the analog power supply via the common power plane. This would cause the output clocks to have more jitter.

In addition to the power pin capacitors, there should be one filter each for the 3.3V and 2.5V power supplies in order to isolate the noisy VDD from the rest of the motherboard. A common practice is use of a pi filter, as shown in Figure 1. The pi filter consists of a 100µF input tantalum capacitor, a ferrite bead with 32Ω impedance at 100MHz, and the parallel combination of a 33µF tantalum capacitor and a 100nF ceramic capacitor at the output. This filter attenuates noise in the frequency range of 40MHz to 100MHz. The filtered voltage is connected to a VDD island with a short and wide trace. The best place to put the VDD island is directly under the RC7100 chip, so that there are no signal crosses between the VDD and the high speed clocks. Use a separate layer for the 2.5V and the 3.3V so that each has the same arrangement. The island should be connected to each of the VDD pins.

The RC7100 has one PLL to synthesize CPU clock and a separate PLL to generate the fixed 48 MHz clock. Each PLL has a separate power supply pin. Pin 19 is the analog VCC of the PLL for CPU and Pin48 is of the VCC of the PLL for USB. These two analog pins should have at least 2.2nF high frequency bypass capacitors. The capacitors should be grounded with multi-via pads to minimize their effective impedance to ground.

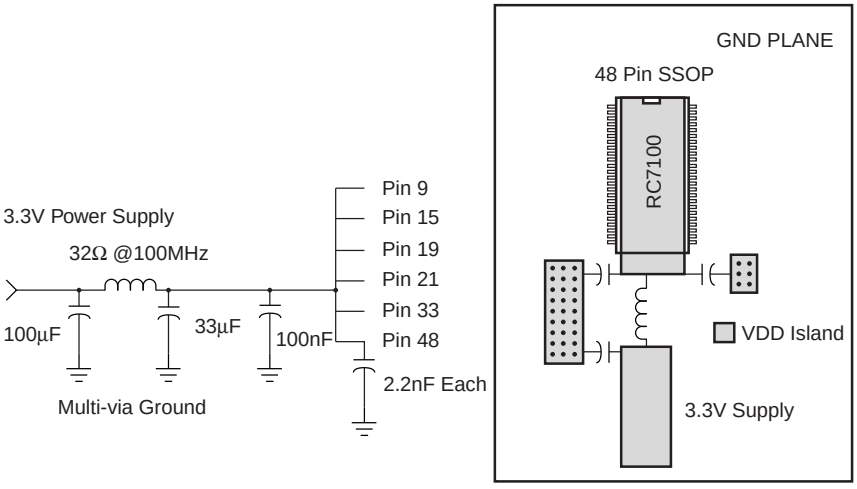

Figure 1. Recommended Power Supply Filter for the RC7100, with Physical Layout. The Same Pi Filter and Layout Should be Used for the 2.5V Power Supply, with the VDD Island on a Separate Layer.

For a sample PCB layout, please contact Fairchild Semiconductor.