# RC7105

## Clock Buffer/Driver

### Features

- Thirteen skew controlled CMOS clock outputs (SDRAM0:12)
- Drives three SDRAM DIMMs
- $I^2C$ interface
- Clock Skew between any two outputs is less than 250 ps
- 1 to 5ns propagation delay
- DC to 133MHz operation
- Single 3.3V supply voltage
- Low power CMOS design in a 28-pin, SOIC package

### Description

The Fairchild RC7105 is a low-voltage, thirteen-output clock buffer. The skew between any two outputs is less than 250 ps and the buffers can be individually enabled or disabled by programming via the $I^2C$ serial interface. Output buffer impedance is approximately 15Ω which is ideal for driving SDRAM DIMMs.

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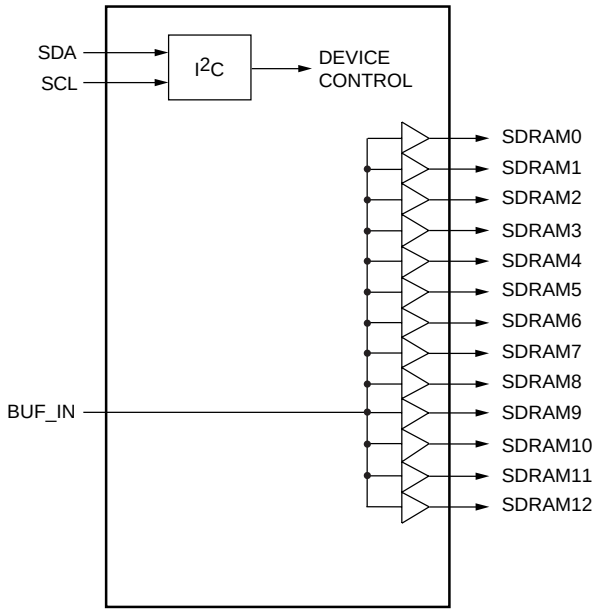
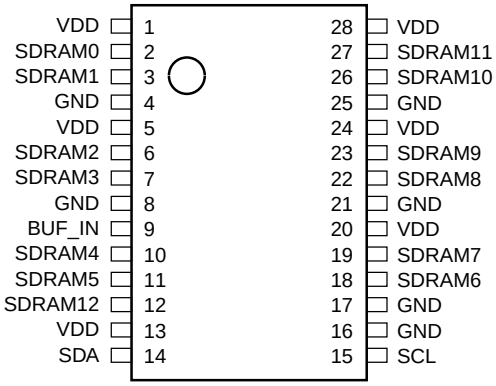
### Block Diagram



## Pin Assignments




## Pin Descriptions

| Pin Name | Pin Number | Type | Pin Function Description |
|---|---|---|---|
| SDRAM0:12 | 2, 3, 6, 7, 10, 11, 18, 19, 22, 23, 26, 27, 12 | OUT | **SDRAM Outputs:** Provides buffered copy of BUF_IN. The propagation delay from a rising input edge to a rising output edge is 1 to 5ns. All outputs are skew controlled to within ±250ps of each other. |
| BUF_IN | 9 | IN | **Clock Input:** This clock input has an input threshold voltage of 1.5V (typ). |
| SDA | 14 | IN/OUT | **$I^2C$ Data input:** Data should be presented to this input as described in the $I^2C$ section of this data sheet. |
| SCL | 15 | IN | **$I^2C$ clock input:** The $I^2C$ clock should be presented to this input as described in the $I^2C$ section of this data sheet. |
| VDD | 1, 5, 13, 20, 24, 28 | POWER | **Power Connection:** Power supply for core logic and output buffers. Connected to 3.3V supply. |
| GND | 4, 8, 16, 17, 21, 25 | GROUND | **Ground Connection:** Connect all ground pins to the common system ground plane. |

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## Absolute Maximum Ratings[1]

(beyond which the device will be damaged)

| Symbol | Parameter | Min. | Units |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any pin with respect to GND | -0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $T_B$ | Ambient Temperature under Bias | -55 to +125 | °C |
| $T_A$ | Operating Temperature | 0 to +70 | °C |

**Notes:**

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

## DC Electrical Characteristics

$T_A$ = 0°C to +70°C; $V_{DD}$ = 3.3V±5%

| Parameter | | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | |
| $I_{DD}$ | 3.3V Supply Current | BUF_IN = 100MHZ | | | 250 | mA |
| **Logic Input** | | | | | | |
| $V_{IL}$ | Input Low Voltage | | GND -0.3 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | VDD+.5 | V |
| $I_{ILEAK}$ | Input Leakage Current, BUF_IN | | -5 | | +5 | µA |
| $I_{ILEAK}$ | Input Leakage Current (Note) | | -20 | | +5 | µA |
| **Logic Outputs (SDRAM0:12)** | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 1mA | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = 1mA | 2.4 | | | V |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 1.4V | 55 | | 159 | mA |
| $I_{OH}$ | Output High Current | $V_{OH}$ = 1.4V | -188 | | -50 | mA |
| **Pin Capacitance/Inductance** | | | | | | |
| $C_{IN}$ | Input Pin Capacitance | | | | 5 | pF |
| $C_{OUT}$ | Output Pin Capacitance | | | | 6 | pF |
| $L_{IN}$ | Input Pin Inductance | | | | 7 | nH |

**Note:** SDA and SCL logic pins have an internal pull-up resistor.

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## AC Electrical Characteristics

$T_A$ = 0°C to +70°C; $V_{DD}$ = 3.3V±5%; (Lump Capacitance Test Load = 30pF)

| Parameter | | Min. | Typ. | Max. | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | 0 | | 133 | MHz | |
| $t_R$ | Output Rise Time | 0.5 | | 1.33 | ns | Measured from 0.4V to 2.4V |
| $t_F$ | Output Fall Time | 0.5 | | 1.33 | ns | Measured from 2.4V to 0.4V |
| $t_{SR}$ | Output Skew, Rising Edges | | | 250 | ps | |
| $t_{SF}$ | Output Skew, Falling Edges | | | 250 | ps | |
| $t_{EN}$ | Output Enable Time | 1.0 | | 8.0 | ns | |
| $t_{DIS}$ | Output Disable Time | 1.0 | | 8.0 | ns | |
| $t_{PR}$ | Rising Edge Propagation Delay | 1.0 | | 5.0 | ns | |
| $f_{PF}$ | Falling Edge Propagation Delay | 1.0 | | 5.0 | ns | |
| $t_D$ | Duty Cycle | 45 | | 55 | % | Measured at 1.5V |
| $Z_0$ | AC Output Impedance | | 15 | | Ω | Average value during switching transition. Used for determining series termination value. |

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# How To Use the Serial Data Interface

## Electrical Requirements

Figure 1 shows the architecture for the $I^2C$ serial interface bus used with the RC7105. Devices on the bus signal with an open drain logic output that actively pulls the bus line low, or lets the bus default to VDD (logic 1). The pull-up resistor on each bus line, SCL and SDA, establishes a default logic 1.

Although the RC7105 is a slave device which cannot write data on the bus, it does transmit an “acknowledge” data pulse after each byte is received. Thus, the SDA line is an I/O pin.

The pull-up resistor value should be designed to meet the rise and fall times specified in AC parameters, based on total bus line capacitance.

## Signaling Requirements

As demonstrated in Figure 2, the $I^2C$ protocol defines valid data bits as stable logic 0 or 1 condition on the SDA line during an SCL high (logic 1) pulse. A transitioning SDA line during an SCL high pulse may be read as a start or stop pulse.

Figure 3 shows how a “start bit” commands the beginning of a write sequence. The “stop bit” shown signifies that the sequence has ended. The RC7105 sends an “acknowledge” pulse after receiving eight data bits by asserting a low pulse on SDA, as shown in Figure 4.



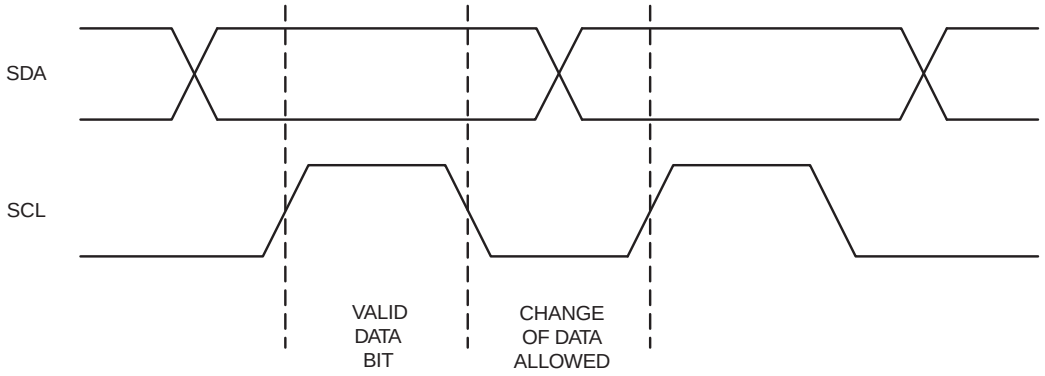


**Figure 2. Serial Data Bus Valid Data Bit**

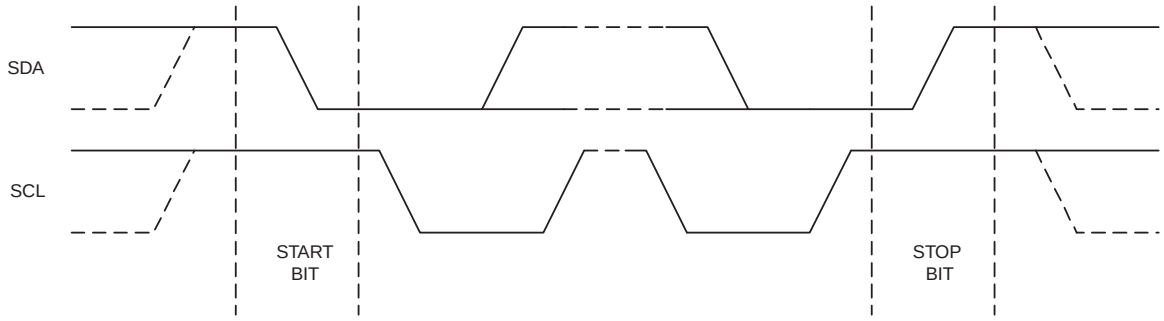


**Figure 3. Serial Data Bus Start and Stop Bit**

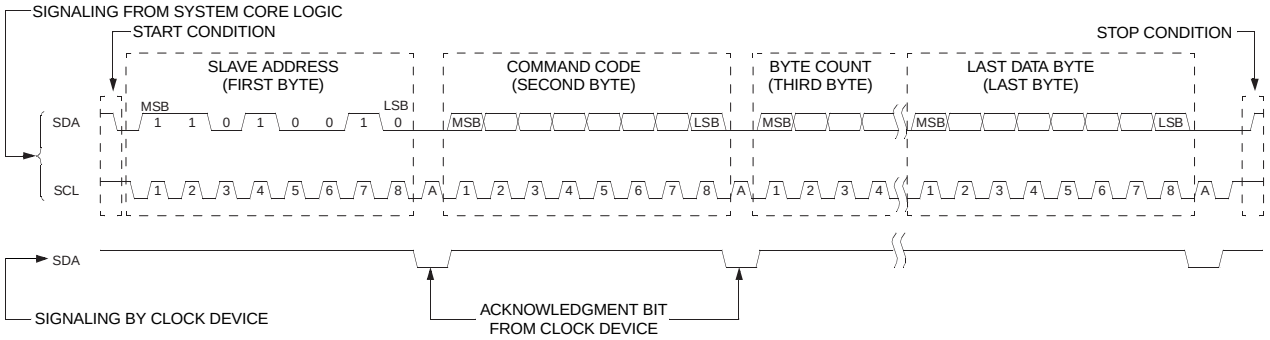


**Figure 4. Serial Data Bus Write Sequence**

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# Functional Description

## Output Drivers

The RC7105 uses CMOS type output buffers which drive the output rail-to-rail (GND to VDD) into typical capacitive loads. Because of this the outputs are both TTL and CMOS level compatible. Nominal output buffer impedance is 15Ω.

## Operation

The RC7105 is programmed by writing ten bytes of eight bits each. See Table 1 for byte sequence.

**Table 1. Byte Writing Sequence**

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---|---|---|---|
| 1 | Slave Address | 11010010 | Commands the RC7105 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7105 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2 | Command Code | Don't Care | Unused by the RC7105, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing ot another addressed slave receiver on the serial data bus. |
| 3 | Byte Count | Don't Care | Unused by the RC7105, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 4 | Data Byte 0 | Refer to Table 2 | The data bits in these bytes set internal RC7105 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 2, Data Byte Serial Configuration Map. |
| 5 | Data Byte 1 | | |
| 6 | Data Byte 2 | | |
| 7 | Data Byte 3 | Don't Care | Refer to Fairchild clock drivers. |
| 8 | Data Byte 4 | | |
| 9 | Data Byte 5 | | |
| 10 | Data Byte 6 | | |

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## Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function within the RC7105. Bit 7, the MSB, is written first. See Table 2 for bit descriptions of Data Bytes 0–2.

**Table 2. Data Bytes 0-2 Serial Configuration Map**

| Bit(s) | Affected Pin | | Control Function | Bit Control | |
|---|---|---|---|---|---|
| | Pin No. | Pin Name | | 0 | 1 |
| **Data Byte 0 SDRAM Active/Inactive Register (1=Enable, 0=Disable)** | | | | | |
| 7 | 11 | SDRAM5 | Clock Output Disable | Low | Active |
| 6 | 10 | SDRAM4 | Clock Output Disable | Low | Active |
| 5 | N/A | Reserved | (Reserved) | — | — |
| 4 | N/A | Reserved | (Reserved) | — | — |
| 3 | 7 | SDRAM3 | Clock Output Disable | Low | Active |
| 2 | 6 | SDRAM2 | Clock Output Disable | Low | Active |
| 1 | 3 | SDRAM1 | Clock Output Disable | Low | Active |
| 0 | 2 | SDRAM0 | Clock Output Disable | Low | Active |
| **Data Byte 1 SDRAM Active/Inactive Register (1=Enable, 0=Disable)** | | | | | |
| 7 | 27 | SDRAM11 | Clock Output Disable | Low | Active |
| 6 | 26 | SDRAM10 | Clock Output Disable | Low | Active |
| 5 | 23 | SDRAM9 | Clock Output Disable | Low | Active |
| 4 | 22 | SDRAM8 | Clock Output Disable | Low | Active |
| 3 | N/A | Reserved | (Reserved) | — | — |
| 2 | N/A | Reserved | (Reserved) | — | — |
| 1 | 19 | SDRAM7 | Clock Output Disable | Low | Active |
| 0 | 18 | SDRAM6 | Clock Output Disable | Low | Active |
| **Data Byte 2 SDRAM Active/Inactive Register (1=Enable, 0=Disable)** | | | | | |
| 7 | N/A | Reserved | (Reserved) | — | — |
| 6 | 12 | SDRAM12 | Clock Output Disable | Low | Active |
| 5 | N/A | Reserved | (Reserved) | — | — |
| 4 | N/A | Reserved | (Reserved) | — | — |
| 3 | N/A | Reserved | (Reserved) | — | — |
| 2 | N/A | Reserved | (Reserved) | — | — |
| 1 | N/A | Reserved | (Reserved) | — | — |
| 0 | N/A | Reserved | (Reserved) | — | — |

**Note:**
At power up all SDRAM outputs are enabled and active. Program all reserved bits to a”0”.

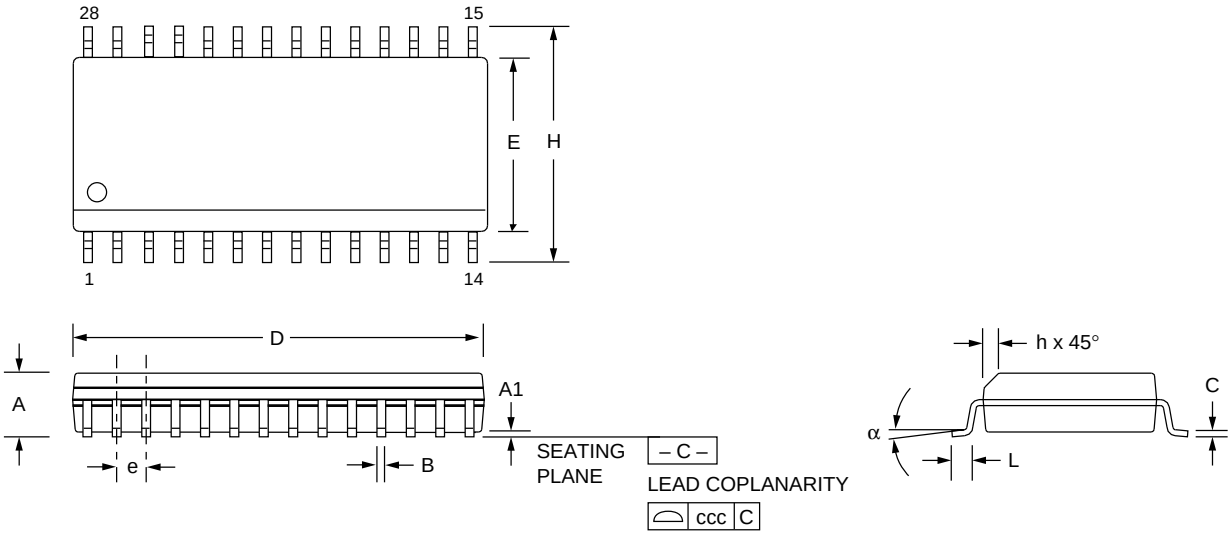
# Mechanical Dimensions

## 28 pin SOIC

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | .093 | .104 | 2.35 | 2.65 | |
| A1 | .004 | .012 | 0.10 | 0.30 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .009 | .013 | 0.23 | 0.32 | |
| D | .697 | .713 | 17.70 | 18.10 | 2 |
| E | .291 | .299 | 7.40 | 7.60 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .394 | .419 | 10.00 | 10.65 | |
| h | .010 | .030 | 0.25 | 0.75 | |
| L | .016 | .050 | 0.40 | 1.27 | |
| N | 28 | | 28 | | 5 |
| α | 0° | 7° | 0° | 7° | |
| ccc | — | .004 | — | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.

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## Ordering Information

| Product Number | Temperature | Screening | Package | Package Marking |
|---|---|---|---|---|
| RC7105 | 0°C to +70°C | | 28 SOIC | RC7105 |

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