RC7104

100MHz Spread Spectrum Motherboard Clock

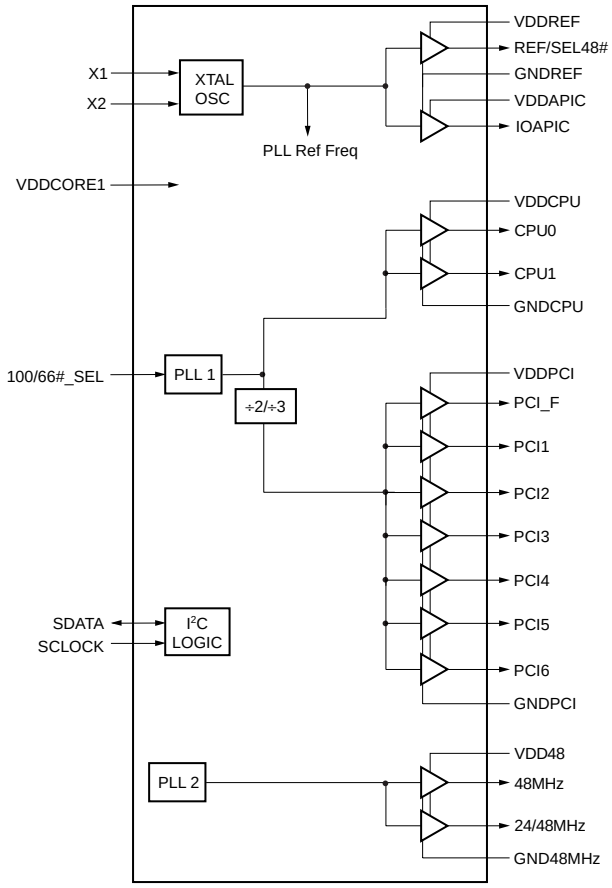
Features

- Employs Fairchild's proprietary Spread Spectrum Technology
- Reduces measured EMI by as much as 10dB
- I^2C programmable
- Two skew-controlled copies of CPU clock
- SEL100/66# selects CPU frequency (100 or 66.8MHz)
- Overclocking up to 133MHz
- Seven copies of PCI clock (synchronous w/CPU clock)
- One copy of 14.31818 MHz IOAPIC clock
- One copy of 48MHz USB clock
- 24 or 48MHz clock is determined by resistor straps on power up
- One copy of 14.31818MHz REF clock

Description

The RC7104 is a clock synthesizer for Pentium II based motherboard systems. The CPU output frequency can be "over driven" through a command to the serial I^2C interface.

Block Diagram



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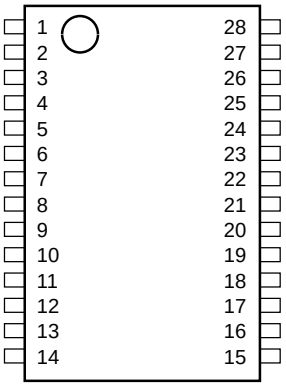
Rev. 0.0.9

Table 1. Pin Selectable Frequency

SEL100/66	CPU(0:1)	PCI
1	100MHz	33.3MHz
0	66.8MHz	33.4MHz

Pin Assignments



Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name
1	X1	8	PCI4	15	GND48	22	CPU0
2	X2	9	VDDPCI	16	SEL100/66#	23	VDDCPU
3	GNDPCI	10	PCI5	17	SCLOCK	24	IOAPIC
4	PCIF	11	PCI6	18	SDATA	25	VDDAPIC
5	PCI1	12	VDD48	19	GNDCPU	26	VDDREF
6	PCI2	13	48MHz	20	VDDCORE1	27	REF/SEL48#
7	PCI3	14	24/48MHz	21	CPU1	28	GNDREF

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Pin Descriptions

Pin Name	Pin Number	Type	Pin Function Description
CPU0:1	22, 21	OUT	**CPU Clock Outputs 0 through 1:** These two CPU clocks run at a frequency set by SEL100/66# and the I^2C bus.
PCI_F PCI1:6	4, 5, 6, 7, 8, 10, 11	OUT	**PCI Bus Clock Outputs 1 through 6 and PCI_F:** These seven PCI clock outputs run synchronously to the CPU clock.
IOAPIC	24	OUT	**I/O APIC Clock Output:** Provides 14.318MHz fixed frequency.
48MHz	13	OUT	**48MHz Output:** Fixed 48MHz USB clock.
24/48MHz	14	OUT	**24MHz or 48MHz Output:** Frequency is set by the state of pin 27 on power up.
REF/SEL48#	27	IN/OUT	**I/O Dual Function REF and SEL48# pin:** Upon power-up, the state of SEL48# is latched. The initial state is set by either a 10K resistor to GND or to VDD. A 10K resistor to GND causes pin 14 to output 48MHz. If the pin is strapped to VDD, pin 14 will output 24MHz. After 2ms, the pin becomes a high drive output that produces a copy of 14.318MHz.
SEL100/66#	16	IN	**Frequency Selection Input:** Selects CPU clock frequency as shown in Table 1.
SDATA	18	IN/OUT	**I^2C Data Pin:** Data should be presented to this input as described in the I^2C section of this data sheet. Internal 250K ohm pull-up resistor.
SCLOCK	17	IN	**I^2C clock Pin:** The I^2C Data clock should be presented to this input as described in the I^2C section of this data sheet.
X1	1	IN	**Crystal Connection or External Reference Frequency Input:** Connect to either a 14.318MHz crystal or other reference signal.
X2	2	IN	**Crystal Connection:** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected.
VDDCORE1	20	POWER	**Power Connection:** Power supply for core logic and PLL circuitry. Connect to 3.3V supply.
VDDPCI	9	POWER	**Power Connection:** Power supply for PCI_F and PCI1:6. Connect to 3.3V supply.
VDDAPIC	25	POWER	**Power Connection:** Power supply for IOAPIC output buffer. Connect to 2.5V supply.
VDDCPU	23	POWER	**Power Connection:** Power supply for CPU0:1 output buffers. Connect to 2.5V supply.
VDD48	12	POWER	**Power Connection:** Power supply for 48MHz USB clock. Connect to 3.3V supply.
VDDREF	26	POWER	**Power Connection:** Power supply for 14.318MHz ISA clock. Connect to 3.3V supply.
GNDPCI, GND48, GND-CPU, GNDREF	3, 15, 19, 28	GROUND	**Ground Connections:** Connect all ground pins to the common system ground plane.

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Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Symbol	Parameter	Rating	Units
V_{DD}, V_{IN}	Voltage on any pin with respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C
V_{ESD}	Input ESD Protection	2 (min)	kV

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DC Electrical Characteristics

T_A = 0°C to +70°C; VDDREF = VDDPCI = VDD48MHz = 3.3V±5%; VDDAPIC = VDDCPU = 2.5V±5%

Parameter		Test Condition	Min.	Typ.	Max.	Units
Supply Current						
I_{DD}	Combined 3.3V Supply Current	CPUCLK = 100MHz Outputs Loaded[1]				mA
Logic inputs						
V_{IL}	Input Low Voltage		GND -.3		0.8	V
V_{IH}	Input High Voltage		2.0		VDD+.3	V
I_{IL}	Input Low Current[2]				-25	µA
I_{IH}	Input High Current[2]				10	µA
I_{IL}	Input Low Current (SEL100/66#)				-5	µA
I_{IH}	Input High Current (SEL100/66#)				+5	µA
Clock Outputs						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.4	mV
V_{OH}	Output High Voltage CPU0, IOAPIC	I_{OH} = 1mA	2			V
	PCI, REF, 24MHz		2.4			
I_{OL}	Output Low Current CPU, IOAPIC	V_{OL} = 1.2V	27		93	mA
	PCI	V_{OL} = 1.4V	26.5		139	
	REF, 48MHz, 24MHz		25		76	
I_{OH}	Output High Current CPU, IOAPIC	V_{OH} = 1.2V	-101		-26	mA
	PCI	V_{OH} = 1.4V	-189		-31	
	REF, 48MHz, 24MHz		-94		-27	
Crystal oscillator						
V_{TH}	X1 Input threshold Voltage[3]			1.5		V
$C_{IN, X1}$	X1 Input Capacitance[5]	Pin X2 unconnected	13.5	18	22.5	pF
Pin Capacitance/Inductance						
C_{IN}	Input Pin Capacitance	Except X1 and X2			5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{IN}	Input Pin Inductance				7	nH

Notes:

1. All clock outputs loaded with maximum lump capacitance test load specified in AC Electrical Characteristics section.
2. RC7104 logic inputs have internal pull-up resistors, except SEL100/66#.
3. X1 input threshold voltage (typical) is VDD/2.
4. The RC7104 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driven X1 with an external clock source (X2 is left unconnected).

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AC Electrical Characteristics

T_A = 0°C to +70°C; VDDREF = VDDPCI = VDD48MHz = 3.3V±5%; VDDAPIC = VDDCPU = 2.5V±5%; f_{XTL} = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled

CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6MHz			CPU = 100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_P	Period	15		15.5	10		10.5	ns	Measured on rising edge at 1.25.
t_H	High Time	5.2			3.0			ns	Duration of clock cycle above 2.0V.
t_L	Low Time	5.0			2.8			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	.4		1.6	.4		1.6	ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	.4		1.6	.4		1.6	ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	45		55	%	Measured on rising and falling edge at 1.25V.
t_{JC}	Jitter, Cycle-to-Cycle			200			200	ps	Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			175			175	ps	Measured on rising edge at 1.25V.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20			20		Ω	Average value during switching transition. Used for determining series termination value.

PCI Clock Outputs, PCI1:6 and PCI_F (Lump Capacitance Test Load = 30pF)

Parameter		CPU = 66.6/100MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
t_P	Period	30			ns	Measured on rising edge at 1.5V.
t_H	High Time	12.0			ns	Duration of clock cycle above 2.4V.
t_L	Low Time	12.0			ns	Duration of clock cycle below 0.4V.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			250	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
t_{SK}	Output Skew			500	ps	Measured on rising edge at 1.5V.
t_O	CPU to PCI Clock Offset	1.5		4.0	ns	Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output.

PCI Clock Outputs, PCI1:6 and PCI_F (Lump Capacitance Test Load = 30pF) (continued)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		30		Ω	Average value during switching transition. Used for determining series termination value.

IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f	Frequency, Actual		14.3818		MHz	Frequency generated by crystal oscillator.
t_R	Output Rise Edge Rate	1		4	V/ns	Measured from 0.4V to 2.0V.
t_F	Output Fall Edge Rate	1		4	V/ns	Measured from 2.0V to 0.4V.
t_D	Duty Cycle	45		55	%	Measured on rising and falling edge at 1.25V.
t_A	Jitter, Absolute			500	ps	Measured on rising edge at 1.25V. Maximum deviation of clock period.
f_{ST}	Frequency Stabilization from Power-up (cold start)			1.5	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

REF Clock Output (Lump Capacitance Test Load = 20pF)

Parameter		CPU = 66.6/100MHz Min.	Typ.	Max.	Units	Test Condition/Comments
f	Frequency, Actual		14.3818		MHz	Determined by PLL divider ratio (see n/m below).
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		Ω	Average value during switching transition. Used for determining series termination value.

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48MHz and 24MHz Clock Output (Lump Capacitance Test Load = 20pF=66.6/100MHz)

Parameter		CPU = 66.6MHz			Units	Test Condition/Comments
		Min.	Typ.	Max.		
f	Frequency, Actual		48.008 24.004		MHz	Determined by PLL divider ratio (see n/m below).
f_D	Deviation from 48MHz		+167		ppm	(48.008 – 48)/48
n/m	PLL Ratio		57/17			(14.31818MHz x 57/17 = 48.008MHz)
t_R	Output Rise Edge Rate	0.5		2	V/ns	Measured from 0.4V to 2.4V.
t_F	Output Fall Edge Rate	0.5		2	V/ns	Measured from 2.4V to 0.4V.
t_D	Duty Cycle	45%		55	%	Measured on rising and falling edge at 1.5V.
t_{JC}	Jitter, Cycle-to-Cycle			500	ps	Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles.
f_{ST}	Frequency Stabilization from Power-up (cold start)			3	ms	Assumes full supply voltage reached within 1ms from power-up.
Z_0	AC Output Impedance		20		ohm	Average value during switching transition. Used for determining series termination value.

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Functional Description

I/O Pin Operation

Pin 27 is a dual purpose l/O pin. The RC7104 upon power up, the first 2ms of operation is used for input logic selection, (allowing the determination of assigned device functions).

During this period, the 48MHz clock output buffer is tristated, allowing the output strapping resistor on the l/O pin to pull the pin and its associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic "0" or "1" condition of the l/O pin is then latched. Next the output buffer is enabled which converts the l/O pin into an operating clock output. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be re-set by turning VDD off and then back on again. (This feature reduces device pin count by combining clock outputs with input select pins.)

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is 20 ohms (nominal) which is minimally affected by the 10 kohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the l/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

An external 10 kohm "strapping" resistor is connected between the l/O pin and ground or VDD. Connection to ground sets a "0" bit, connection to VDD sets a "1" bit. Figure 1 and Figure 2 show two suggested methods for strapping resistor connections.

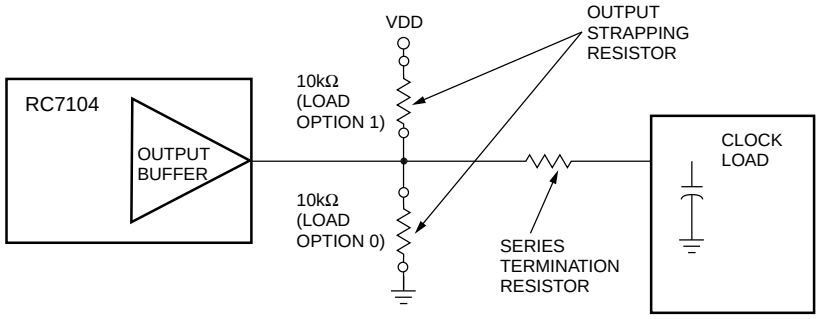

Figure 1. Input Logic Selection through Resistor Load Option

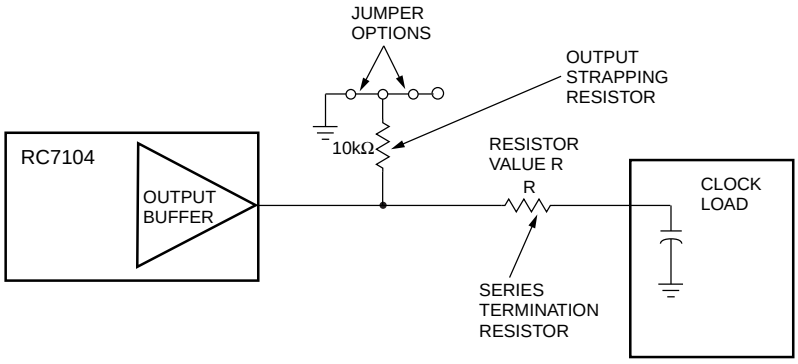

Figure 2. Input Logic Selection through Jumper Option

Serial Data Interface

The RC7104 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7104 initializes with default register settings. Therefore, the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset.

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Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 2 summarizes the control functions of the serial data interface.

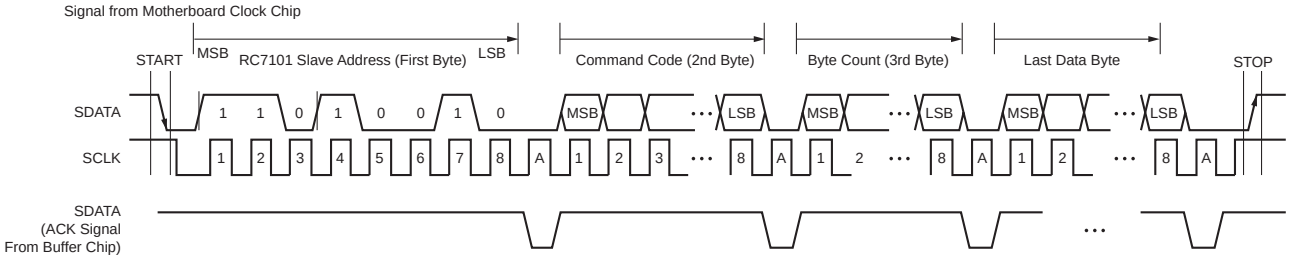
Table 2. Serial Data Interface Control Functions Summary

Control Function	Description	Common Application
Clock Output Disable	Any individual clock output(s) can be disabled. Disabled outputs are actively held low.	Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots.
CPU Clock Frequency Selection	Provides CPU/PCI frequency selections beyond the 100 and 66.66MHz selections that are provided by the SEL100/66# pin. Frequency is changed in a smooth and controlled fashion.	For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation.
Output Tristate	Puts all clock outputs into a high impedance state.	Production PCB testing.
Test Mode	All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 4.	Production PCB testing.
(Reserved)	Reserved function for future device revision or production device testing.	No user application. Register bit must be written as 0.

Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.

RC7104 I²C Interface Write Sequence Example



Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

The data transfer rate is 100kbits/s in the standard mode and 400kbits/s in the fast mode. The serial protocol uses block writes only. Bytes are written with the lowest first and the highest last with the ability to stop after any complete byte has been transferred. The clock driver is a slave/receiver only and is only capable of receiving data with the exception of sending acknowledgements. It is not capable of sending data.

Operation

The RC7104 is programmed by writing 10 bytes of eight bits each. See Table 3 for byte order.

Table 3. Byte Writing Sequence

Byte Sequence	Byte Name	Bit Sequence	Byte Description
1	Slave Address	11010010	Commands the RC7104 to accept the bits in Data Bytes 3-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7104 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver).
2	Command Code	Don' t Care	Unused by the RC7104, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
3	Byte Count	Don't Care	Unused by the RC7104, therefore bit values are ignored (don' t care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus.
4	Data Byte 0	Don' t Care	Refer to Fairchild SDRAM Buffers. These bytes are not used by the RC7104.
5	Data Byte 1		
6	Data Byte 2		
7	Data Byte 3	Refer to Table 5	The data bits in these bytes set internal RC7104 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 4, Data Byte Serial Configuration Map.
8	Data Byte 4		
9	Data Byte 5		
10	Data Byte 6		

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Writing Data Bytes

Each bit of the 10 data bytes controls a particular device function except for the "reserved" bits. These must by preserved by writing a logic 0. Bit 7, the MSB, is written first. See Table 4 for bit descriptions of Data Bytes 3–6.

Table 5 shows additional frequency selections that are programmable via the serial data interface.

Table 7 shows the mode select functions for Byte 3, bits 1 and 0.

Table 4. Data Bytes 3-6 Serial Configuration Map

Bit(s)	Affected Pin		Control Function		Bit Control		Default
	Pin No.	Pin Name			0	1	
Data Byte 3							
7	—	—	(Reserved)		—	—	0
6	—	—	SEL_2		Refer to Table 5		0
5	—	—	SEL_1		Refer to Table 5		0
4	—	—	SEL_0		Refer to Table 5		0
3	—		BYT0 _FS#		Frequency Controlled by external SEL100/ 66# pin	Frequency Controlled by BYT0 SEL (2:0)	0
2	—		(Reserved)				0
1-0	—	—	Bit 1	Bit 0	Function (See Table 7 for function details)		00
			0	0	Normal Operation		
			0	1	Test Mode		
			1	0	Spread Spectrum on (See Table 6 for frequency & spread selections, when Spread Spectrum is on. See Table 5 for frequency selections when Spread Spectrum is off).		
			1	1	All Outputs Tristated		
Data Byte 4							
7	—	—	(Reserved)		—	—	0
6	14	24/48MHz	Clock Output disable		Low	Active	1
5	—	—	(Reserved)		—	—	0
4	—	—	(Reserved)		—	—	0
3	—	—	(Reserved)		—	—	0
2	21	CPU1	Clock Output disable		Low	Active	1
1	—	—	(Reserved)		—	—	0
0	22	CPU0	Clock Output disable		Low	Active	1
Data Byte 5							
7	4	PCICLK_F	Clock Output disable		Low	Active	1
6	11	PCI6	Clock Output disable		Low	Active	1
5	10	PCI5	Clock Output disable		Low	Active	1
4	—	—	(Reserved)		—	—	0
3	8	PCI4	Clock Output disable		Low	Active	1
2	7	PCI3	Clock Output disable		Low	Active	1
1	6	PCI2	Clock Output disable		Low	Active	1
0	5	PCI1	Clock Output disable		Low	Active	1

Table 4. Data Bytes 3-6 Serial Configuration Map (continued)

Bit(s)	Affected Pin		Control Function	Bit Control		Default
	Pin No.	Pin Name		0	1	
Data Byte 6						
7	—	—	(Reserved)	—	—	0
6	—	—	(Reserved)	—	—	0
5	24	IOAPIC	Clock Output disable	Low	Active	1
4	—	—	(Reserved)	—	—	0
3	—	—	(Reserved)	—	—	0
2	—	—	(Reserved)	—	—	0
1	27	REF	Clock Output disable	Low	Active	1
0	—	—	(Reserved)	—	—	0

Table 5. Additional Frequency Selections through Serial Data Interface Data Bytes when Spread Spectrum is turned off

Input Conditions			Output Frequency	
Data Byte 3, Bit 3 = 1				
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)
0	0	0	124.3	62.2
0	0	1	75.2	37.6
0	1	0	83.5	41.8
0	1	1	66.8	33.4
1	0	0	103.2	34.4
1	0	1	112.3	37.4
1	1	0	133.6	44.5
1	1	1	100.2	33.4

Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes when Spread Spectrum is turned on

Input Conditions			Output Frequency		
Data Byte 3, Bit 3 = 1					
Bit 6 SEL_2	Bit 5 SEL_1	Bit 4 SEL_0	CPU, SDRAM Clocks (MHz)	PCI Clocks (MHz)	Spread Percentage
0	0	0	124	41.3	±0.25% Center
0	0	1	75	37.5	±0.25% Center
0	1	0	83.3	41.6	±0.25% Center
0	1	1	66.8	33.4	±0.25% Center
1	0	0	103	34.25	±0.25% Center
1	0	1	112	33.3	±0.25% Center
1	1	0	133.3	44.43	±0.25% Center
1	1	1	100	33.3	±0.25% Center

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Table 7. Select Function for Data Byte 3, Bits 0:1

Function	Input Conditions		Output Frequency				
	Data Byte 3						
	Bit 1	Bit 0	CPU0:1	PCI_F, PCI1:6	REF, IOAPIC	48MHz	24MHz
Normal Operation	0	0	[1]	[1]	14.318MHz	48MHz	24MHz
Test Mode	0	1	X1/2	CPU/2 or 3	X1	X1/2	X1/4
Spread Spectrum	1	0	±0.5%	±0.5%	14.318MHz	48MHz	24MHz
Tristate	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

Notes:

1. CPU and PCI frequency selections are listed in Table 1 and Table 5.

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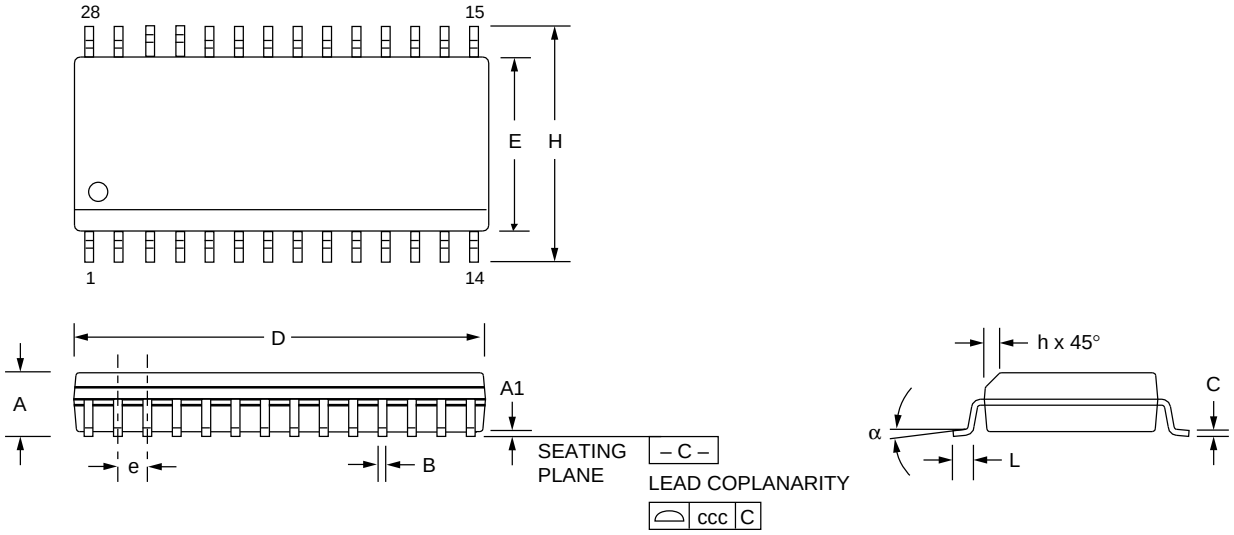
Mechanical Dimensions

28 pin SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	
D	.697	.713	17.70	18.10	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.030	0.25	0.75	
L	.016	.050	0.40	1.27	
N	28		28		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. Symbol "N" is the maximum number of terminals.



Advanced Information

Ordering Information

Product Number	Temperature	Screening	Package	Package Marking
RC7104			28 SOIC	RC7104

Advanced Information