# RC7102

## BX Spread Spectrum Frequency Synthesizer for Pentium II®

### Features

- Maximized EMI suppression using Fairchild's proprietary Spread Spectrum Technology
- Single chip system frequency synthesizer for Intel BX chip set
- Two copies of CPU output
- Six copies of PCI output
- One 48MHz output for USB
- One 24MHz output for SIO
- Two buffered reference outputs
- One IOAPIC output
- Fourteen SDRAM outputs provide support for 3 DIMMs
- Supports frequencies up to 150MHz
- $I^2C$ interface for programming
- Power management control inputs
- Smooth CPU frequency switching from 66.8

### Description

The RC7102 was developed as a single chip device to meet the clocking needs of the Intel BX™ chipset. In addition to the typical outputs provided by standard 100 MHz BX™ FTG's, the RC7102 adds a fourteen output buffer, supporting SDRAM DIMM modules in conjunction with the chipset.

Fairchild's proprietary spread spectrum frequency synthesis technique is a feature of the CPU and PCI outputs. When enabled, this feature reduces the peak EMI measurements by up to 10dB.

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### Block Diagram

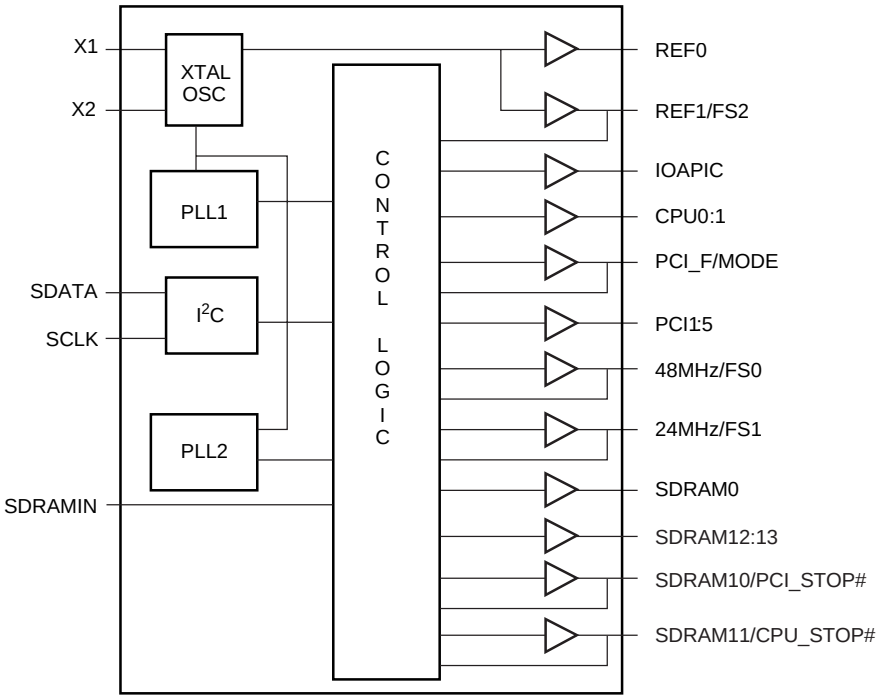


**Table 1. Mode Input Table**

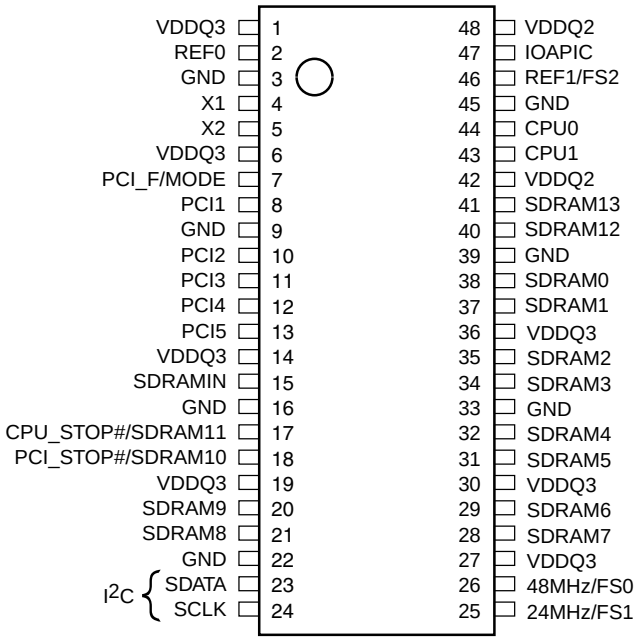
| Mode | Pin 17 | Pin 18 |
|---|---|---|
| 0 | CPU-STOP# | PCI_STOP# |
| 1 | SDRAM11 | SDRAM10 |

**Table 2. Pin Selectable Frequency**

| Input Address | | | CPU Outputs (MHz) | PCI Outputs (MHz) |
|---|---|---|---|---|
| FS2 | FS1 | FS0 | | |
| 1 | 1 | 1 | 100 | 33.3 (CPU/3) |
| 1 | 1 | 0 | 133.3 | 44.4 (CPU/3) |
| 1 | 0 | 1 | 112 | 37.3 (CPU/3) |
| 1 | 0 | 0 | 103 | 34.3 (CPU/3) |
| 0 | 1 | 1 | 66.8 | 33.4 (CPU/2) |
| 0 | 1 | 0 | 83.3 | 41.7 (CPU/2) |
| 0 | 0 | 1 | 75 | 37.5 (CPU/2) |
| 0 | 0 | 0 | 124 | 41.3 (CPU/3) |

## Pin Assignments

**48 pin SSOP**

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## Pin Assignments

| Pin Name | Pin Number | Type | Pin Function Description |
|---|---|---|---|
| CPU0:1 | 43, 44 | OUT | **CPU Outputs:** The CPU clock outputs are controlled by the CLK_STOP# control pin. |
| PCI1:5 | 8, 10, 11, 12, 13 | OUT | **PCI Clock Outputs 1 through 5:** These five PCI clock outputs are controlled by the PCI_STOP# control pin. |
| MODE/PCI_F | 7 | IN/OUT | **Fixed PCI Clock Output:** Frequency is set by the FS0:2 inputs or through serial input interface. (see Tables 2 and 6) This output is not affected by the PCI_STOP# input. Upon power-up MODE input will be latched, which will enable or disable SDRAM10 and SDRAM11. (see Tables 1 and 2) |
| CPU_STOP#/ SDRAM11 | 17 | IN/OUT | **$\overline{\text{CPU\_STOP}}$ Input:** When brought low, the CPU clock outputs are stopped low after completing a full clock cycle. |
| IOAPIC | 47 | OUT | **IOAPIC Clock Output:** Provides 14.318MHz fixed frequency. The output voltage swing is controlled by VDDQ2.. |
| 48MHz/FS0 | 26 | IN/OUT | **48MHz Output:** 48MHz is provided in normal operation. In standard systems, this output can be used as the reference for the Universal Serial Bus. Upon power-up FS0 input will be latched, which will set clock frequencies as described in Table 2. |
| 24MHz/FS1 | 25 | IN/OUT | **24MHz Output:** 24MHz is provided in normal operation. In standard systems, this output can be used as the clock input for a Super I/O chip. Upon power-up FS1 input will be latched, which will set clock frequencies as described in Table 2. |
| REF1/FS2 | 46 | IN/OUT | **I/O Dual Function REF1 and FS2 pin:** Upon power-up, FS2 input will be latched which will set clock frequencies as described in Table 2. When an output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins. |
| REF0 | 2 | OUT | REF0 output, this pin provides a fixed clock signal equal in frequency to the reference signal provided at the X1/X2 pins. |
| SDRAMIN | 15 | IN | **Buffered Input Pin:** The signal provided to this input pin is buffered to 14 outputs (SDRAM0:13). |
| SDRAM0:13 | 38, 37, 35, 34, 32, 31, 29, 28, 21, 20, 18, 17, 40, 41 | OUT | **Buffered Outputs:** These fourteen dedicated outputs provide copies of the signal provided at the SDRAMIN input. The swing is set by VDDQ3, and if the CPU clock is used to drive the SDRAMIN then they are deactivated when CPU_STOP# input is set low. |
| SCLK | 24 | IN | Clock pin for $I^2C$ Circuitry. |
| SDATA | 23 | IN/OUT | Data pin for $I^2C$ Circuitry. |
| X1 | 4 | IN | **Crystal Connection or External Reference Frequency Input:** This pin has dual functions. It can be used as an external 14.318MHz crystal connection or as an external reference frequency input. |
| PCI_STOP#/ SDRAM10 | 18 | IN/OUT | **SDRAM10 or PCI_STOP# Pin:** Function determined by MODE pin. The PCI_STOP# input enables the PCI 1:5 outputs when high and causes them to remain at logic 0 when low. |
| X2 | 5 | IN | **Crystal Connection:** An input connection for an external 14.318MHz crystal. If using an external reference, this pin must be left unconnected. |
| VDDQ3 | 1, 6, 14, 19, 27, 30, 36 | POWER | **Power Connection:** Power supply for core logic, PLL circuitry, SDRAM outputs, PCI outputs, reference outputs, 48MHz output, and 24MHz output. Connect to 3.3V supply |

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## Pin Assignments (continued)

| Pin Name | Pin Number | Type | Pin Function Description |
|---|---|---|---|
| VDDQ2 | 42, 48 | POWER | **Power Connection:** Power supply for IOAPIC, CPU_F, and CPU1 output buffers. Connect to 2.5V. |
| GND | 3, 9, 16, 22, 33, 39, 45 | GROUND | **Ground Connections:** Connect all ground pins to the common system ground plane. |

## Absolute Maximum Ratings[1]

(beyond which the device will be damaged)

| Symbol | Parameter | Rating | Unit |
|---|---|---|---|
| $V_{DD}$, $V_{IN}$ | Voltage on any pin with respect to GND | –0.5 to +7.0 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $T_B$ | Ambient Temperature under Bias | –55 to +125 | °C |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $ESD_{PROT}$ | Input ESD Protection | 2 (min) | kV |

**Notes:**

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.

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## DC Electrical Characteristics

$T_A$ = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%

| Parameter | | | Min. | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| **Supply Current** | | | | | | | |
| $I_{DD}$ | 3.3V Supply Current | | | TBD | | mA | CPU0:1 = 100Mhz Outputs Loaded[1] |
| $I_{DD}$ | 2.5V Supply Current | | | TBD | | mA | CPU0:1 = 100Mhz Outputs Loaded[1] |
| **Logic Inputs** | | | | | | | |
| $V_{IL}$ | Input Low Voltage | | GND -.3 | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | | 2.0 | | VDD +.3 | V | |
| $I_{IL}$ | Input Low Current[2] | | | | -25 | µA | |
| $I_{IH}$ | Input High Current[2] | | | | 10 | µA | |
| **Clock Outputs** | | | | | | | |
| $V_{OL}$ | Output Low Voltage | | | | 0.4 | V | $I_{OL}$ = 1mA |
| $V_{OH}$ | Output High Voltage | | 2.4 | | | V | $I_{OH}$ = 1mA |
| $V_{OH}$ | Output High Voltage | CPU0:1, IOAPIC | 2.0 | | | V | $I_{OH}$ = -1mA |
| $I_{OL}$ | Output Low Current: | CPU0:1 | 27 | | 93 | mA | $V_{OL}$ = 1.2V |
| | | IOAPIC | 27 | | 93 | mA | $V_{OL}$ = 1.2V |
| | | PCI_F, PCI1:5 | 26.5 | | 139 | mA | $V_{OL}$ = 1.4V |
| | | SDRAM0:13 | 55 | | 152 | mA | $V_{OL}$ = 1.4V |
| | | REF0:1 | 25 | | 76 | mA | $V_{OL}$ = 1.4V |
| | | 48MHz | 25 | | 76 | mA | $V_{OL}$ = 1.4V |
| | | 24Mhz | 25 | | 76 | mA | $V_{OL}$ = 1.4V |
| $I_{OH}$ | Output High Current | CPU_F, CPU1 | -101 | | -26 | mA | $V_{OH}$ = 1.2V |
| | | IOAPIC | -101 | | -26 | mA | $V_{OH}$ = 1.2V |
| | | PCI_F, PCI1:5 | -189 | | -31 | mA | $V_{OH}$ = 1.4V |
| | | SDRAM0:13 | -188 | | -50 | mA | $V_{OH}$ = 1.4V |
| | | REF0:1 | -94 | | -27 | mA | $V_{OH}$ = 1.4V |
| | | 48MHz | -94 | | -27 | mA | $V_{OH}$ = 1.4V |
| | | 24MHz | -94 | | -27 | mA | $V_{OH}$ = 1.4V |
| **Crystal Oscillator** | | | | | | | |
| $V_{TH}$ | X1 Input threshold Voltage (Note 3) | | | 1.65 | | V | VDDQ3 = 3.3V |
| $C_{IN,X1}$ | X1 Input Capacitance (Note 5) | | | 18 | | pF | Pin X2 unconnected |
| **Pin Capacitance/Inductance** | | | | | | | |
| $C_{IN}$ | Input Pin Capacitance | | | | 5 | pF | Except X1 and X2 |
| $C_{OUT}$ | Output Pin Capacitance | | | | 6 | pF | |
| $L_{IN}$ | Input Pin Inductance | | | | 7 | nH | |

**Notes:**

1. All clock outputs loaded with 6" 60 ohm traces with 22pF capacitors.
2. RC7102 logic inputs have internal pull-up devices (pull-ups not full CMOS level).
3. X1 input threshold voltage (typical) is VDD/2.
4. The RC7102 contains an internal crystal load capacitor between pin X1 and ground and another between pin X2 and ground. Total load placed on crystal is 14pF; this includes typical stray capacitance of short PCB traces to crystal.
5. X1 input capacitance is applicable when driving X1 with an external clock source (X2 is left unconnected).

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## AC Electrical Characteristics

$T_A$ = 0°C to +70°C; VDDQ3 = 3.3V±5%; VDDQ2 = 2.5V±5%; $f_{XTL}$ = 14.31818MHz

AC clock parameters are tested and guaranteed over stated operating conditions using the stated lump capacitive load at the clock output; Spread Spectrum clocking is disabled.

### CPU Clock Outputs, CPU0:1 (Lump Capacitance Test Load = 20pF)

| Parameter | | CPU = 66.6MHz | | | CPU = 100MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| $t_P$ | Period | 15 | | 15.5 | 10 | | 10.5 | ns | Measured on rising edge at 1.25. |
| $t_H$ | High Time | 5.2 | | | 3.0 | | | ns | Duration of clock cycle above 2.0V. |
| $t_L$ | Low Time | 5.0 | | | 2.8 | | | ns | Duration of clock cycle below 0.4V. |
| $t_R$ | Output Rise Edge Rate | 1 | | 4 | 1 | | 4 | V/ns | Measured from 0.4V to 2.0V. |
| $t_F$ | Output Fall Edge Rate | 1 | | 4 | 1 | | 4 | V/ns | Measured from 2.0V to 0.4V. |
| $t_D$ | Duty Cycle | 45 | | 55 | 45 | | 55 | % | Measured on rising and falling edge at 1.25V. |
| $t_{JC}$ | Jitter, Cycle-to-Cycle | | | 250 | | | 250 | ps | Measured on rising edge at 1.25V. Maximum difference of cycle time between two adjacent cycles. |
| $t_{SK}$ | Output Skew | | | 175 | | | 175 | ps | Measured on rising edge at 1.25V. |
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | 3 | | | 3 | ms | Assumes full supply voltage reached within 1ms from power-up. |
| $Z_0$ | AC Output Impedance | | 20 | | | 20 | | ohm | Average value during switching transition. Used for determining series termination value. |

### PCI Clock Outputs, PCI_F and PCI_1:5 (Lump Capacitance Test Load = 30pF)

| Parameter | | CPU = 66.6/ 100MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $t_P$ | Period | 30 | | | ns | Measured on rising edge at 1.5V. |
| $t_H$ | High Time | 12.0 | | | ns | Duration of clock cycle above 2.4V. |
| $t_L$ | Low Time | 12.0 | | | ns | Duration of clock cycle below 0.4V. |
| $t_R$ | Output Rise Edge Rate | 1 | | 4 | V/ns | Measured from 0.4V to 2.4V. |
| $t_F$ | Output Fall Edge Rate | 1 | | 4 | V/ns | Measured from 2.4V to 0.4V. |
| $t_D$ | Duty Cycle | 45 | | 55 | % | Measured on rising and falling edge at 1.5V. |
| $t_{JC}$ | Jitter, Cycle-to-Cycle | | | 500 | ps | Measured on rising edge at 1.5V. Maximum difference of cycle time between two adjacent cycles. |
| $t_{SK}$ | Output Skew | | | 500 | ps | Measured on rising edge at 1.5V. |
| $t_O$ | CPU to PCI Clock Skew | 1.5 | | 4.0 | ns | Covers all CPU/PCI outputs. Measured on rising edge at 1.5V. CPU leads PCI output. |
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | | ms | Assumes full supply voltage reached within 1ms from power-up. |

### PCI Clock Outputs, PCI_F and PCI_1:5 (Lump Capacitance Test Load = 30pF) (continued)

| Parameter | | CPU = 66.6/ 100MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $Z_0$ | AC Output Impedance | | 30 | | ohm | Average value during switching transition. Used for determining series termination value. |

### IOAPIC Clock Output (Lump Capacitance Test Load = 20pF)

| Parameter | | CPU = 66.6/ 100MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| f | Frequency, Actual | | 14.3818 | | MHz | Frequency generated by crystal oscillator. |
| $t_R$ | Output Rise Edge Rate | 1 | | 4 | V/ns | Measured from 0.4V to 2.0V. |
| $t_F$ | Output Fall Edge Rate | 1 | | 4 | V/ns | Measured from 2.0V to 0.4V. |
| $t_D$ | Duty Cycle | 45 | | 55 | % | Measured on rising and falling edge at 1.25V. |
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | 1.5 | ms | Assumes full supply voltage reached within 1ms from power-up. |
| $Z_0$ | AC Output Impedance | | 15 | | ohm | Average value during switching transition. Used for determining series termination value. |

### REF0:1 Clock Output (Lump Capacitance Test Load = 20pF)

| Parameter | | CPU = 66.6/ 100MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| f | Frequency, Actual | | 14.3818 | | MHz | Frequency generated by crystal oscillator. |
| $t_R$ | Output Rise Edge Rate | 0.5 | | 2 | V/ns | Measured from 0.4V to 2.4V. |
| $t_F$ | Output Fall Edge Rate | 0.5 | | 2 | V/ns | Measured from 2.4V to 0.4V. |
| $t_D$ | Duty Cycle | 45% | | 55 | % | Measured on rising and falling edge at 1.5V. |
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | 3 | ms | Assumes full supply voltage reached within 1ms from power-up. |
| $Z_0$ | AC Output Impedance | | 40 | | ohm | Average value during switching transition. Used for determining series termination value. |

### 48MHz Clock Output (Lump Capacitance Test Load = 20pF)

| Parameter | | CPU = 66.6MHz | | | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| f | Frequency, Actual | | 48.008 | | MHz | Determined by PLL divider ratio (see n/m below). |
| $f_D$ | Deviation from 48MHz | | +167 | | ppm | (48.008 – 48)/48 |
| m/n | PLL Ratio | | 57/17 | | | (14.31818MHz x 57/17 = 48.008MHz) |
| $t_R$ | Output Rise Edge Rate | 0.5 | | 2 | V/ns | Measured from 0.4V to 2.4V. |
| $t_F$ | Output Fall Edge Rate | 0.5 | | 2 | V/ns | Measured from 2.4V to 0.4V. |
| $t_D$ | Duty Cycle | 45% | | 55 | % | Measured on rising and falling edge at 1.5V. |

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### 48MHz Clock Output (Lump Capacitance Test Load = 20pF) (continued)

| Parameter | | CPU = 66.6MHz Min. | Typ. | Max. | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | 3 | ms | Assumes full supply voltage reached within 1ms from power-up. |
| $Z_0$ | AC Output Impedance | | 40 | | ohm | Average value during switching transition. Used for determining series termination value. |

### 24MHz Clock Output (Lump Capacitance Test Load = 20pF)

| Parameter | | CPU = 66.6MHz Min. | Typ. | Max. | Units | Test Condition/Comments |
|---|---|---|---|---|---|---|
| f | Frequency, Actual | | 24.004 | | MHz | Determined by PLL divider ratio (see n/m below). |
| $f_D$ | Deviation from 24MHz | | +167 | | ppm | (24.004 – 24)/24 |
| m/n | PLL Ratio | | 57/34 | | | (14.31818MHz x 57/34 = 24.004MHz) |
| $t_R$ | Output Rise Edge Rate | 0.5 | | 2 | V/ns | Measured from 0.4V to 2.4V. |
| $t_F$ | Output Fall Edge Rate | 0.5 | | 2 | V/ns | Measured from 2.4V to 0.4V. |
| $t_D$ | Duty Cycle | 45% | | 55 | % | Measured on rising and falling edge at 1.5V. |
| $f_{ST}$ | Frequency Stabilization from Power-up (cold start) | | | 3 | ms | Assumes full supply voltage reached within 1ms from power-up. |
| $Z_0$ | AC Output Impedance | | 40 | | ohm | Average value during switching transition. Used for determining series termination value. |

### SDRAM Clock Outputs, SDRAM0:13 (Lump Capacitance Test Load =30pF)

| Parameter | | Min. | Typ. | Max. | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| $f_{IN}$ | Input Frequency | 0 | | 150 | MHz | |
| $t_R$ | Output Rise Time | 0.5 | | 1.33 | nS | Measured from 0.4V to 2.4V |
| $t_F$ | Output Fall Time | 0.5 | | 1.33 | nS | Measured from 2.4V to 0.4V |
| $t_{SR}$ | Output Skew, Rising Edge | | | 250 | pS | |
| $t_{SF}$ | Output Skew, Falling Edge | | | 250 | pS | |
| $t_{EN}$ | Output Enable Time | 1.0 | | 8.0 | nS | |
| $t_{DIS}$ | Output Disable Time | 1.0 | | 8.0 | nS | |
| $t_{PR}$ | Rising Edge Propagation Delay | 1.0 | | 5.0 | nS | |
| $t_{PF}$ | Falling Edge Propagation Delay | 1.0 | | 5.0 | nS | |
| $t_D$ | Duty Cycle | 45 | | 55 | % | Measured at 1.5V |
| $Z_O$ | AC Output Impedance | | 15 | | Ω | |

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# Functional Description

## I/O Pin Operation

Pins 7, 17, 18, 25, 26, 46 are dual purpose l/O pins. Upon power up these pins act as logic inputs, allowing the determination of assigned device functions. A short time after power up, the logic state of each pin is latched and the pins become clock outputs. This feature reduces device pin count by combining clock outputs with input select pins.

An external 10k ohm “strapping” resistor is connected between the l/O pin and ground or VDD. Connection to ground sets a latch to "0", connection to VDD sets a latch to "1". Figure 1 and Figure 2 show two suggested methods for strapping resistor connections.

Upon RC7102 power up, the first 2ms of operation is used for input logic selection. During this period, the six I/O pins(7, 17, 18, 25, 26, 46) are tristated, allowing the output strapping resistor on the l/O pins to pull the pin and their associated capacitive clock load to either a logic high or low state. At the end of the 2ms period, the established logic "0" or "1" condition of the l/O pin is latched. Next the output buffer is enabled which converts the l/O pins into operating clock outputs. The 2ms timer is started when VDD reaches 2.0V. The input bits can only be reset by turning VDD off and then back on again.

It should be noted that the strapping resistors have no significant effect on clock output signal integrity. The drive impedance of clock output is <40 ohms (nominal) which is minimally affected by the 10k ohm strap to ground or VDD. As with the series termination resistor, the output strapping resistor should be placed as close to the l/O pin as possible in order to keep the interconnecting trace short. The trace from the resistor to ground or VDD should be kept less than two inches in length to prevent system noise coupling during input logic sampling.

When the clock outputs are enabled following the 2ms input period, the specified output frequency is delivered on the pin, assuming that VDD has stabilized. If VDD has not yet reached full value, output frequency initially may be below target but will increase to target once VDD voltage has stabilized. In either case, a short output clock cycle may be produced from the CPU clock outputs when the outputs are enabled.

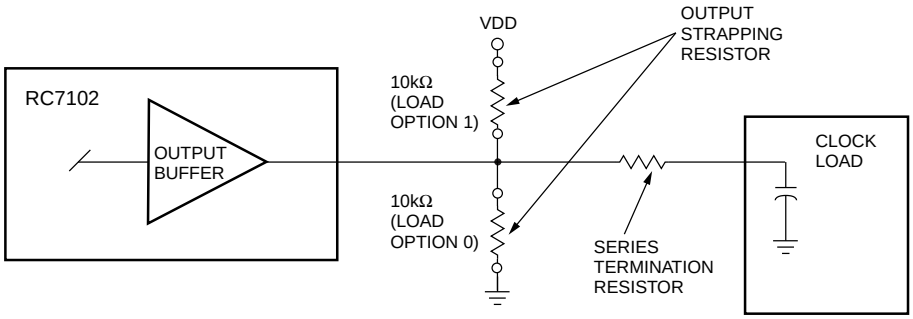


**Figure 1. Input Logic Selection through Resistor Load Option**

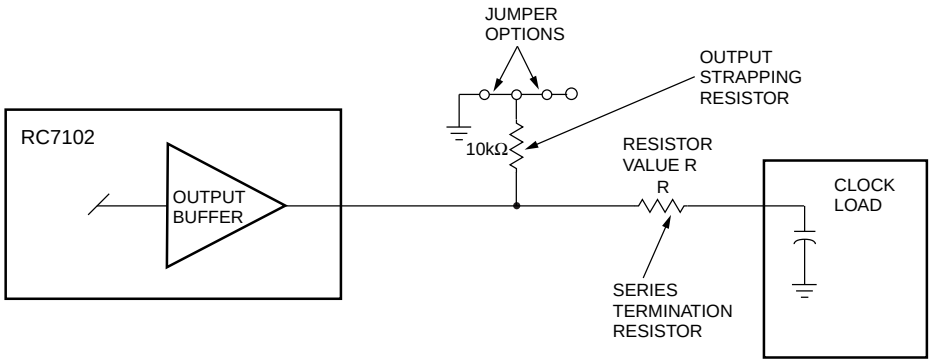


**Figure 2. Input Logic Selection through Jumper Option**

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## Serial Data Interface

The RC7102 features a two-pin, serial data interface that can be used to configure internal register settings that control particular device functions. Upon power-up, the RC7102 initializes with default register settings, therefore the use of this serial data interface is optional. The serial interface is write-only (to the clock chip) and is the dedicated function of device pins SDATA and SCLOCK. In motherboard applications, SDATA and SCLOCK are typically driven by two logic outputs of the chipset. Clock device register changes are normally made upon system initialization, if any are required. The interface can also be used during system operation for power management functions. Table 3 summarizes the control functions of the serial data interface.

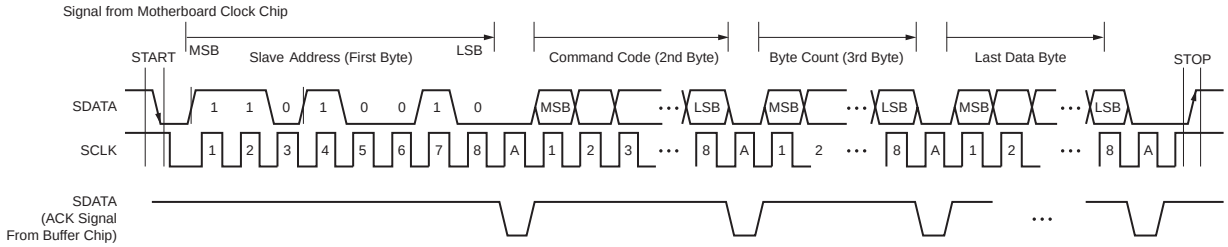
**Table 3. Serial Data Interface Control Functions Summary**

| Control Function | Description | Common Applications |
|---|---|---|
| Clock Output Disable | Any individual clock output(s) can be disabled. Disabled outputs are actively held low. | Unused outputs are disabled to reduce EMI and system power. Examples are clock outputs to unused PCI slots. |
| CPU Clock Frequency Selection | Provides CPU/PCI frequency selections through software. Frequency is changed in a smooth and controlled fashion. | For alternate microprocessors and power management options. Smooth frequency transition allows CPU frequency change under normal system operation. |
| Spread Spectrum Enabling | Enables or disables spread spectrum clocking. | For EMI reduction. |
| Output Tristate | Puts clock output into a high impedance state. | Production PCB testing. |
| (Reserved) | Reserved function for future device revision or production device testing. | No user application. Register bit must be written as 0. |
| Test Mode | All clock outputs toggle in relation to X1 input, internal PLL is bypassed. Refer to Table 7. | Production PCB Testing |

### Signaling Requirements for the I²C Serial Port

To initiate communications with the serial port, a start bit is invoked. The start bit is defined as the SDATA line is brought low while the SCLOCK is held high. Once the start bit is initiated, valid data can then be sent. Data is considered to be valid when the clock goes to and remains in the high state. The data can change when the clock goes low. To terminate the transmission, a stop bit is invoked. The stop bit occurs when the SDATA line goes from a low to a high state while the SCLOCK is held high. See Figure below.

## RC7104 I²C Interface Write Sequence Example




Note: Once the clock detects the start condition and its ADDRESS is matched, the clock chip will pull down the SDATA at every 8th bit. The 8 bit data from SDATA is latched into the Buffer Chip when the ACK is generated. This ACK signal will continue as long as STOP condition is detected The COMMAND CODE and BYTE COUNT is not used by the Buffer Chip.

## Operation

Data is written to the RC7102 in eleven bytes of eight bits each. Bytes are written in the order shown in Table 4.

**Table 4. Byte Writing Sequence**

| Byte Sequence | Byte Name | Bit Sequence | Byte Description |
|---|---|---|---|
| 1 | Slave Address | 11010010 | Commands the RC7102 to accept the bits in Data Bytes 0-6 for internal register configuration. Since other devices may exist on the same common serial data bus, it is necessary to have a specific slave address for each potential receiver. The slave receiver address for the RC7102 is 11010010. Register setting will not be made if the Slave Address is not correct (or is for an alternate slave receiver). |
| 2 | Command Code | Don't Care | Unused by the RC7102, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Command Code Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 3 | Byte Count | Don't Care | Unused by the RC7102, therefore bit values are ignored (don't care). This byte must be included in the data write sequence to maintain proper byte allocation. The Byte Count Byte is part of the standard serial communication protocol and may be used when writing to another addressed slave receiver on the serial data bus. |
| 4 | Data Byte 0 | Refer to Table 6 | The data bits in Data Bytes 0-7 set internal RC7102 registers that control device operation. The data bits are only accepted when the Address Byte bit sequence is 11010010, as noted above. For description of bit control functions, refer to Table 5, Data Byte Serial Configuration Map. |
| 5 | Data Byte 1 | | |
| 6 | Data Byte 2 | | |
| 7 | Data Byte 3 | | |
| 8 | Data Byte 4 | | |
| 9 | Data Byte 5 | | |

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## Writing Data Bytes

Each bit in Data Bytes 0-5 control a particular device function except for the "reserved" bits which must be written as a logic 0. Bits are written MSB (most significant bit) first, which is bit 7. Table 5 gives the bit formats for registers located in Data Bytes 0-5.

Table 6 details additional frequency selections that are available through the serial data interface.

Table 7 details the select functions for Byte 0, bits 1 and 0.

**Table 5. Data Bytes 0-5 Serial Configuration Map**

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|---|---|---|---|---|---|---|
| | Pin No. | Pin Name | | 0 | 1 | |
| **Data Byte 0** | | | | | | |
| 7 | — | CPU and PCI | Spread Amount - Must equal 1 for Down Spread | ± 0.25 | ± 0.5 | 0 |
| 6 | — | — | SEL_2 | See Table 6 | | 0 |
| 5 | — | — | SEL_1 | See Table 6 | | 0 |
| 4 | — | — | SEL_0 | See Table 6 | | 0 |
| 3 | — | — | Hardware/Software Frequency Select | Hardware | Software | 0 |
| 2 | — | CPU and PCI | Spread Type | Center | Down | 0 |
| 1 | 7, 8, 10, 11, 12, 13, 43, 44 | CPU and PCI | Spread Spectrum Clock | Normal | Spread | 0 |
| 0 | All Clocks | All Clocks | Clock Output Tristate | Active | Tristate | 0 |
| **Data Byte 1** | | | | | | |
| 7 | — | — | (Reserved) | — | — | 1 |
| 6 | — | — | (Reserved) | — | — | 1 |
| 5 | — | — | (Reserved) | — | — | 1 |
| 4 | — | — | Test Mode | see Table 7 | | 1 |
| 3 | 40 | SDRAM12 | Clock Output Disable | Low | Active | 1 |
| 2 | 41 | SDRAM13 | Clock Output Disable | Low | Active | 1 |
| 1 | 43 | CPU1 | Clock Output Disable | Low | Active | 1 |
| 0 | 44 | CPU0 | Clock Output Disable | Low | Active | 1 |
| **Data Byte 2** | | | | | | |
| 7 | — | — | (Reserved) | — | — | 1 |
| 6 | 7 | PCI_F | Clock Output Disable | Low | Active | 1 |
| 5 | — | — | (Reserved) | — | — | 1 |
| 4 | 13 | PCI5 | Clock Output Disable | Low | Active | 1 |
| 3 | 12 | PCI4 | Clock Output Disable | Low | Active | 1 |
| 2 | 11 | PCI3 | Clock Output Disable | Low | Active | 1 |
| 1 | 10 | PCI2 | Clock Output Disable | Low | Active | 1 |
| 0 | 8 | PCI1 | Clock Output Disable | Low | Active | 1 |

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**Table 5. Data Bytes 0-5 Serial Configuration Map** (continued)

| Bit(s) | Affected Pin | | Control Function | Bit Control | | Default |
|---|---|---|---|---|---|---|
| | Pin No. | Pin Name | | 0 | 1 | |
| **Data Byte 3** | | | | | | |
| 7 | — | — | (Reserved) | — | — | 1 |
| 6 | — | — | (Reserved) | — | — | 1 |
| 5 | 26 | 48Mhz | Clock Output Disable | Low | Active | 1 |
| 4 | 25 | 24MHz | Clock Output Disable | Low | Active | 1 |
| 3 | — | — | (Reserved) | — | — | 1 |
| 2 | 21, 20, 18, 17 | SDRAM8:11 | Clock Output Disable (SDRAM 10, 11 only when MODE=1) | Low | Active | 1 |
| 1 | 32, 31, 29, 28 | SDRAM4:7 | Clock Output Disable | Low | Active | 1 |
| 0 | 38, 37, 35, 34 | SDRAM0:3 | Clock Output Disable | Low | Active | 1 |
| **Data Byte 4** | | | | | | |
| 7 | — | — | (Reserved) | — | — | 1 |
| 6 | — | — | (Reserved) | — | — | 1 |
| 5 | — | — | (Reserved) | — | — | 1 |
| 4 | — | — | (Reserved) | — | — | 1 |
| 3 | — | — | (Reserved) | — | — | 1 |
| 2 | — | — | (Reserved) | — | — | 1 |
| 1 | — | — | (Reserved) | — | — | 1 |
| 0 | — | — | (Reserved) | — | — | 1 |
| **Data Byte 5** | | | | | | |
| 7 | — | — | (Reserved) | — | — | 1 |
| 6 | — | — | (Reserved) | — | — | 1 |
| 5 | — | — | (Reserved) | — | — | 1 |
| 4 | 47 | IOAPIC | Clock Output Disable | Low | Active | 1 |
| 3 | — | — | (Reserved) | — | — | 1 |
| 2 | — | — | (Reserved) | — | — | 1 |
| 1 | 46 | REF1 | Clock Output Disable | Low | Active | 1 |
| 0 | 2 | REF0 | Clock Output Disable | Low | Active | 1 |

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**Table 6. Additional Frequency Selections through Serial Data Interface Data Bytes**

| Input Conditions | | | Output Frequency | |
|---|---|---|---|---|
| Data Byte 0, Bit 3 = 1 | | | | |
| Bit 6 SEL_2 | Bit 5 SEL_1 | Bit 4 SEL_0 | CPU, SDRAM Clocks (MHz) | PCI Clocks (MHz) |
| 1 | 1 | 1 | 100. 2 | 33.4 |
| 1 | 1 | 0 | 133.3 | 44.4 |
| 1 | 0 | 1 | 112 | 37.3 |
| 1 | 0 | 0 | 103 | 34.3 |
| 0 | 1 | 1 | 66.8 | 33.4 |
| 0 | 1 | 0 | 83.3 | 41.65 |
| 0 | 0 | 1 | 75 | 37.5 |
| 0 | 0 | 0 | 124 | 41.3 |

**Table 7. Test Mode**

| | Input Conditions | Output Frequency | | | | |
|---|---|---|---|---|---|---|
| | Data Byte 1 | | | | | |
| Function | Bit 4 | CPU0:1 | PCI_F, PCI1:5 | REF, IOAPIC | 48MHz | 24MHz |
| Normal Operation | 1 | Note 1 | Note 1 | 14.318 MHz | 48 MHz | 24 MHz |
| Test Mode | 0 | X1/2 | CPU/2 or 3 | X1 | X1/2 | X1/4 |

**Note 1**: CPU and PCI frequency selections are listed in Table 2 and Table 6.

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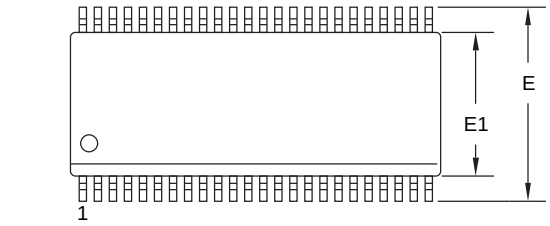
# Mechanical Dimensions

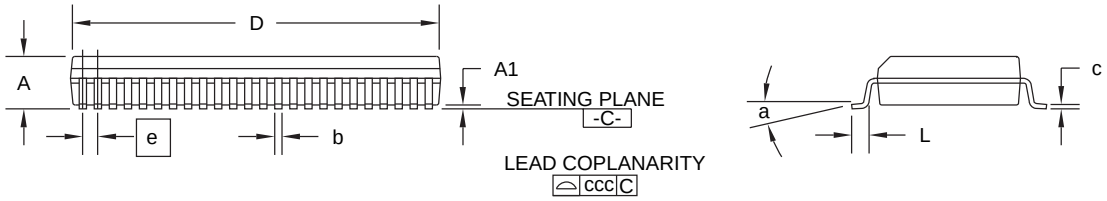
## 48 pin SSOP

| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | .095 | .110 | 2.41 | 2.79 | |
| A1 | .008 | .016 | 0.20 | 0.41 | |
| b | .008 | .0135 | 0.20 | 0.34 | 5 |
| c | .005 | .010 | 0.13 | 0.25 | 5 |
| D | .620 | .630 | 15.75 | 16.00 | 2, 4 |
| E | .395 | .420 | 10.03 | 10.67 | |
| E1 | .291 | .299 | 7.39 | 7.59 | 2 |
| e | .025 BSC | | 0.64 BSC | | |
| L | .020 | .040 | 0.51 | 1.02 | 3 |
| N | 48 | | 48 | | 6 |
| a | 0° | 8° | 0° | 8° | |
| ccc | --- | .004 | --- | 0.13 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
2. "D" and "E1" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "b" & "c" dimensions include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.

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## Ordering Information

| Product Number | Temperature | Screening | Package | Package Marking |
|---|---|---|---|---|
| RC7102 | | | 48 SSOP | RC7102 |

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