RF3320

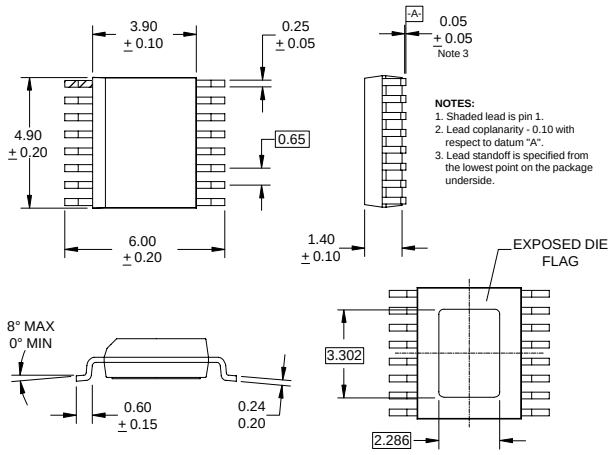
CABLE REVERSE PATH
PROGRAMMABLE GAIN AMPLIFIER

Typical Applications

- Euro-DOCSIS/DOCSIS Cable Modems
- CATV Set-Top Boxes
- Telephony Over Cable
- Home Networks
- Automotive/Mobile Multimedia
- Coaxial and Twisted Pair Line Driver

Product Description

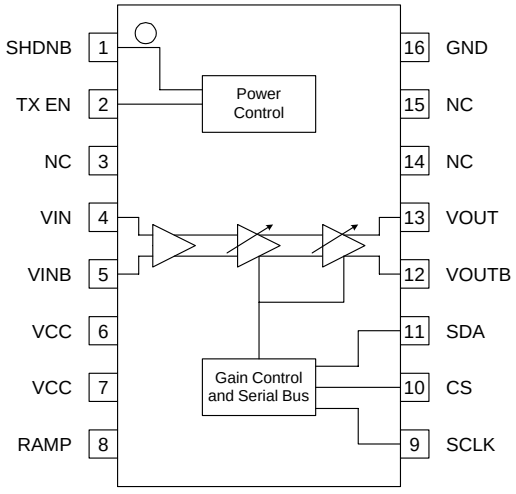
The RF3320 is a variable gain amplifier for use in CATV reverse path (upstream) applications. It is DOCSIS-compliant for use in cable modems. The gain control covers a 58dB range and is serially programmable via three-wire digital bus for compatibility with standard baseband chipsets. Amplifier shutdown and transmit disable modes are software- and hardware-controlled. The device is placed into software-shutdown mode via the serial control bus. The device operates over the frequency band of 5MHz to 65MHz for use in current U.S. and European systems. The amplifier delivers up to 60dBmV at the output of the balun. Gain is controllable in accurate 1dB steps. The device is provided in a thermally enhanced, exposed die flag package.



Package Style: SSOP-16 EDF Slug

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 5V Supply
- Differential Input and Output
- -30dB to +28dB Voltage Gain Range
- 5MHz to 65MHz Operation
- Sophisticated Power Management
- DOCSIS 1.1 RF Compliant

Ordering Information

RF3320	Cable Reverse Path Programmable Gain Amplifier
RF3320 PCBA	Fully Assembled Evaluation Board

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Input RF Level	12	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Humidity	80	%
Maximum Power Dissipation	0.5	W
Maximum T_J	150	°C

Caution! ESD sensitive device.

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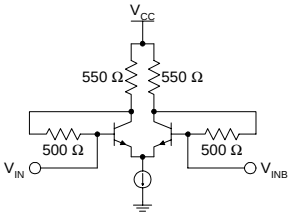
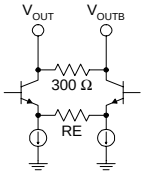
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC}=4.75V to 5.25V, TXEN=SHDNB=1, V_{IN}=30dBmV (rms) differential, output impedance=75Ω through a 2:1 transformer. Typical performance is at T_A=+25°C, V_{CC}=5V.
DC Specifications					
Supply Voltage	4.75	5.0	5.25	V	
Supply Current					
Maximum Gain		130	160	mA	Gain Control Word=58
Low Gain		65	105	mA	Gain Control Word<35
Transmit Disable		25	35	mA	TXEN=0
Software-Shutdown		3	5	mA	Bit 7 of gain control word FALSE
Sleep		0.05		mA	SHDNB=0
Logic High Voltage	2			V	
Logic Low Voltage			0.8	V	
Logic Leakage Current	-1		1	µA	
AC Specifications					
Voltage Gain					
Maximum	27	28		dB	5MHz to 42MHz; Gain Control Word=58
	26			dB	42MHz to 65MHz; Gain Control Word=58
Minimum		-30	-29	dB	5MHz to 42MHz; Gain Control Word=0
			-28	dB	42MHz to 65MHz; Gain Control Word=0
3dB Bandwidth		100		MHz	Intended operating range is 5MHz to 65MHz.
1dB Compression Point		66		dBmV	
Maximum Input Level			34	dBmV(rms)	Modulated. To meet distortion specifications.
Maximum Output Level			60	dBmV(rms)	Modulated. Into 75Ω load at balun output, all distortion tones <-50dBc.
ACPR		-59	-47	dBc	V_{IN}=34dBmV (rms); QPSK modulation; Symbol rate=160ksps (2 bits per symbol); 20-bit PRBS (pseudo-random bit stream); 0.25 alpha root cosine filter
Output IM3		-58	-55	dBc	Tones at 40MHz and 40.2MHz, V_{OUT}=+54dBmV/tone, maximum gain, OIP3 is therefore +84dBmV, IIP3 is 58dBmV.
Output Third Harmonic Distortion					
F=20MHz, V_{OUT}=59dBmV		-60	-55	dBc	Maximum Gain, CW
F=65MHz, V_{OUT}=59dBmV		-55	-50	dBc	Maximum Gain, CW
Output Second Harmonic Distortion					
F=20MHz, V_{OUT}=59dBmV		-70	-60	dBc	Maximum Gain
F=65MHz, V_{OUT}=59dBmV		-70	-60	dBc	Maximum Gain

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
AC Specifications, cont'd					
Output Step Size	0.8	1.0	1.1	dB	
Isolation in Transmit Disable Mode	-80	-95		dBc	Maximum Gain, 20MHz
Output Noise					
Maximum Gain		-37	-30	dBmV/ 160kHz	-96dBc for a 59dBmV carrier in a 160kHz bandwidth.
Minimum Gain		-55	-50	dBmV/ 160kHz	-64dBc for an 8dBmV carrier in a 160kHz bandwidth.
Transmit Disabled		-75	-70	dBmV/ 160kHz	TXEN=0
TX EN Enable Time		0.5	1.0	µS	Time for gain to reach 99% of final value. See Note 1.
TX EN Transient Duration	2.4	3.0		µS	See Note 1.
Output Switching Transients		5	10	mV_{P-P}	Maximum Gain
		3	5	mV_{P-P}	Minimum Gain
Output Impedance	255	300	345	Ω	Chip output impedance is nominally 300Ω. Differential to single-ended output conversion to 75Ω is performed in a balun with a 2:1 turns ratio, corresponding to a 4:1 impedance ratio.
Input Impedance		75		Ω	Differential
Thermal					
$Theta_{JC}$		28		°C/W	

Note 1: The enable time is determined by the value of the capacitor on pin 8 (RAMP). A higher capacitor value will increase the enable time, but will reduce the transient voltage.

Pin	Function	Description	Interface Schematic
1	SHDNB	Chip shutdown pin. Forcing a logic low causes all circuits to switch off and gain settings to be lost.	
2	TX EN	Signal path enable pin. Logic high turns on signal path. Logic low turns off signal path, but leaves serial bus active.	
3	NC	Not connected. This pin should be grounded.	
4	VIN	Input pin. This should be externally AC-coupled to signal source.	See pin 5.
5	VINB	Complementary input pin. This should be externally coupled to signal source. For single-ended use, this pin should be AC-coupled to ground.	
6	VCC	This pin is connected to the supply voltage.	
7	VCC	Same as pin 6.	
8	RAMP	An external capacitor between this pin and ground controls turn-on time.	
9	SCLK	Serial bus clock input.	
10	CS	Serial bus enable.	
11	SDA	Serial bus data input.	
12	VOUTB	Open collector output. Connect to VCC via balun primary.	See pin 13.
13	VOUT	Open collector output. Connect to VCC via balun primary.	
14	NC	Same as pin 3.	
15	NC	Same as pin 3.	
16	GND	Connect to ground.	
PKG BASE	GND	Die is mounted on a heat sink slug that should be connected to ground. Device grounds are internally bonded to the slug.	

Serial Bus Block Diagram

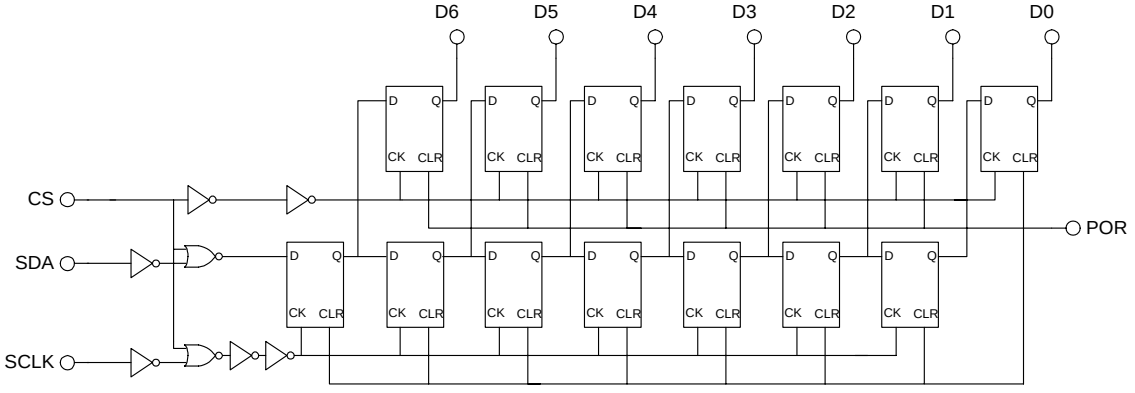


Table 1. Serial Interface Control Word Format

Bit	Mnemonic	Description
MSB 6	D6	Sleep Mode (Software Shutdown)
5	D5	Gain Control, Bit MSB
4	D4	Gain Control, Bit 4
3	D3	Gain Control, Bit 3
2	D2	Gain Control, Bit 2
1	D1	Gain Control, Bit 1
LSB 0	D0	Gain Control, Bit LSB

Serial Bus Timing Diagram

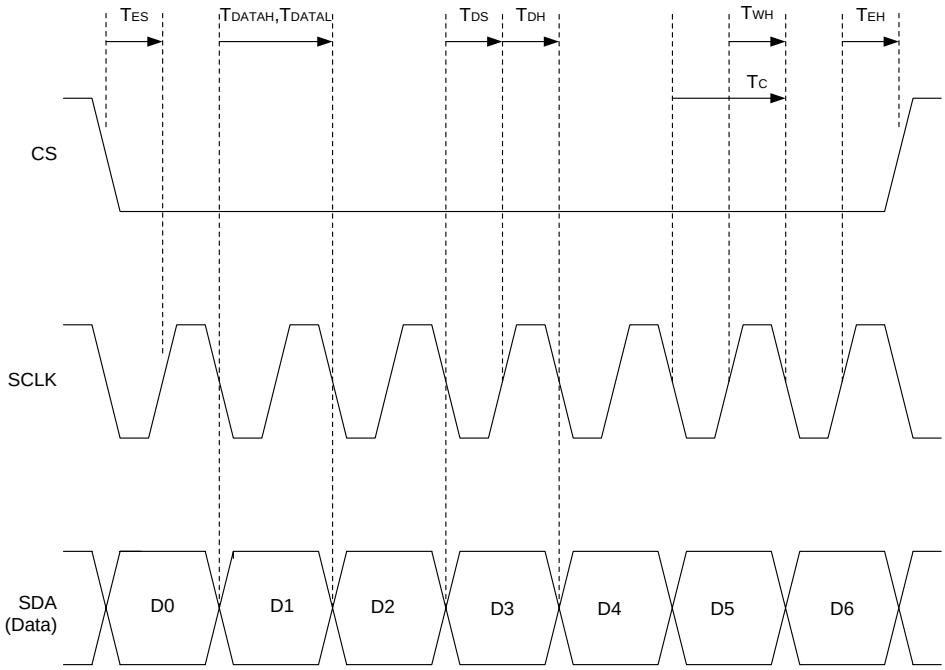


Table 2. Timing Data

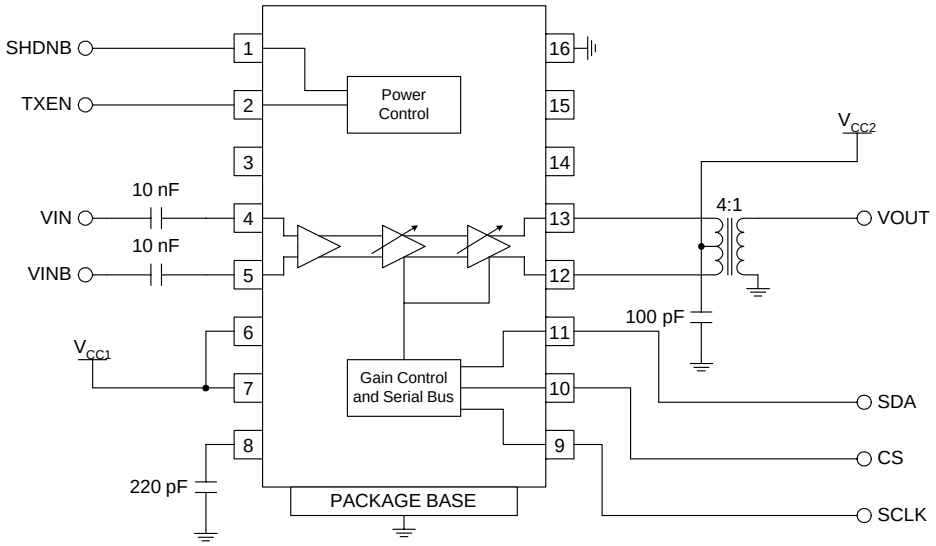
Parameter	Symbol	Min	Typ	Max	Units
SCLK Pulsewidth	T_{WH}	50			ns
SCLK Period	T_C	100			ns
Setup Time, SDA versus S CLK	T_{DS}	10			ns
Setup Time, CS versus S CLK	T_{ES}	10			ns
Hold Time, SDA versus S CLK	T_{DH}	20			ns
Hold Time, CS versus S CLK	T_{EH}	20			ns
SCLK Pulsewidth, High	T_{DATAH}	50			ns
SCLK Pulsewidth, Low	T_{DATAL}	50			ns

Table 3. Programming State

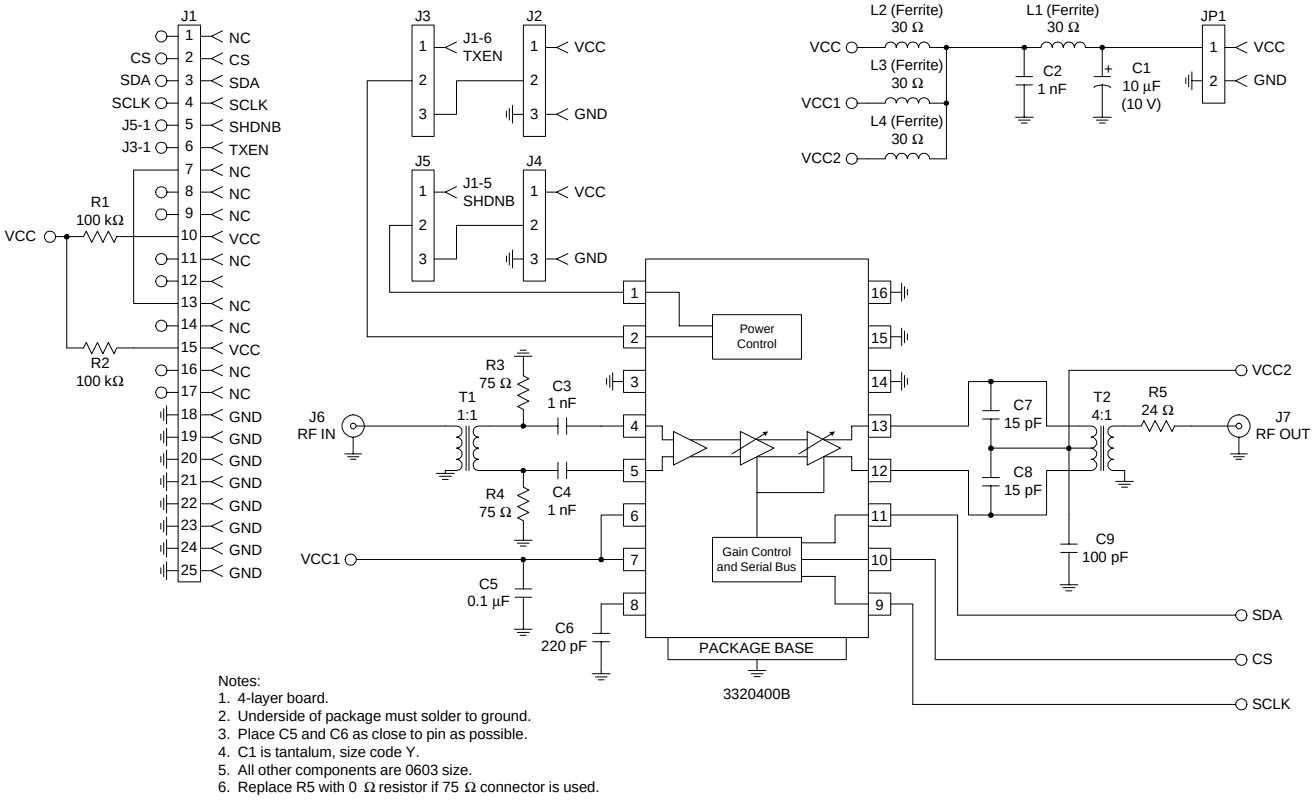
	TX	SHDND	MSB6
Enter Sleep Mode	X	H	L
Exit Sleep Mode	X	H	H*
Enter Shutdown	X	L	X
Exit Shutdown	X	H	H*
TX Enable	H	X	X
TX Disable	L	X	X

H=High Voltage Logic
L=Low Voltage Logic
X=Don't Care
*Gain Control Data Must be Re-Sent

Typical Application Schematic



Evaluation Board Schematic



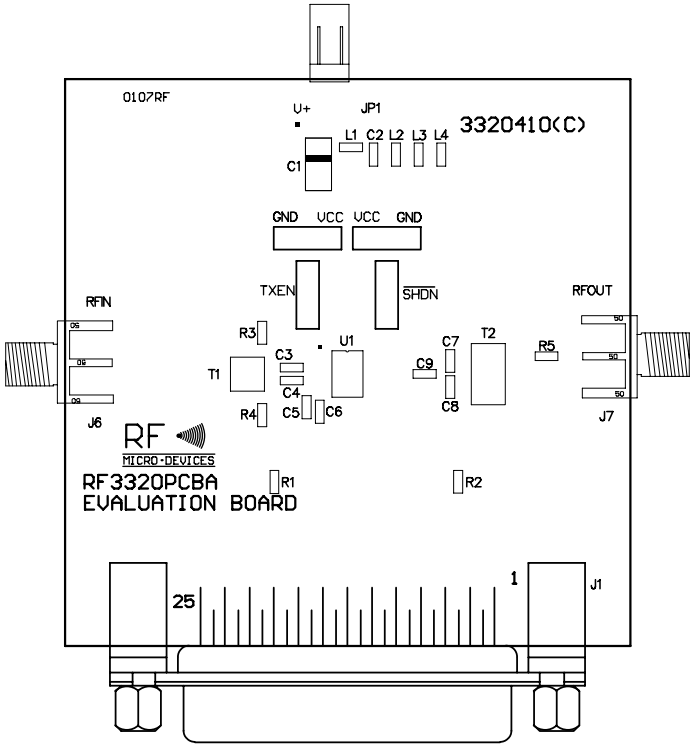
Notes:
1. 4-layer board.
2. Underside of package must solder to ground.
3. Place C5 and C6 as close to pin as possible.
4. C1 is tantalum, size code Y.
5. All other components are 0603 size.
6. Replace R5 with 0 Ω resistor if 75 Ω connector is used.

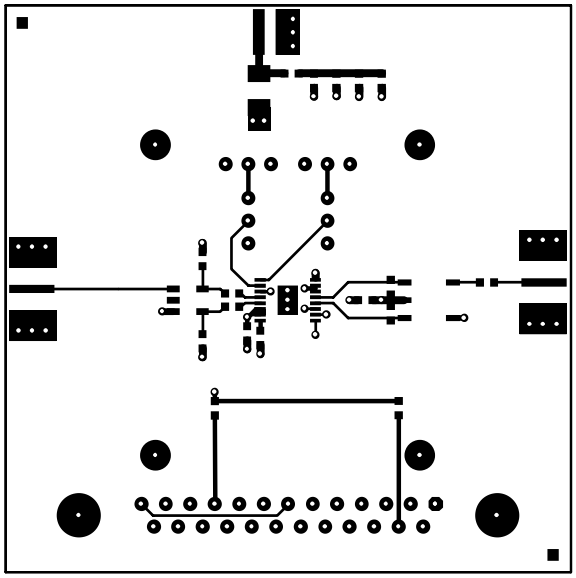
PCB Layout Considerations

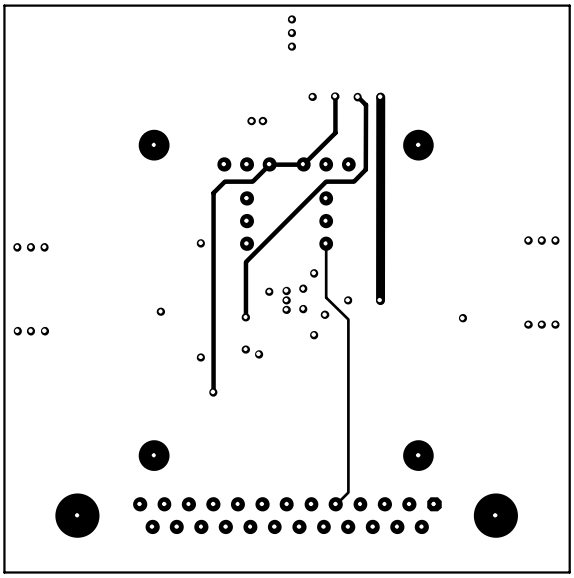
The RF3320 Evaluation board can be used as a guide for the layout in your application. Care should be taken in laying out the RF3320 in other applications. The RF3320 will have similar results if the following guidelines are taken into consideration:

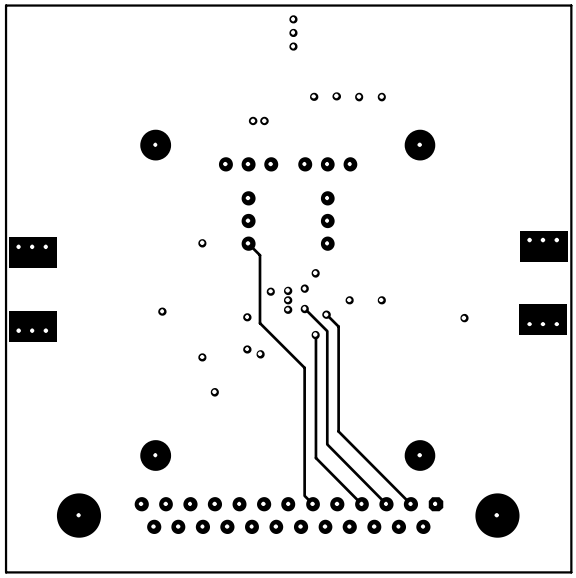
- Make sure underside of package is soldered to a good ground on the PCB.
- Keep input and output traces as short as possible.
- Ensure a good ground plane by using multiple vias to the ground plane.
- Use a low noise power supply along with decoupling capacitors.

Evaluation Board Layout
Board Size 2.5” x 2.5”
Board Thickness 0.058”, Board Material FR-4

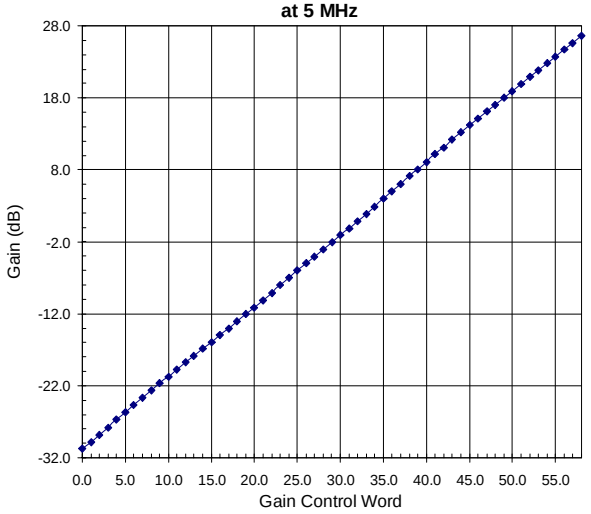




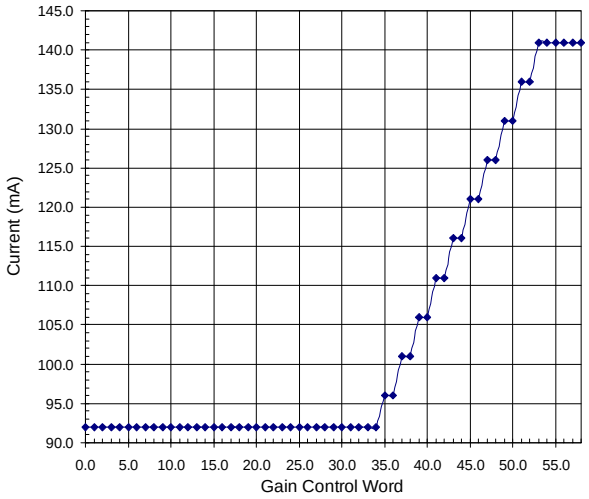




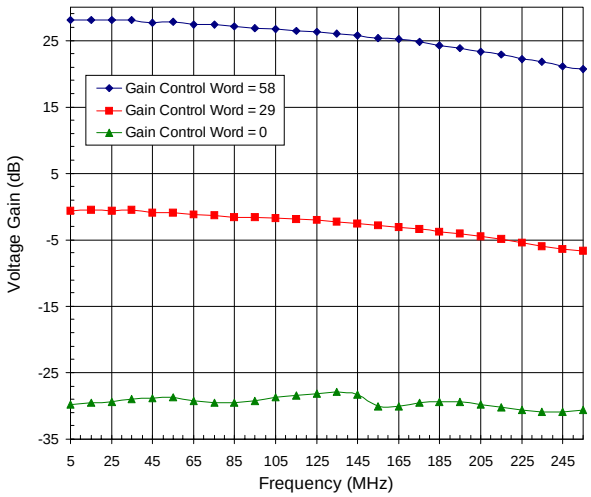
Gain versus Gain Control Word at 5 MHz



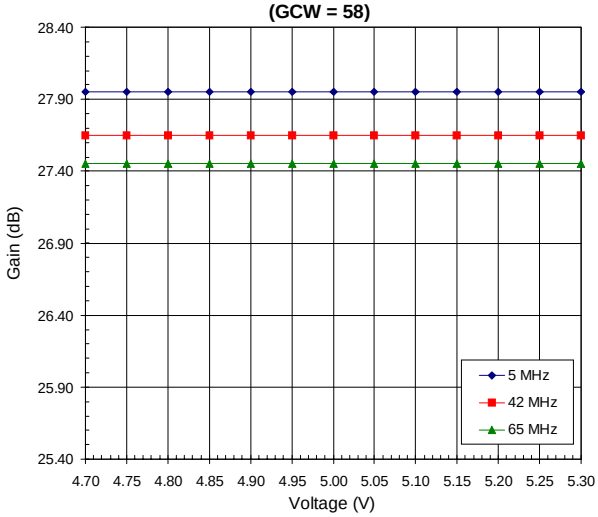
Current versus Gain Control Word



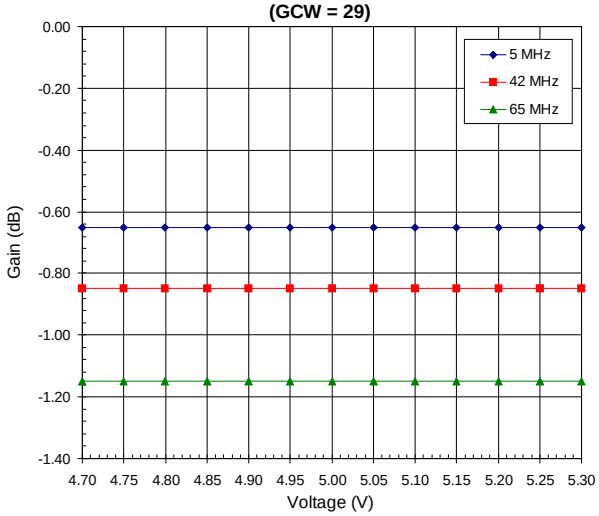
Gain versus Frequency



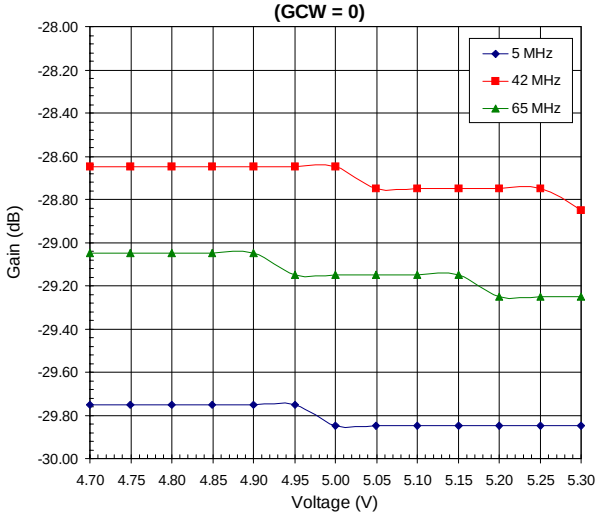
Gain versus Supply Voltage (GCW = 58)



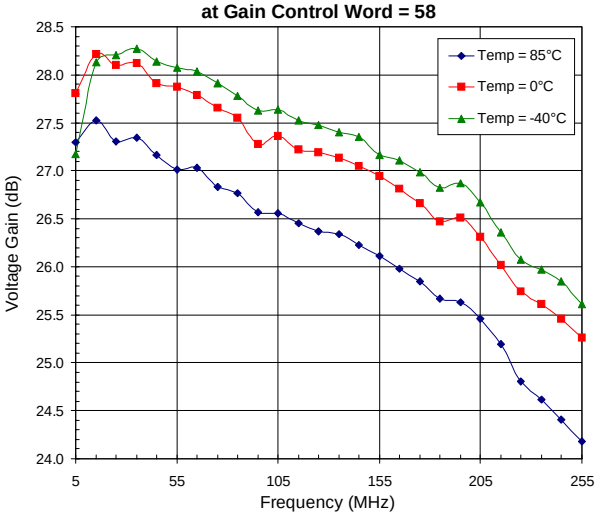
Gain versus Supply Voltage (GCW = 29)



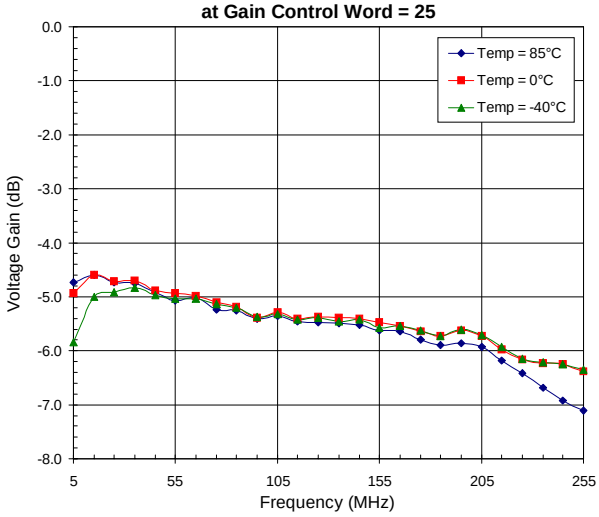
Gain versus Supply Voltage (GCW = 0)



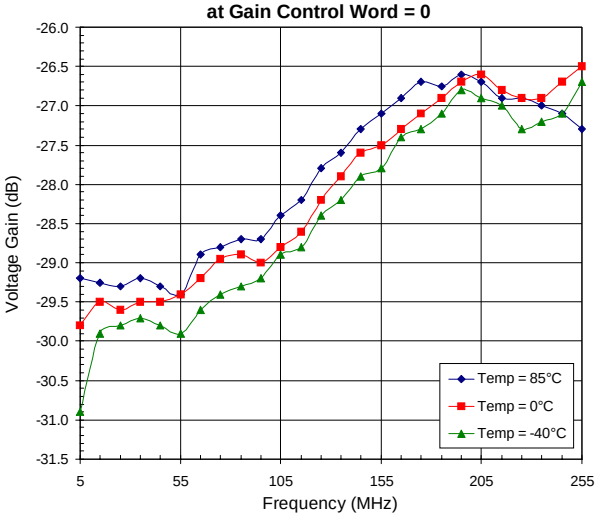
Gain versus Frequency at Gain Control Word = 58



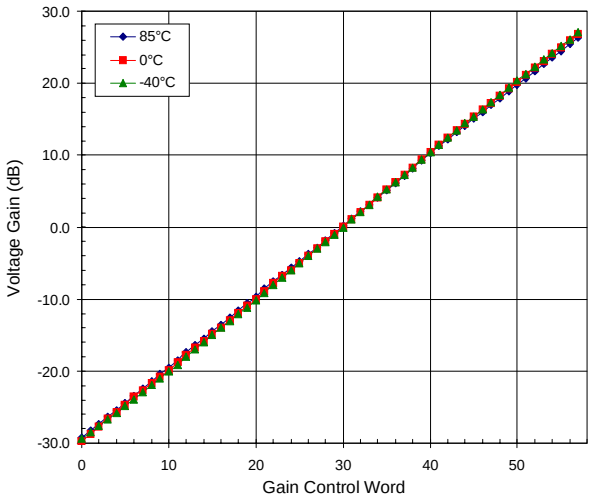
Gain versus Frequency at Gain Control Word = 25



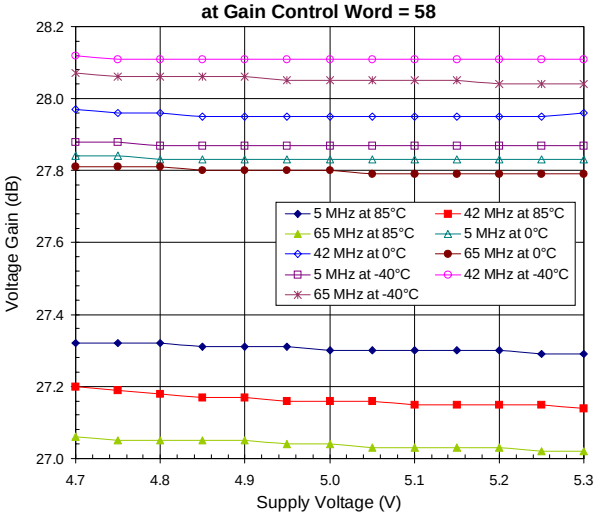
Gain versus Frequency at Gain Control Word = 0



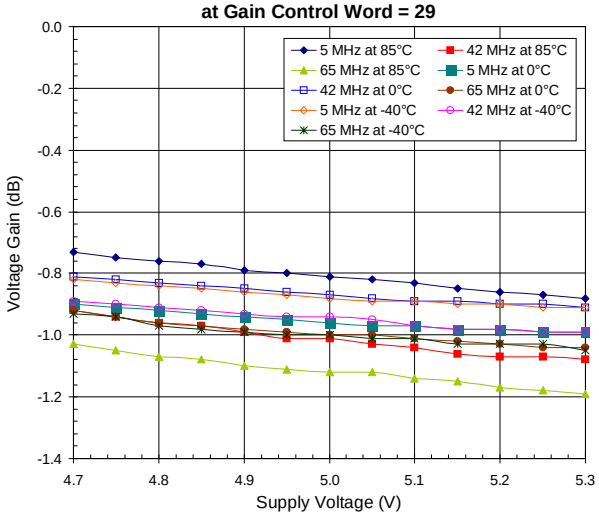
Gain versus Gain Control Word



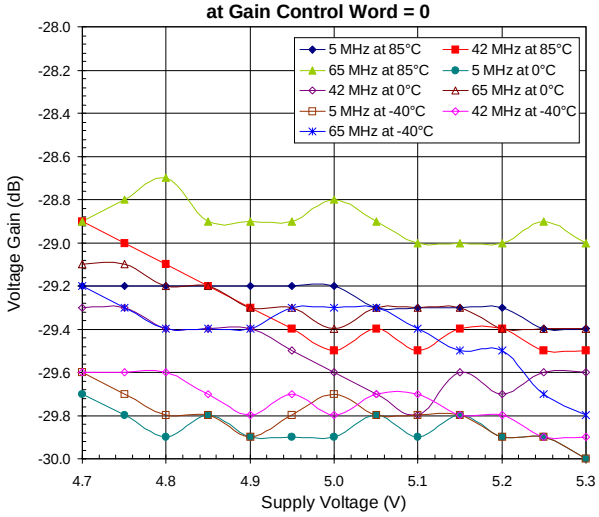
Gain versus Supply Voltage at Gain Control Word = 58



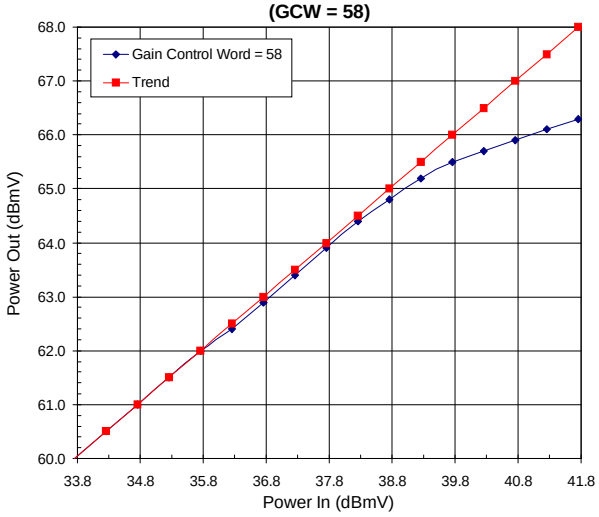
Gain versus Supply Voltage at Gain Control Word = 29



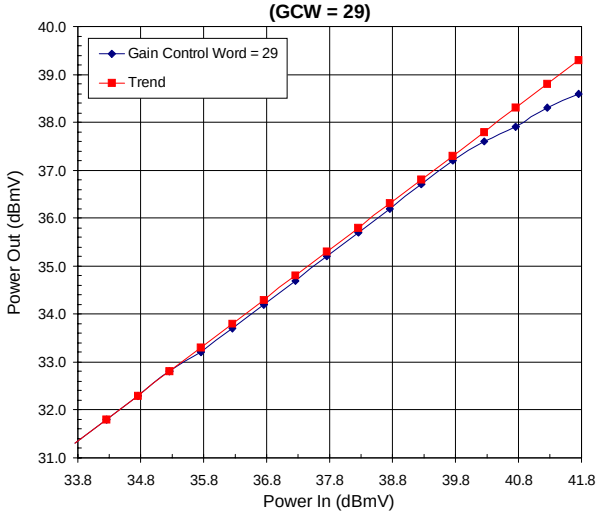
Gain versus Supply Voltage at Gain Control Word = 0



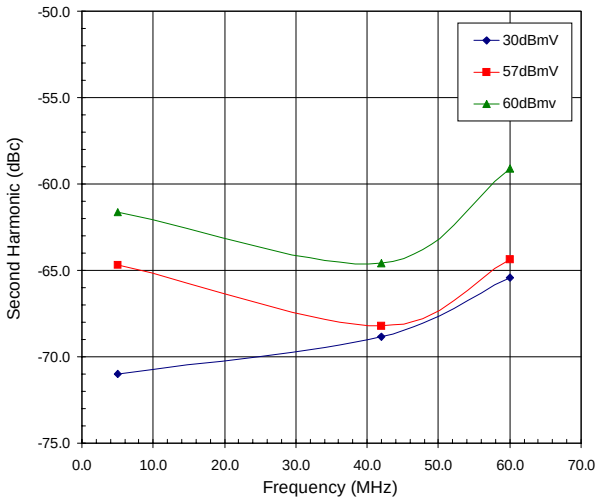
-1 dB Compression Point (GCW = 58)



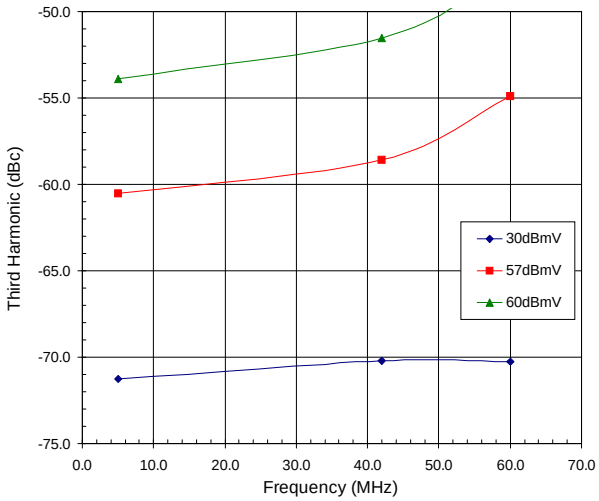
-1 dB Compression Point (GCW = 29)



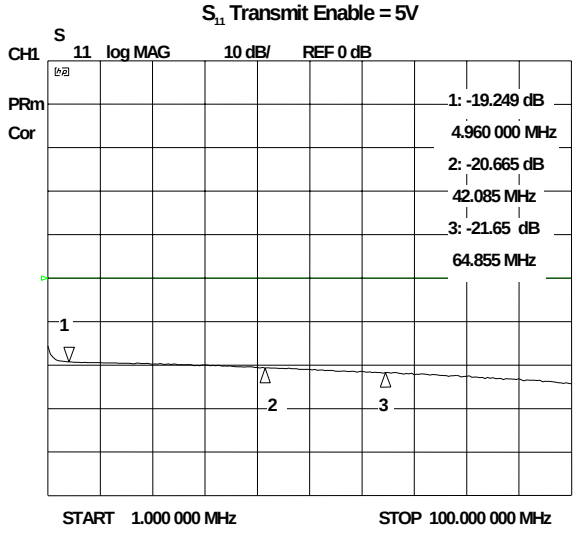
Second Harmonic versus Frequency and Output Level



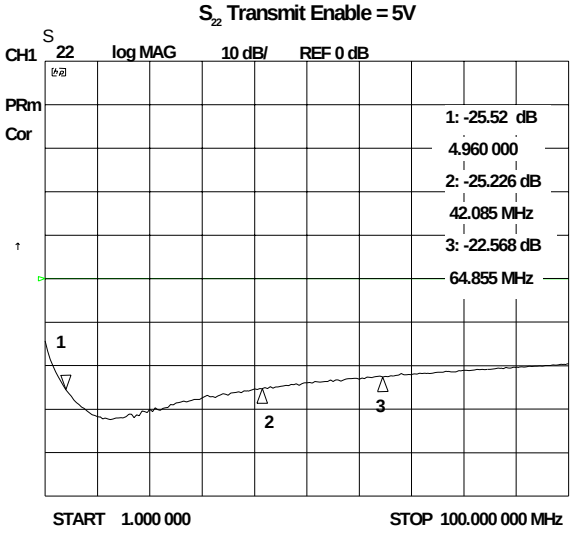
Third Harmonic versus Frequency and Output Level



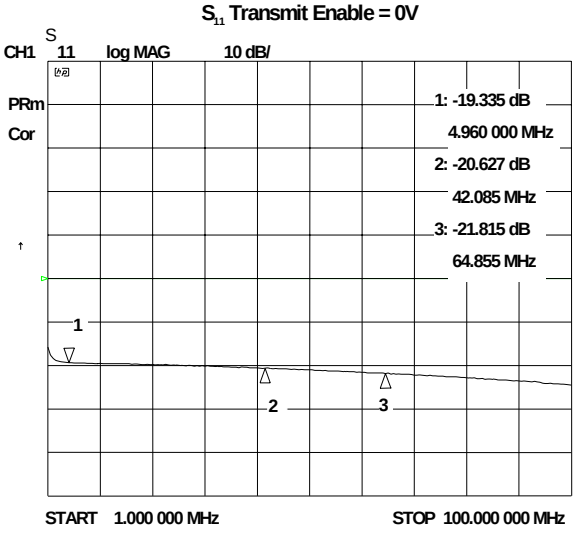
S_{11} Transmit Enable = 5V



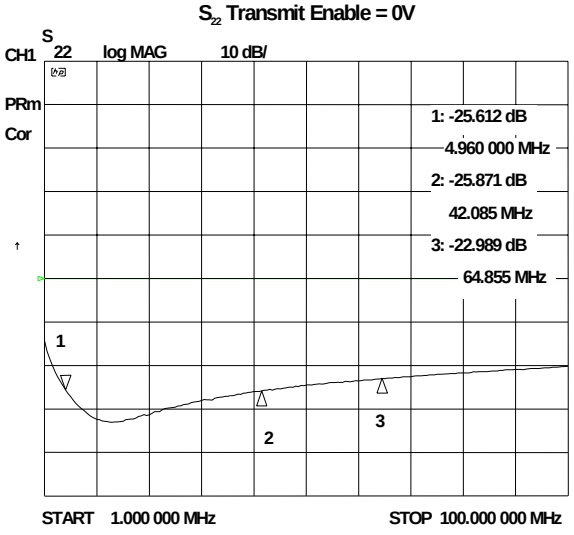
S_{22} Transmit Enable = 5V



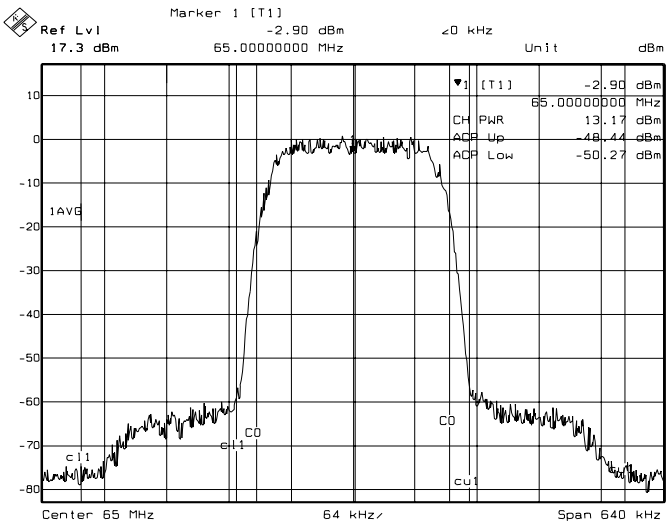
S_{11} Transmit Enable = 0V



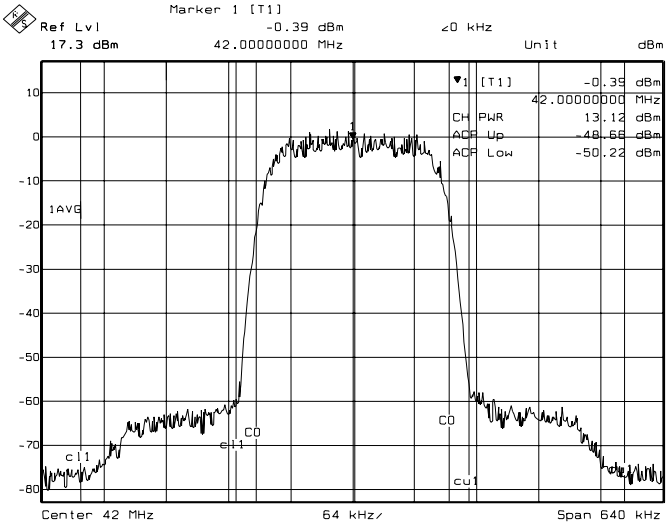
S_{22} Transmit Enable = 0V



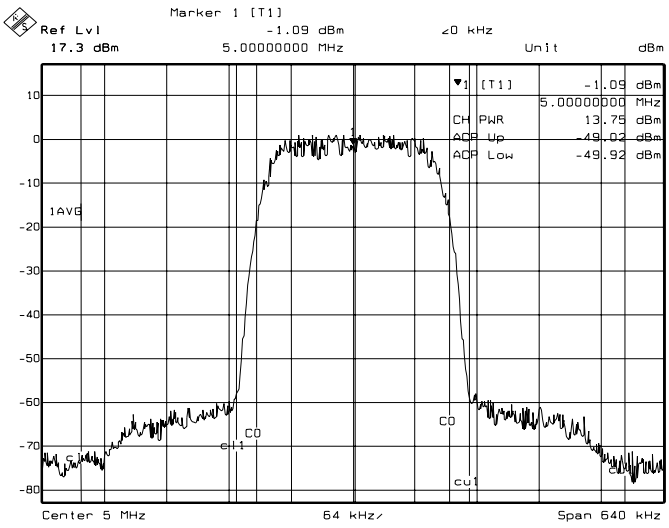
ACPR at 65MHz



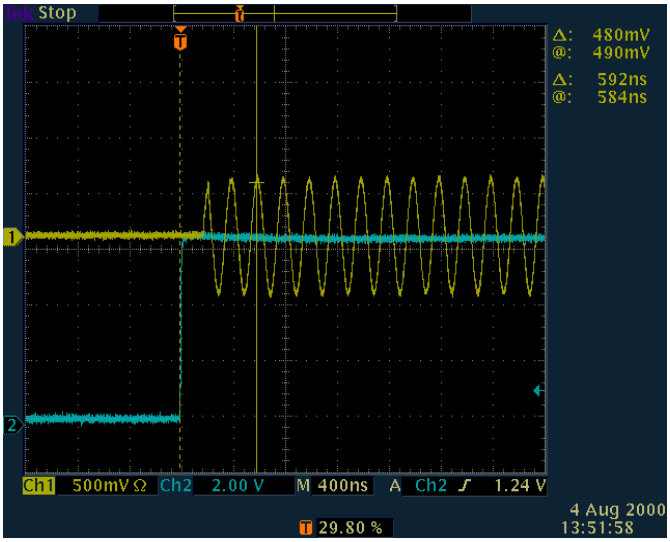
ACPR at 42MHz



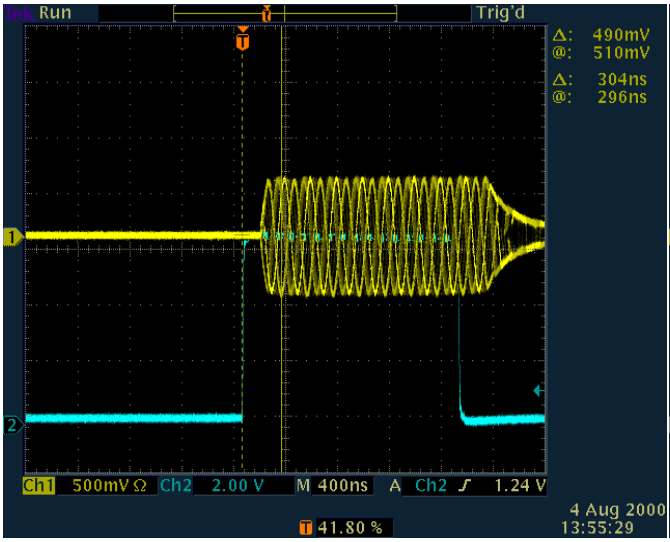
ACPR at 5MHz



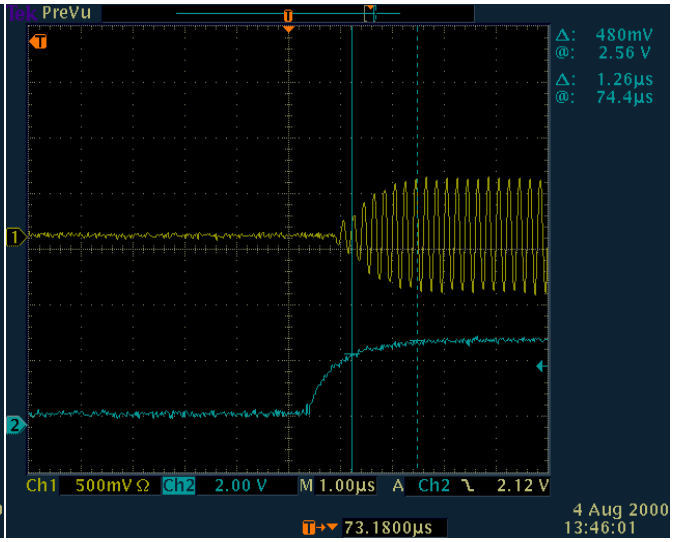
Power Up Settling Time Coming Out Of Shutdown Condition



Power Up Settling Time Coming Out Of Shutdown Condition (Entire Pulse)



Power Up Settling Time Coming Out Of Sleep Condition



Special Handling Information for Shrunk Small Outline Package (SSOP1-EPP) Products

These packages are considered JEDEC Level 5 for moisture sensitivity and require special handling to assure reliable performance.

The exposed copper slug on the bottom of the package improves both thermal and electrical performance. Since the RFIC is mounted directly on the thermal slug, and the slug is soldered directly on the PCB, the thermal resistance to the PCB is minimized. Also, the RF ground for the amplifier is established through this copper slug as it is soldered to the ground plane on the PCB. This offers the least inductance ground path available.

Care must be taken when soldering these packages to the PCB. They are currently considered JEDEC Level 5 for moisture sensitivity. Therefore the parts must be handled in a dry environment prior to soldering, as is specified in the JEDEC specification. Specifically, RFMD recommends the following procedure prior to assembly:

1. Dry-bake the parts at 125°C for 24 hours minimum. Note: the shipping tubes cannot withstand 125°C baking temperature.
2. Parts delivered on tape and reel are already dry-baked and dry-packed. These may be stored for up to one year, but must be assembled within 48 hours after opening the bag.
3. Assemble the dry-baked parts within two days of removal from the oven.
4. During this two-day period, the parts must be stored in humidity less than 60%.

IMPORTANT!

If the two-day period is exceeded, then this procedure must be repeated prior to assembly.