## Overview

The 16/18/64/72-Mbit Concurrent Rambus™ DRAMs (RDRAM®) are extremely high-speed CMOS DRAMs organized as 2M or 8M words by 8 or 9 bits. They are capable of bursting unlimited lengths of data at 1.67 ns per byte (13.3ns per eight bytes). The use of Rambus Signaling Logic (RSL) technology permits 600MHz transfer rates while using conventional system and board design methodologies. Low effective latency is attained by operating the two or four 1KByte or 2KByte sense amplifiers as high speed caches, and by using random access mode (page mode) to facilitate large block transfers. Concurrent (simultaneous) bank operations permit high effective bandwidth using interleaved transactions.

RDRAMs are general purpose high-performance memory devices suitable for use in a broad range of applications including PC and consumer main memory, graphics, video, and any other application where high-performance at low cost are required.

## Features

- ❒ Compatible with prior generation RDRAMs
- ❒ 600 MB/s peak transfer rate per RDRAM
- ❒ Rambus Signaling Level (RSL) interface
- ❒ Synchronous, concurrent protocol for block-oriented, interleaved (overlapped) transfers
- ❒ 480MB/s effective bandwidth for random 32 byte transfers from one RDRAM
- ❒ 13 active signals require just 32 total pins on the controller interface (including power)
- ❒ 3.3 volt operation
- ❒ Additional/multiple Rambus Channels each provide an additional 600 MB/s bandwidth
- ❒ Two or four 1KByte or 2KByte sense amplifiers may be operated as caches for low latency access
- ❒ Random access mode enables any burst order at full bandwidth within a page
- ❒ Graphics features include write-per-bit and mask-per-bit operations

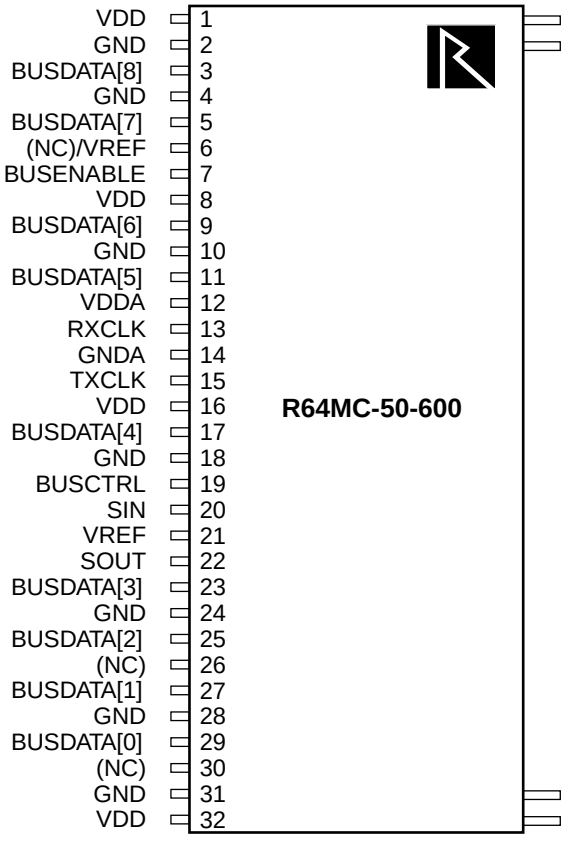
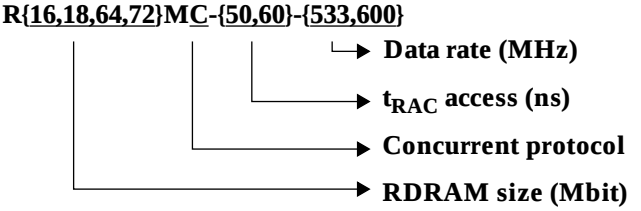



**Figure 1: Pin Assignment (SHP-32 top view)**

## Part Numbers

The 16/18- and 64/72-Mbit RDRAM is available in both horizontal surface mount (SHP) and vertical surface mount (SVP) packages, and with 533 and 600 MHz clock rate. The part numbers for the various options are assigned in the following manner:




**Example: R64MC-50-600:** This designates a 64Mbit RDRAM using Concurrent protocol, which has a 50ns $t_{RAC}$ access time, and which operates at data transfer rates of up to 600MHz.

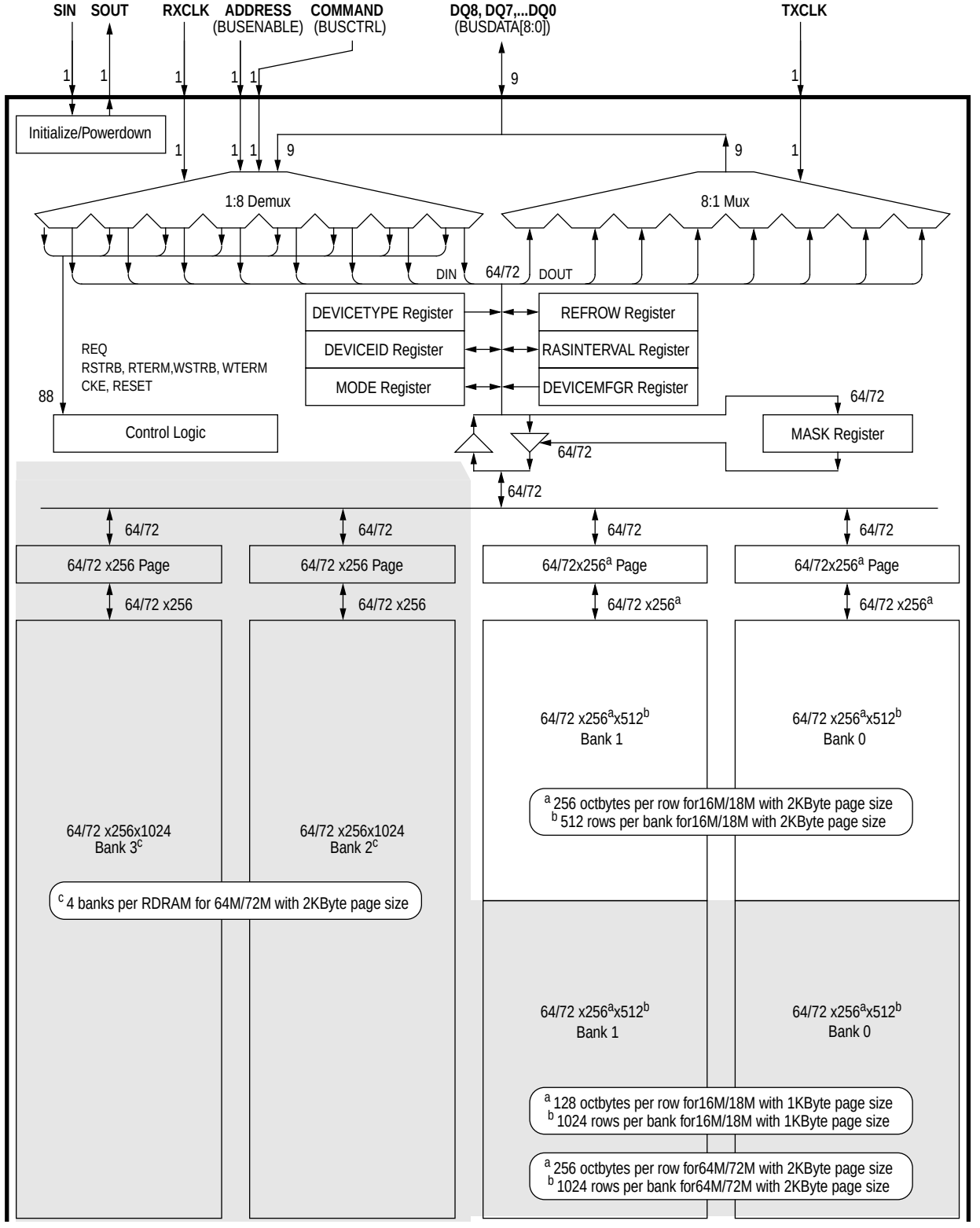



**Figure 2: 16/18/64/74Mbit Concurrent RDRAM Block Diagram**

## General Description

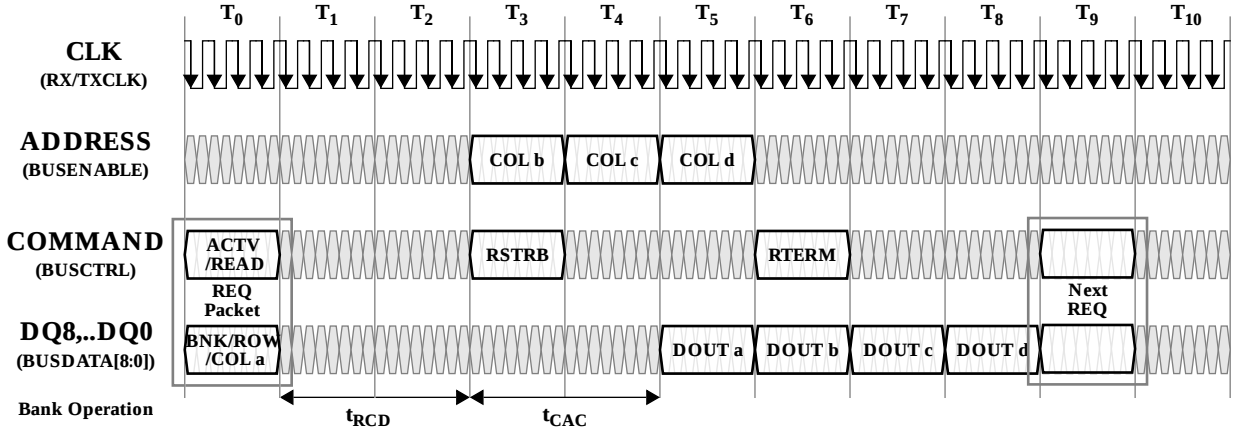
Figure 2 is a block diagram of an RDRAM. At the bottom is a standard DRAM core organized as two or four independent banks, with each bank organized as 512 or 1024 rows, and with each row consisting of 1KByte or 2KBytes of memory cells. One row of a bank may be "activated" at any time (ACTV command) and placed in the 1KByte or 2KByte "page" for the bank. Column accesses (READ and WRITE commands) may be made to this active page.

The smallest block of memory that may be accessed with READ and WRITE commands is an octbyte (eight bytes). Bitmask and bytemask options are available with the WRITE command to allow finer write granularity. There are six control registers that are accessed at initialization time to configure the RDRAM for a particular application.

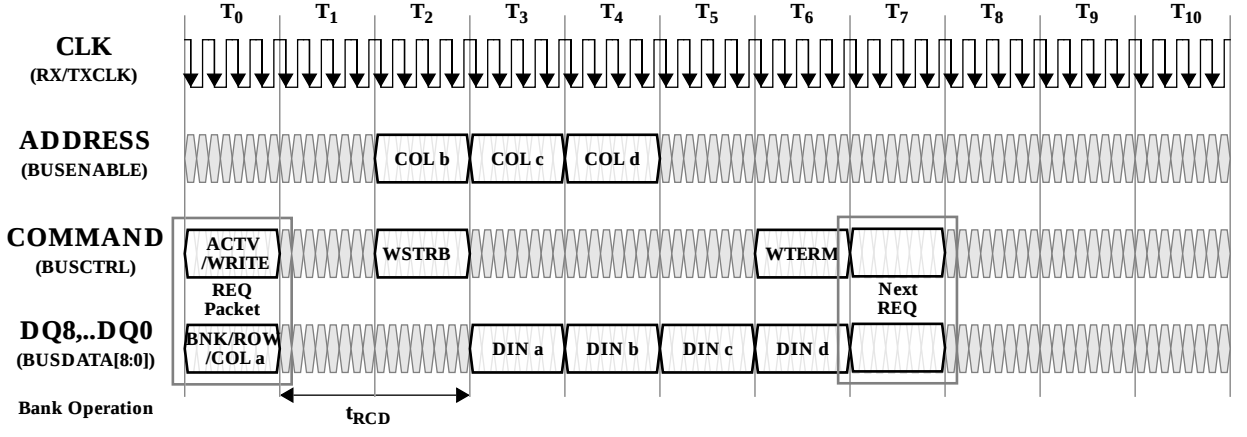
## Basic Operation

Figure 3a shows an example of a read transaction. A transaction begins in interval $T_0$ with the transfer of a REQ packet. The REQ packet contains the command (ACTV / READ), a device, bank, and row address (BNK / ROW) of the page to be activated, and the column address (COLa) of the first octbyte to be read from the page.

The selected bank performs the activation of the selected row during $T_1$ and $T_2$ (the $t_{RCD}$ interval). Next, the selected bank reads the selected octbyte during $T_3$ and $T_4$ (the $t_{CAC}$ interval). A second command RSTRB (read strobe) is transferred during $T_3$ and causes the first octbyte (DOUTa) to be transferred during $T_5$.




**(a) BANK ACTIVATE AND RANDOM READ CYCLES WITHIN A PAGE**




**(b) BANK ACTIVATE AND RANDOM WRITE CYCLES WITHIN A PAGE**

**Figure 3: Read and Write Transaction Examples**

In this example, three additional octbytes are read from the activated page. These column addresses (COLb, COLc, and COLd) are transferred in $T_3$, $T_4$, and $T_5$, respectively. The data octbytes (DOUTb, DOUTc, and DOUTd) are transferred in $T_5$, $T_6$, and $T_7$. The end of the data octbytes is signaled by a third command RTERM (read terminate) in $T_6$. The next REQ packet may be sent in $T_9$, or in any interval thereafter.

Figure 3b shows an example of a write transaction. The transaction begins in interval $T_0$ with the transfer of a REQ packet. The REQ packet contains, the command (ACTV / WRITE), a device, bank, and row address (BNK / ROW) of the page to be activated, and the column address (COLa) of the first octbyte to be written to the page.

The selected bank performs the activation of the selected row during $T_1$ and $T_2$ (the $t_{RCD}$ interval). A second command WSTRB (write strobe) is transferred during $T_2$ and causes the first octbyte (DINa) to be transferred during $T_3$.

In this example, three additional octbytes are written to the activated page. These column addresses (COLb, COLc, and COLd) are transferred in $T_2$, $T_3$, and $T_4$, respectively. The data octbytes (DINb, DINc, and DINd) are transferred in $T_4$, $T_5$, and $T_6$. The end of the data octbytes is signaled by a third command WTERM (write termination) in $T_6$. The next REQ packet may be sent in $T_7$, or in any interval thereafter.

## Interleaved Transactions

The previous examples showed noninterleaved transactions - the next REQ packet was transferred *after* the last data octbyte of the current transaction. In an interleaved transaction, the next REQ packet is transferred *before* the first data octbyte of the current transaction. This permits the row and column access intervals of the next transaction to overlap the data transfer of the current transaction.

Figure 4 shows an example of interleaved read transactions. The first transaction proceeds exactly as the noninterleaved example of Figure 3a (all packets of the first transaction are labeled with “1”). However, in $T_5$ the REQ packet for the second transaction is transferred (all packets of the second transaction are labeled with “2”). The $t_{RCD2}$ and $t_{CAC2}$ intervals overlap the transfer of DOUT1 data octbytes and thus increase the effective bandwidth of the RDRAM since there are no unused intervals.

A transaction consists of an address transfer phase and a data transfer phase. The REQ packet performs address transfer, and the remaining packets perform data transfer (DOUT, COL, RSTRB, and RTERM in the case of a read transaction). The time interval between the address and data transfer phases of the current transaction may be adjusted to match the data length of the previous transaction (as long as the row and column access times for the current transaction are observed). Thus, there are no limits on the types of memory transaction which may be interleaved; any mixing of transaction length and command type is permitted.

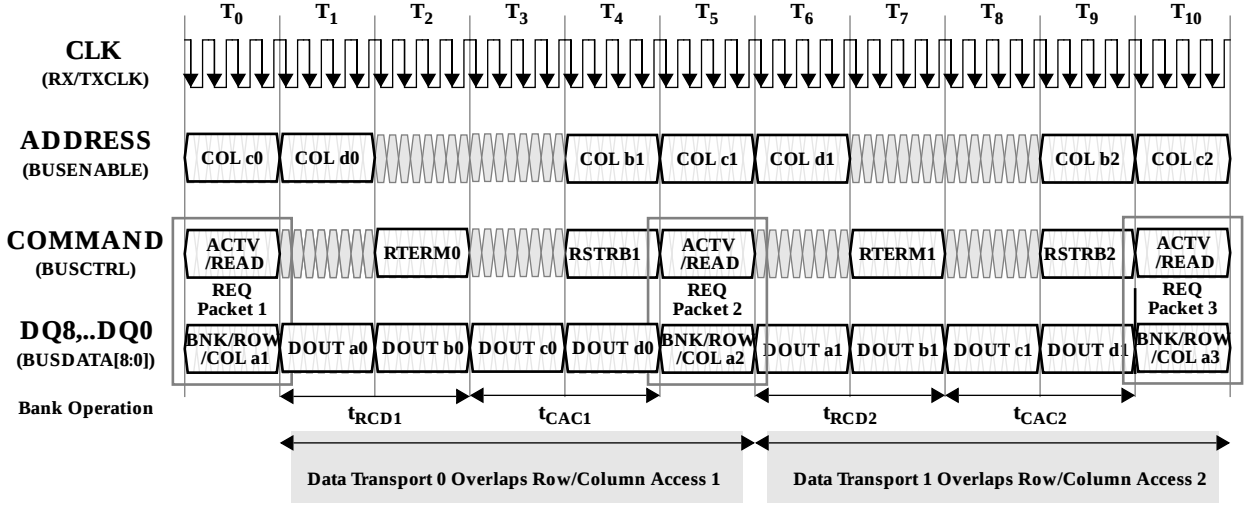



**Figure 4: Interleaved Read Transaction Example**

**SHP and SVP Pin Numbering**

| | | |
|---|---|---|
| VDD | 1 | 17 DQ4 |
| GND | 2 | 18 GND |
| DQ8 | 3 | 19 COMMAND |
| GND | 4 | 20 SIN |
| DQ7 | 5 | 21 VREF |
| NC (16/18M);VREF (64/72M) | 6 | 22 SOUT |
| ADDRESS | 7 | 23 DQ3 |
| VDD | 8 | 24 GND |
| DQ6 | 9 | 25 DQ2 |
| GND | 10 | 26 (NC) |
| DQ5 | 11 | 27 DQ1 |
| VDDA | 12 | 28 GND |
| RXCLK | 13 | 29 DQ0 |
| GNDA | 14 | 30 (NC) |
| TXCLK | 15 | 31 GND |
| VDD | 16 | 32 VDD |

**Table 1: Pin Descriptions**

| Signal | I/O | Description |
|---|---|---|
| DQ8..DQ0 (BUSDATA[8:0]) | I/O | Signal lines for REQ, DIN, and DOUT packets. The REQ packet contains the address field, command field, and other control fields. These are RSL signals[a]. |
| CLK (RXCLK) | I | Receive clock. All input packets are aligned to this clock. This is an RSL signal. [a] |
| CLK (TXCLK) | I | Transmit clock. DOUT packets are aligned with this clock. This is an RSL signal. [a] |
| VREF | I | Logic threshold reference voltage for RSL signals. |
| COMMAND (BUSCTRL) | I | Signal line for REQ, RSTRB, RTERM, WSTRB, WTERM, RESET, and CKE packets. This is an RSL signal. [a] |
| ADDRESS (BUSENABLE) | I | Signal line for COL packets with column addresses. This is an RSL signal. [a] |
| VDD, VDDA | | +3.3V power supply. VDDA is a separate analog supply for clock generation in the RDRAM. |
| GND, GNDA | | Circuit ground. GNDA is a separate analog ground for clock generation in the RDRAM. |
| SIN | I | Initialization daisy chain input. CMOS levels. |
| SOUT | O | Initialization daisy chain output. CMOS levels. |

a. RSL stands for Rambus Signaling Levels, a low-voltage-swing, active-low signaling technology.

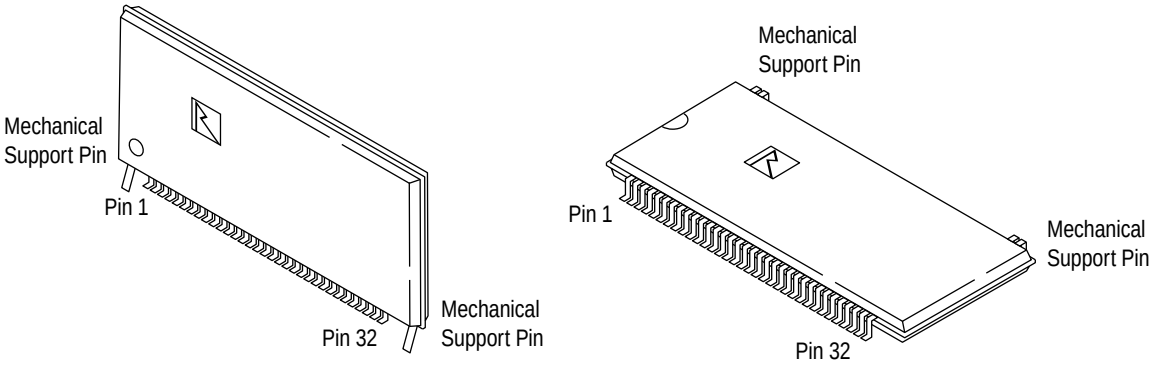



**Figure 6: Vertical SVP and Horizontal SHP Packages**

## REQ Packet (Address Transfer)

An REQ packet initiates a transaction by transferring the address and command information to the RDRAM. Figure 7 shows the format of the REQ packet. Note that each RDRAM wire carries eight bits of information in each $t_{PACKET}$.This is the time required to transfer an octbyte of data and is the natural granularity with which to illustrate timing relationships. The clock that is actually used by the RDRAM has a period of $t_{CYCLE}$, with information transferred on each clock edge. $t_{PACKET}$ is four times $t_{CYCLE}$.

In the REQ packet, the bits which are gray are reserved, and should be driven with a zero. In particular, the bits in $t_{CYCLE}$ $t_6$ and $t_7$ are needed for bus-turnaround during read transactions.

**A35..A3:** The address field A35..A3 consumes the greatest number of bits. These are allocated to device, bank, row, and column addressing according to Table 2:

**Table 2: A35..A3 Address Fields**

| Field | 16/18M (1KB Page) | 16/18M (2KB Page) | 64/72M (2KB Page) |
|---|---|---|---|
| COL | A9..A3 | A10..A3 | A10..A3 |
| ROW | A19..A10 | A19..A11 | A20..A11 |
| BNK | A20 | A20 | A22, A21 |
| DEV | A35..A21 | A35..A21 | A35..A23 |

**OP5..OP0:** The command field OP5..OP0 specifies the type of transaction that is to be performed, according to Table 3. The OP0 bit selects a read or write transaction, the OP1 bit selects a memory or register space access, and OP5..OP2 select command options.These command options include B in OP2 (see byte masking on page 14), D in OP3 for selecting broadcast operations (see refresh on page 24), and b1,b0 in OP5,OP4 (see bit masking on page 14).

**ACTV:** This bit specifies activation or precharge / activation of a bank at the beginning of a transaction, and is designated by prepending “ACTV / ” or “PRE / ACTV / ” to the command.

**AUTO:** This bit specifies auto-precharge of a bank at the end of the transaction, and is designated by appending “A” to the command.

**START:** This bit is always set to a one and indicates the beginning of a request to the RDRAM.

**REGSEL:** This bit is used for accessing registers.

**PEND2...PEND0:** This field is set to “000” for noninterleaved transactions, and to a nonzero value for interleaved transactions. This is the number of previous STRB and TERM packets the RDRAM is to skip. Refer to the *Concurrent RDRAM Design Guide* for further details.

**M7..M0:** This field is used to perform byte masking of the first data octbyte DINa for all memory write transactions (OP1, 0=01). Refer to byte masking on page 14.

**Table 3: Command Encoding**

| ACTV | AUTO | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | Command | Description |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X | 0 | 0 | READ | Read |
| 0 | 0 | b1 | b0 | D | B | 0 | 1 | WRITE | Write (b1,b0,B masking and D broadcast options) |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | RREG | Register Read |
| 0 | 0 | 0 | 0 | D | 1 | 1 | 1 | WREG | Register Write (D) |
| 0 | 1 | 0 | 0 | 0 | X | 0 | 0 | READA | Read / AutoPrecharge |
| 0 | 1 | b1 | b0 | D | B | 0 | 1 | WRITEA | Write / AutoPrecharge (b1,b0,D,B) |
| 1 | 0 | 0 | 0 | 0 | X | 0 | 0 | ACTV / READ | Activate / Read |
| 1 | 0 | b1 | b0 | D | B | 0 | 1 | ACTV / WRITE | Activate / Write (b1,b0,D,B) |
| 1 | 1 | 0 | 0 | 0 | X | 0 | 0 | ACTV / READA | Activate / Read / AutoPrecharge |
| 1 | 1 | b1 | b0 | D | B | 0 | 1 | ACTV / WRITEA | Activate / Write / AutoPrecharge (b1,b0,D,B) |
| 1 | 0 | 0 | 0 | 0 | X | 0 | 0 | PRE / ACTV / READ | Precharge / Activate / Read |
| 1 | 0 | b1 | b0 | D | B | 0 | 1 | PRE / ACTV / WRITE | Precharge / Activate / Write (b1,b0,D,B) |
| 1 | 1 | 0 | 0 | 0 | X | 0 | 0 | PRE / ACTV / READA | Precharge / Activate / Read / AutoPrecharge |
| 1 | 1 | b1 | b0 | D | B | 0 | 1 | PRE / ACTV / WRITEA | Precharge / Activate / Write / AutoPrecharge(b1,b0,D,B) |

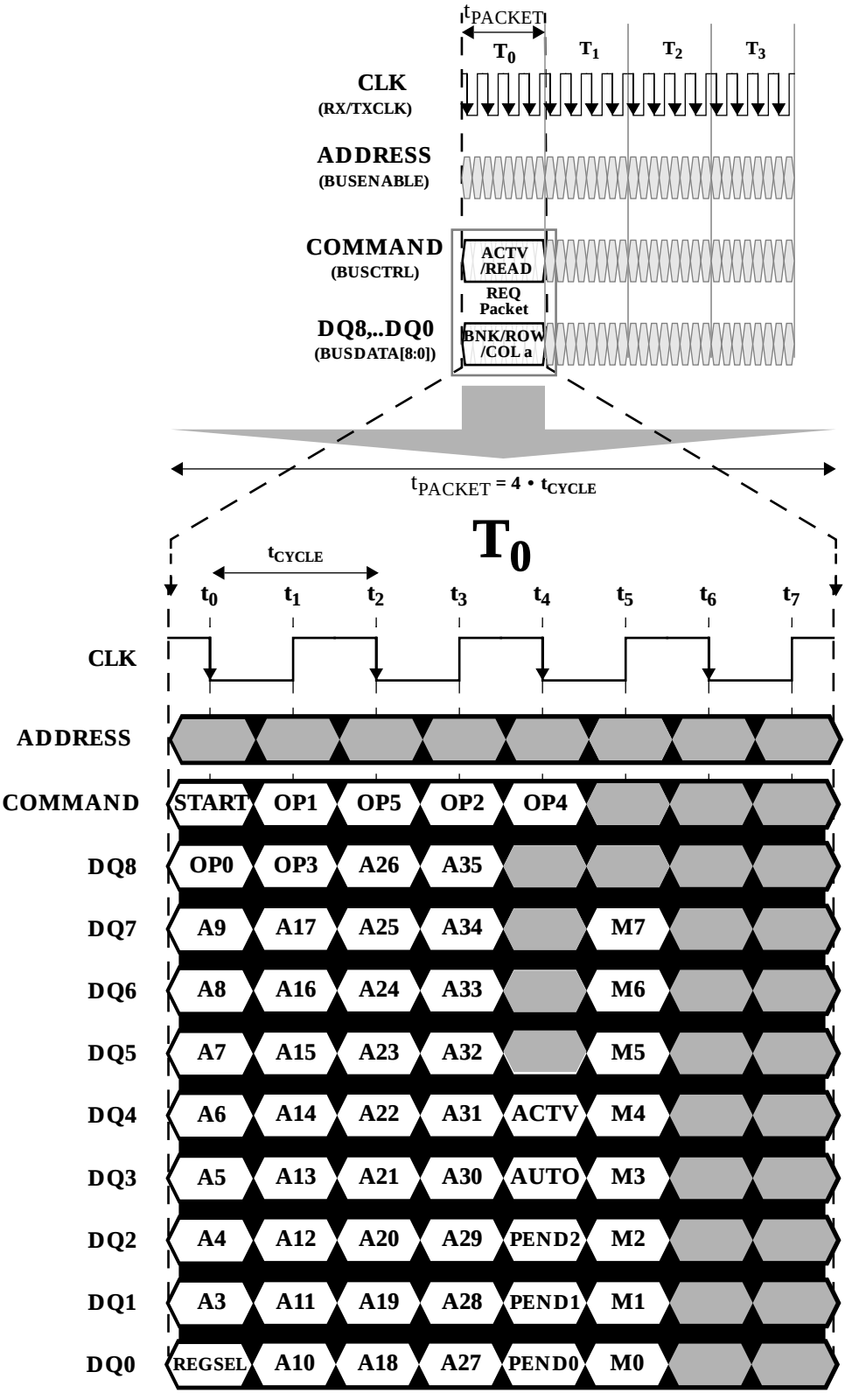



**Figure 7: REQ Packet Format**

## Data Transfer Packets

The next set of packet types are used for data transfer. Their formats are summarized in Figure 8.

As in the REQ packet, eight bits are transferred on each wire during each $t_{PACKET}$ interval. The rising and falling edges of the RDRAM clock define the transfer windows for each of these bits. The data transfer packets will align to the $t_{PACKET}$ intervals defined by the START bit of the REQ packet by simply observing the timing rules that are developed in the next few sections of this document.

### DIN and DOUT Packets

There are nine wires allocated for the data bytes. These wires are labeled DQ8..DQ0. The eight bytes transferred in a DIN or DOUT packet have 72 bits, which are labeled D0..D63 (on the DQ0..DQ7 wires) and E0..E7 (on the DQ8 wire). The 18Mbit and 72Mbit RDRAMs have storage cells for the E0..E7 bits. The E0..E7 bits are also used with byte masking operations. This is described in the section on byte masking on page 14.

### COL Packet

The column address A10..A3 of the first octbyte of data (DINa or DOUTa) is provided in the REQ packet. The COL packet contains an eight bit field A10..A3, which provides the column address for the second and subsequent data octbytes (an RDRAM with 1KByte pages uses A9..A3). The COL packets have a fixed timing relationship with respect to the DIN and DOUT packets to which they correspond. As the DIN and DOUT packets are moved (to accommodate interleaving ), the COL packets move with them.

### RSTRB and RTERM Packets

The RSTRB and RTERM packets indicate the beginning and end of the DOUT packets that are transferred during a read transaction. The RSTRB and RTERM packets are each eight bits and consist of a single “1” in an odd $t_{CYCLE}$ position, with the other seven positions “0”. Note that when a transaction transfers a single data octbyte, the RSTRB and RTERM packets will overlay one another. This is permitted and is in fact the reason that each packet consists of a single asserted bit. An example of this case is shown in Figure 15a. There will be transaction situations in which the RTERM overlays a REQ packet (two octbyte interleaved transaction). Again, this is permitted. The general rule is that the RTERM may overlay any of the other packets on the Command (BUSCTRL) wire, and RSTRB may overlay any other except for a REQ packet.

### WSTRB and WTERM Packets

The WSTRB and WTERM packets indicate the beginning and end of the series of DIN packets that are transferred during a write transaction. The WSTRB and WTERM packets are each eight bits and consist of a single “1” in an odd $t_{CYCLE}$ position, with the other seven positions “0”. Note that when a transaction transfers a single data octbyte, the WSTRB and WTERM packets will not overlay one another (unlike the case of a one octbyte read). An example of this case is shown in Figure 15b. There will be transaction situations in which the WSTRB overlays a REQ packet (no bank activate). Again, this is permitted. An example of this is shown in Figure 10a. The general rule is that the WSTRB may overlay any of the other packets on the Command (BUSCTRL) wire, and WTERM may overlay any other except for a REQ packet.

## CKE Packet

The average power of the RDRAM can be reduced by using Suspend power mode. This is done by setting the FR field of the MODE register to a zero (the MODE register is shown in Figure 18). A CKE packet must be sent a time $t_{CKE}$ ahead of each REQ packet (this is shown in interval $T_0$ in Figure 22b). This causes the RDRAM to transition from Suspend to Enable mode. When the RDRAM has finished the transaction, it returns to Suspend mode. The CKE packet will overlay the RSTRB and RTERM packets when transactions are interleaved. If the FR field is set to a one, CKE packets are not used and the RDRAM remains in Enable mode.

## RESET Packet

The RESET packet is used during initialization. When RESET packets are driven for a time $t_{RESET}$ or greater, the RDRAM will assume a known state. Because the RESET packet is limited to this one use, it will not interact with the other packet types. This is illustrated in Figure 22a.

## PWRUP Packet

The PWRUP packet is used to cause an RDRAM to transition from Powerdown to Enable mode. This is illustrated in Figure 22c.

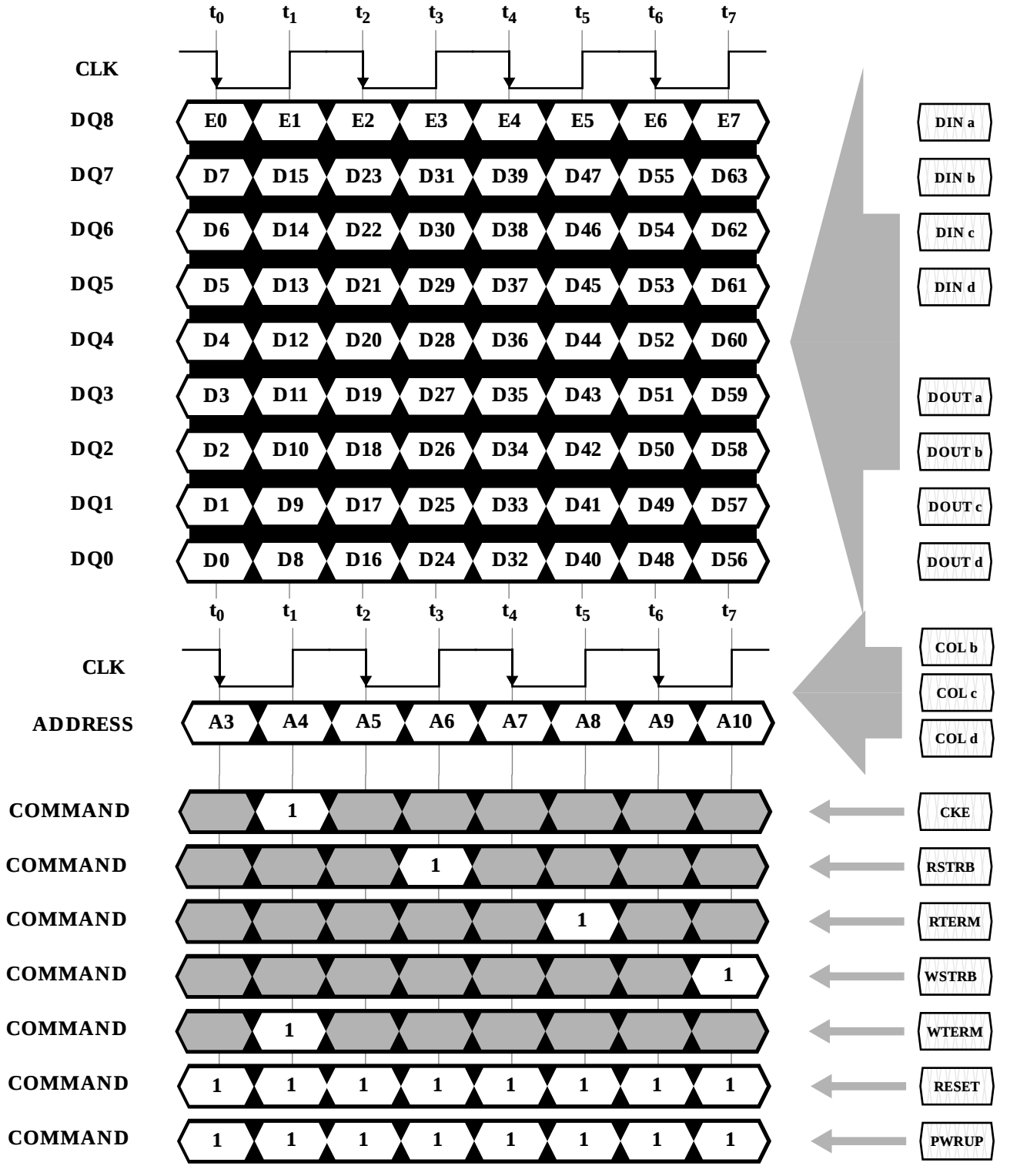



**Figure 8: DIN, DOUT, COL, CKE, RSTRB, RTERM, WSTRB, WTERM, and RESET Packet Formats**

## Read Transactions

When a controller issues a read request to an RDRAM, one of three transaction cases will occur. This is a function of the request address and the state of the RDRAM.

**READ:** The first case is shown in Figure 9a. This occurs when the requested bank has been left in an activated state and the requested row address matches the address of this activated row. This is also called a page hit read and is invoked by the READ or READA commands.

There are three timing parameters which specify the positioning of the packets which control the data transfer. These are as follows:

| | |
|---|---|
| $t_{SDR}$ | Start of RSTRB to start of DOUT |
| $t_{CDR}$ | Start of COL to start of DOUT |
| $t_{TDR}$ | Start of RTERM to end of DOUT |

These parameters are all expressed in units of $t_{CYCLE}$, and the minimum and maximum values are the same; the RSTRB, RTERM, COL, and DOUT packets move together as a block.

A fourth parameter has a minimum value only, and positions the block of data transfer packets relative to the REQ (address transfer) packet:

| | |
|---|---|
| $t_{RSR}$ | Start of REQ to start of RSTRB for READ |

When a read transaction is formed, these packet constraints must be observed. In addition, there are constraints upon the timing of the bank operations which must also be observed. These are shown in Figure 9a next to the label “Bank Operation”. After the transfer of the REQ packet in $T_0$, the RDRAM performs a column access (requiring $t_{CAC}$ for the column access time) of the first data octbyte DOUTa during $T_1$ and $T_2$. The RDRAM performs three column cycles (requiring $t_{CC}$ for the column cycle time) in order to access the next three data octbytes (DOUTb, DOUTc, DOUTd) during $T_3$,$T_4$ and $T_5$. Each data octbyte is transferred one $t_{PACKET}$ interval after it is accessed.

**ACTV/READ:** The second case is shown in Figure 9b. This occurs when the requested bank has been left in a precharged state. This is invoked by the ACTV / READ and ACTV / READA commands.

The RSTRB, RTERM, COL, and DOUT packets remain in the same relative positions as in the READ case, but they move further from the REQ packet:

| | |
|---|---|
| $t_{ASR}$ | Start of REQ to start of RSTRB for ACTV / READ |

After the transfer of the REQ packet in $T_0$, the RDRAM performs an activation operation (requiring $t_{RCD}$ for the row-column delay) during $T_1$ and $T_2$. This leaves the requested row activated. From this point the sequence of bank operations are identical to the READ case, except that everything has shifted two $t_{PACKET}$ intervals further from the REQ packet. The sum of $t_{RCD}$ and $t_{CAC}$ is also known as $t_{RAC}$ (the row access time).

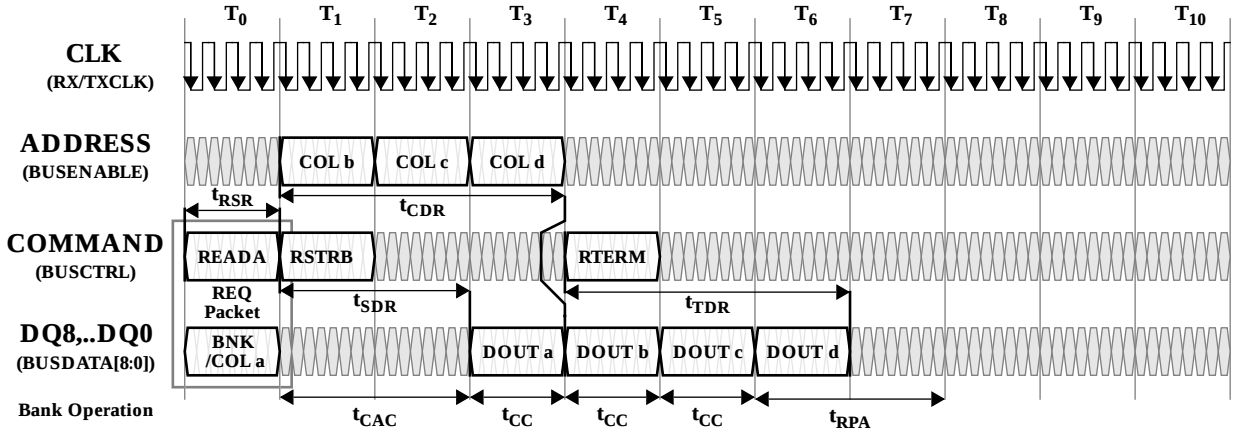
**PRE/ACTV/READ:** The third case is shown in Figure 9c. This occurs when the requested bank has been left in an activated state and the requested row address doesn’t match the address of this activated row. This is also called a page miss read and is invoked by the PRE / ACTV / READ and PRE / ACTV / READA commands. The RDRAM knows the difference between a PRE / ACTV / READ and a ACTV / READ because each RDRAM bank has a flag indicating whether it is precharged or activated. The external controller tracks this flag, and also tracks the address of each activated bank in order to distinguish READ and PRE / ACTV / READ accesses.

The RSTRB, RTERM, COL, and DOUT packets remain in the same relative positions as in the READ case, but they move further from the REQ packet:

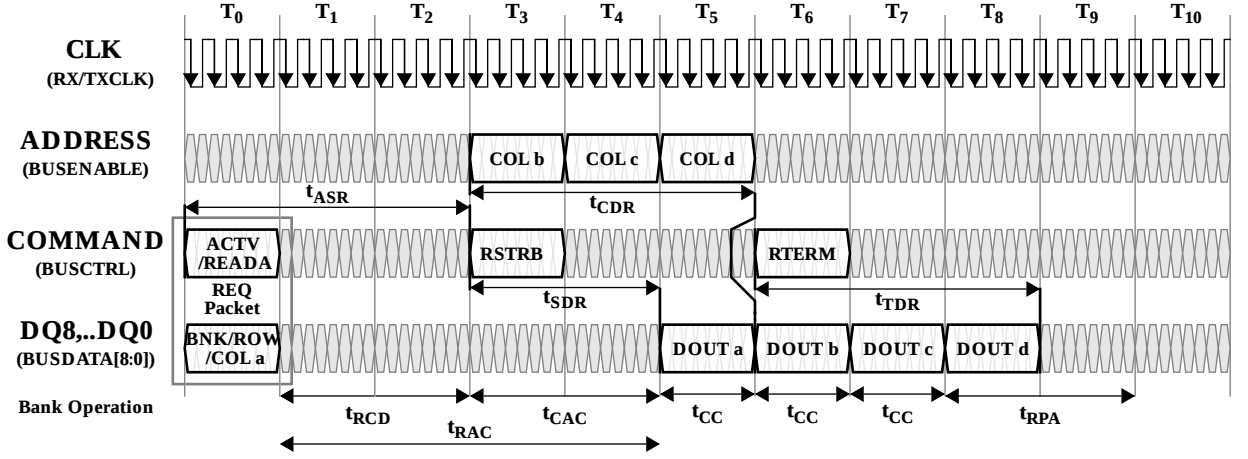
| | |
|---|---|
| $t_{PSR}$ | Start of REQ to start of RSTRB for PRE / ACTV / READ |

After the transfer of the REQ packet in $T_0$, the RDRAM performs a precharge operation ($t_{RP}$) during $T_1$ and $T_2$, and an activation operation ($t_{RCD}$) during $T_3$ and $T_4$. This leaves the requested row activated. From this point the sequence of bank operations are identical to the READ case, except that everything has shifted four $t_{PACKET}$ intervals further from the REQ packet. The sum of $t_{RP}$, $t_{RCD}$, and $t_{CAC}$ is also known as $t_{RC}$ (the row cycle time).

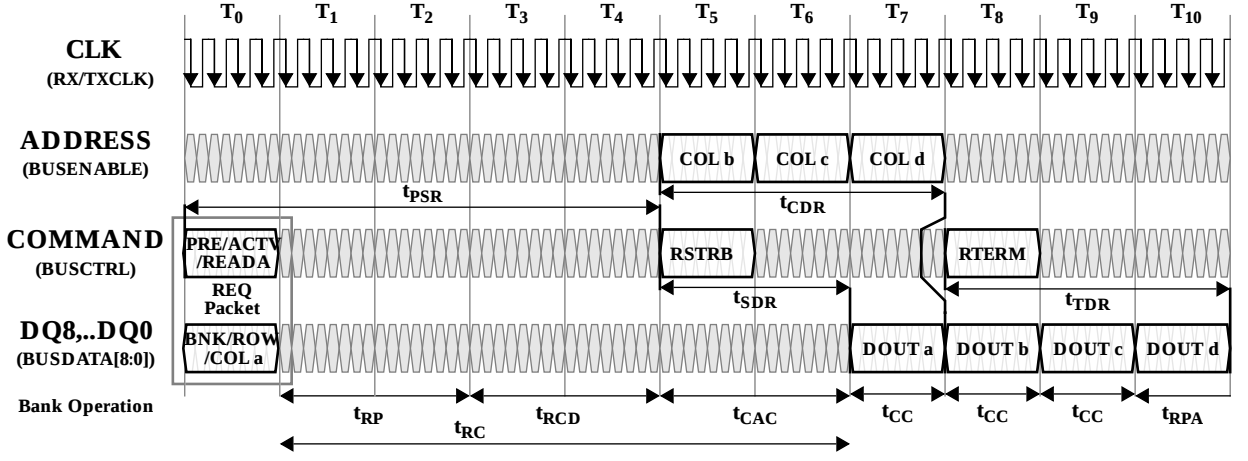
**Auto-Precharge Option:** For a READ, ACTV / READ, or a PRE / ACTV / READ command, the bank operations are complete once the last data octbyte has been accessed. The bank will be left with the requested row activated. For a READA, ACTV / READA, or a PRE / ACTV / READA command, there is an additional step. During the two $t_{PACKET}$ intervals after the last data octbyte access an auto-precharge operation (requiring $t_{RPA}$ for the row precharge, auto) is performed. This leaves the bank in a precharged state.




**(a) READA - RANDOM READ CYCLES WITHIN A PAGE**




**(b) ACTV/READA - BANK ACTIVATE AND RANDOM READ CYCLES WITHIN A PAGE**




**(c) PRE/ACTV/READA - BANK PRECHARGE/ACTIVATE AND RANDOM READ CYCLES IN A PAGE**

**Figure 9: Read Transactions**

## Write Transactions

When a controller issues a write request to an RDRAM, one of three transaction cases will occur. This is a function of the request address and the state of the RDRAM.

**WRITE:** The first case is shown in Figure 10a. This occurs when the requested bank has been left in an activated state and the requested row address matches the address of this activated row. This is called a page hit write and is invoked by the WRITE or WRITEA commands.

There are three timing parameters which specify the positioning of the packets which control the data transfer. These are as follows:

| | |
|---|---|
| $t_{SDW}$ | Start of WSTRB to start of DIN |
| $t_{CDW}$ | Start of COL to start of DIN |
| $t_{TDW}$ | Start of WTERM to end of DIN |

These parameters are all expressed in units of $t_{CYCLE}$, and the minimum and maximum values are the same; the WSTRB, WTERM, COL, and DIN packets move together as a block.

A fourth parameter has a minimum value only, and positions the block of data transfer packets relative to the REQ (address transfer) packet:

| | |
|---|---|
| $t_{WSW}$ | Start of REQ to start of WSTRB for WRITE |

When a write transaction is formed, these packet constraints must be observed. In addition, there are constraints upon the timing of the bank operations which must also be observed. These are shown in Figure 10a next to the label “Bank Operation”. After the transfer of the REQ packet in $T_0$, the RDRAM performs a column access (requiring $t_{CAC}$ for the column access time) of the first data octbyte DINa during $T_1$ and $T_2$. The RDRAM performs three column cycles (requiring $t_{CC}$ for the column cycle time) in order to retire the next three data octbytes (DINb, DINc, DINd) during $T_3$, $T_4$ and $T_5$. Each data octbyte is transferred one $t_{PACKET}$ interval before it is stored.

**ACTV/WRITE:** The second case is shown in Figure 10b. This occurs when the requested bank has been left in a precharged state. This is invoked by the ACTV / WRITE and ACTV / WRITEA commands.

The WSTRB, WTERM, COL, and DIN packets remain in the same relative positions as in the page hit case, but they move further from the REQ packet:

| | |
|---|---|
| $t_{ASW}$ | Start of REQ to start of WSTRB for ACTV / WRITE |

After the transfer of the REQ packet in $T_0$, the RDRAM performs an activation operation (called $t_{RCD}$ or row-column delay) during $T_1$ and $T_2$. This leaves the requested row activated. From this point the sequence of bank operations are identical to the WRITE case, except that everything has shifted two $t_{PACKET}$ intervals further from the REQ packet. The sum of $t_{RCD}$ and $t_{CAC}$ is also known as $t_{RAC}$ (the row access time).

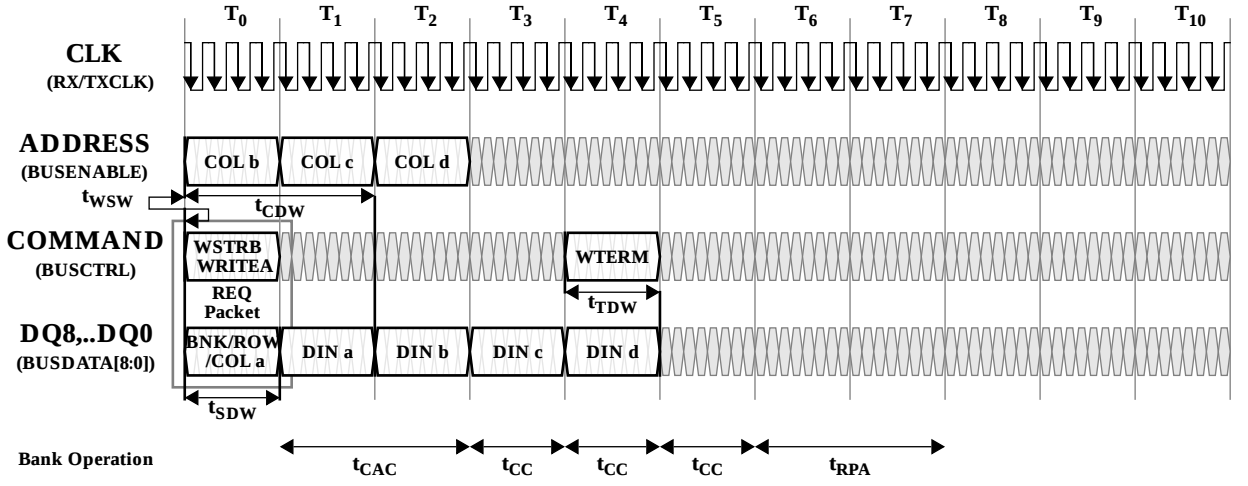
**PRE/ACTV/WRITE:** The third case is shown in Figure 10c. This occurs when the requested bank has been left in an activated state and the requested row address doesn’t match the address of this activated row. This is also called a page miss write and is invoked by the PRE / ACTV / WRITE and PRE / ACTV / WRITEA commands. The RDRAM knows the difference between a PRE / ACTV / WRITE and a ACTV / WRITE because each RDRAM bank has a flag indicating whether it is precharged or activated. The external controller tracks this flag, and also tracks the address of each activated bank in order to distinguish PRE / ACTV / WRITE and WRITE accesses.

The WSTRB, WTERM, COL, and DIN packets remain in the same relative positions as in the WRITE case, but they move further from the REQ packet:

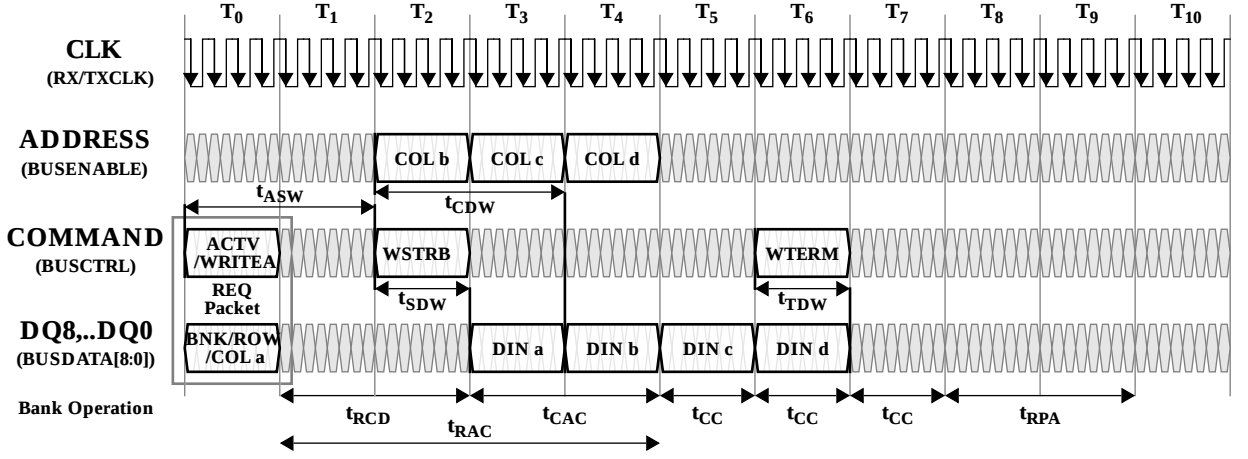
| | |
|---|---|
| $t_{PSW}$ | Start of REQ to start of WSTRB for PRE / ACTV / WRITE |

After the transfer of the REQ packet in $T_0$, the RDRAM performs a precharge operation ($t_{RP}$) during $T_1$ and $T_2$, and an activation operation ($t_{RCD}$) of during $T_3$ and $T_4$. This leaves the requested row activated. From this point the sequence of bank operations are identical to the WRITE case, except that everything has shifted four $t_{PACKET}$ intervals further from the REQ packet. The sum of $t_{RP}$, $t_{RCD}$, and $t_{CAC}$ is also known as $t_{RC}$ (the row cycle time).

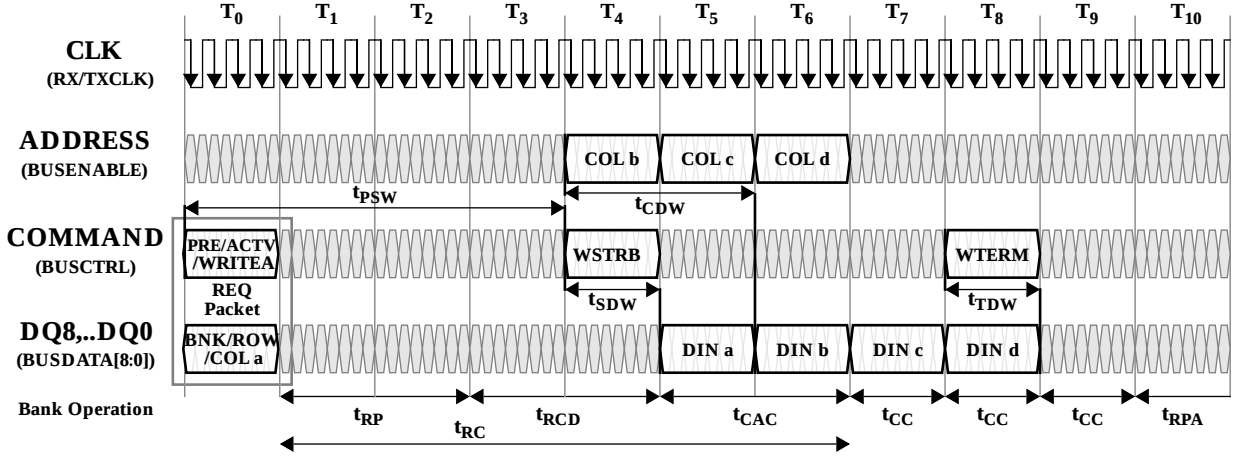
**Auto-Precharge Option:** For a WRITE, ACTV / WRITE or a PRE / ACTV / WRITE command, the bank operations are complete once the last data octbyte has been accessed. The bank will be left with the requested row activated. For a WRITEA, ACTV / WRITEA or a PRE / ACTV / WRITEA command, there is an additional step. During the two $t_{PACKET}$ intervals after the last data octbyte access an auto-precharge operation (requiring $t_{RPA}$ for the row precharge, auto) is performed. This leaves the bank in a precharged state.




**(a) WRITEA - RANDOM WRITE CYCLES WITHIN A PAGE**




**(b) ACTV/WRITEA - BANK ACTIVATE AND RANDOM WRITE CYCLES WITHIN A PAGE**




**(c) PRE/ACTV/WRITEA - BANK PRECHARGE/ACTIVATE AND RANDOM WRITE CYCLES IN A PAGE**

**Figure 10: Write Transactions**

## Bytemask Operations

All memory write transactions (OP1,OP0=01) use the M7..M0 field of the REQ packet to control byte masking of the first octbyte DINa of write data. M7 controls bits D56..D63,E7 while M0 controls bits D0..D7,E0. A “0” means don’t write and a “1” means write.

The M7..M0 field should be filled with “00000000” for non-memory-write transactions.

**OP2=1:** When OP2=1 for a memory write transaction, the remaining data octbytes (DINb, DINc,...) are written unconditionally (all bytes are written).

**OP2=0:** When OP2=0, the remaining data octbytes (DINb, DINc,...) are written with a bytemask. Each bytemask is carried on the DQ8 wire, pipelined one $t_{PACKET}$ interval ahead of the data octbyte it controls.

Figure 13b shows the format of the M packet and DIN packet when OP2=0. M7 controls bits D56..D63 (of the next DIN packet) and M0 controls bits D0..D7 (of the next DIN packet). Figure 13a summarizes the location of the M packets and the DIN packets they control.

When 16M and 64M RDRAMs are used, there is no limitation caused by the use of bytemask operations; the DQ8 wire is only used for the REQ packet and M packets.

When 18M and 72M RDRAMs are used, there is a limitation caused by the use of bytemask operations; the E7..E0 bits of the 72 bit DIN packet may not be used when OP2=0. To achieve bytemasking, it will be necessary to use read-modify-write operations or single-octbyte writes with the bytemask in the REQ packet and OP2=1.

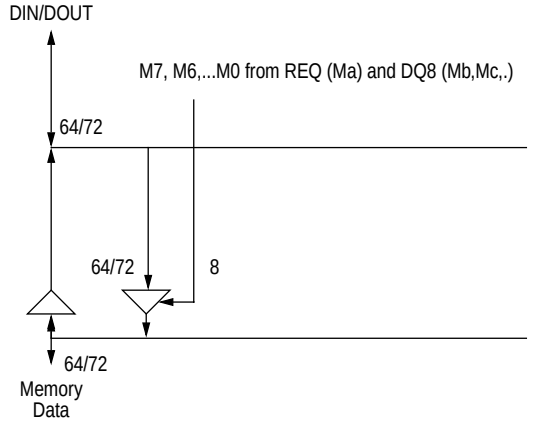



**Figure 11: Details of ByteMask Logic**

## Bitmask Operations

All memory write transactions (OP1,OP0=01) may use bitmask operations (OP5,OP4). Bitmask operations may be used simultaneously with the bytemask operations just described; a particular data bit is written only if the corresponding bytemask M and bitmask m are set.

**OP5,OP4=00:** This is the default option with no bitmask operation selected; all data bits are written, subject to any bytemask operation.

**OP5,OP4=01:** This is the write-per-bit option. Figure 14a shows the transaction format. The 64 / 72-bit MASK register is used as a static bit mask, controlling whether each of the 64 / 72 bits of DIN octbytes is written (m=1) or not written (m=0). The MASK register is loaded using the dynamic bitmask operation (OP5,OP4=10).

**OP5,OP4=10:** This is the dynamic bitmask option. Figure 14b shows the transaction format. Alternate octbytes (ma, mc,..) are loaded into the MASK register to be used as a bitmask for the data octbytes (DINb, DINd,...). Only the COL packets which correspond to DIN packets (COLb, COLd,..) contain a valid column address. The MASK register is left with the last bitmask that is transferred (mc in this case). The write-enable signal is asserted after DIN packet (Figure 12).

**OP5,OP4=11:** This is the mask-per-bit option. Figure 14c shows the transaction format. The 64 / 72-bit MASK register is used as a static data octbyte DIN. The bitmask packets (ma, mb,...) control whether the data is written (m=1) or not written (m=0). The MASK register is loaded using the dynamic bitmask operation (OP5,OP4=10).

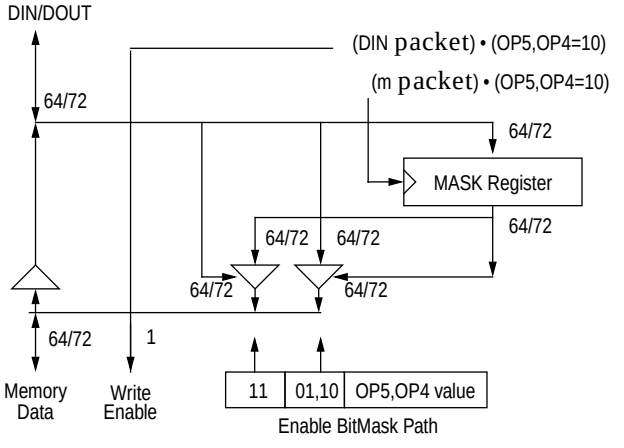
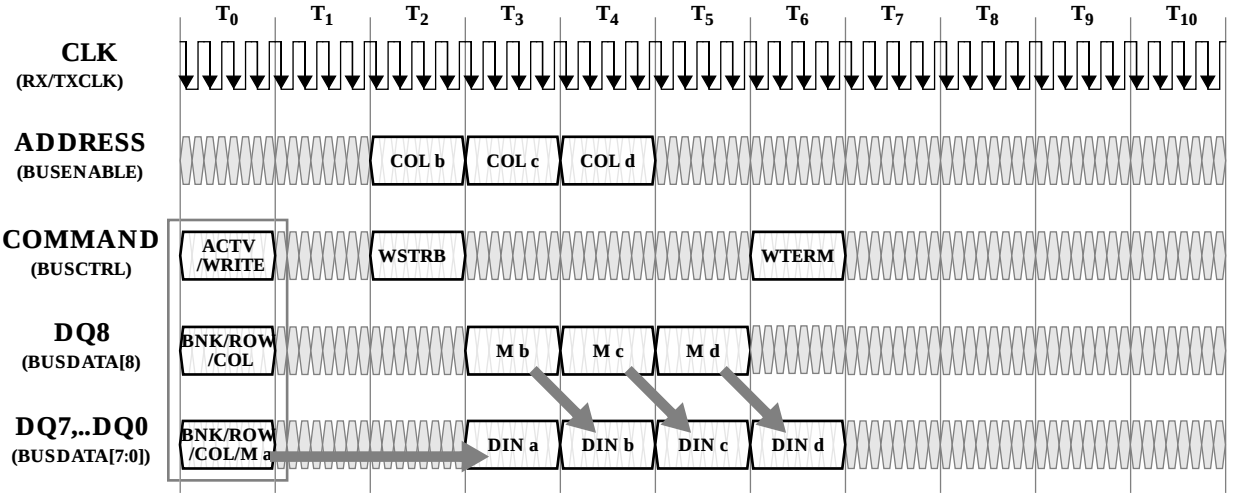
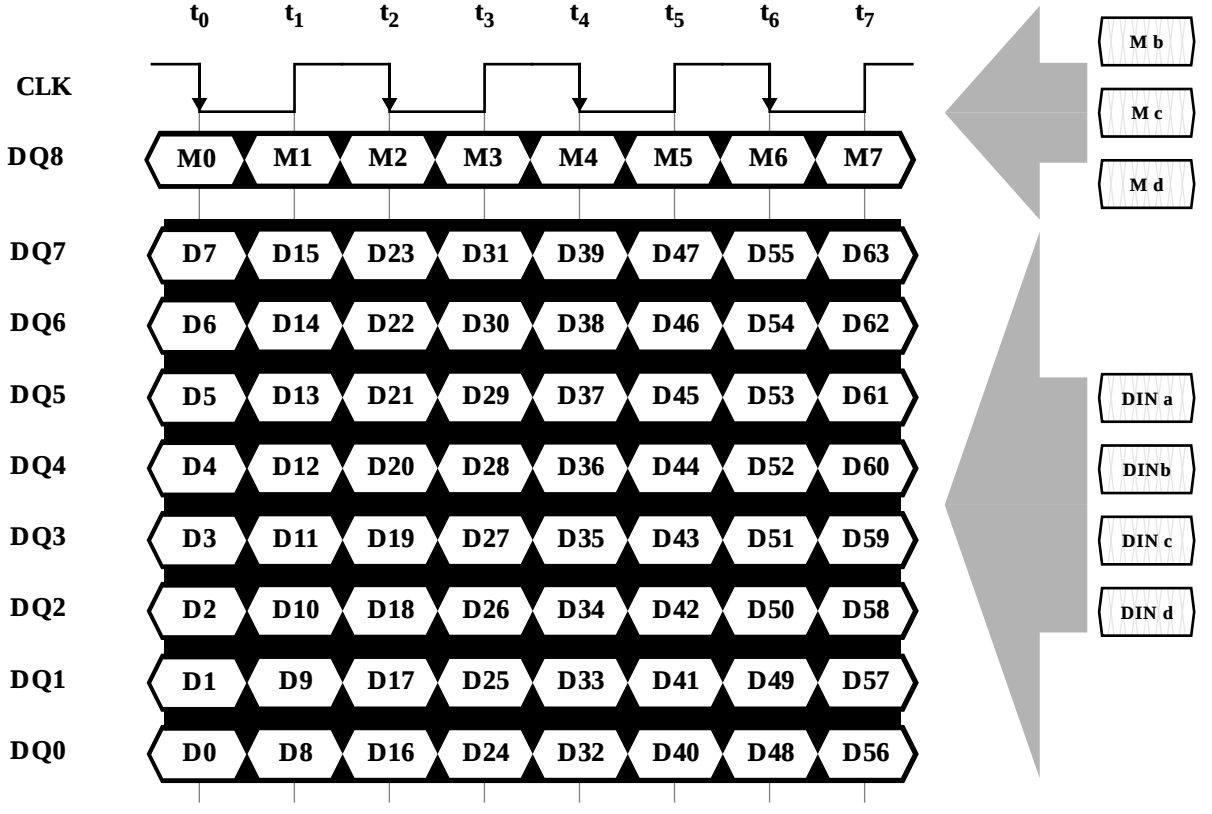



**Figure 12: Details of BitMask Logic**

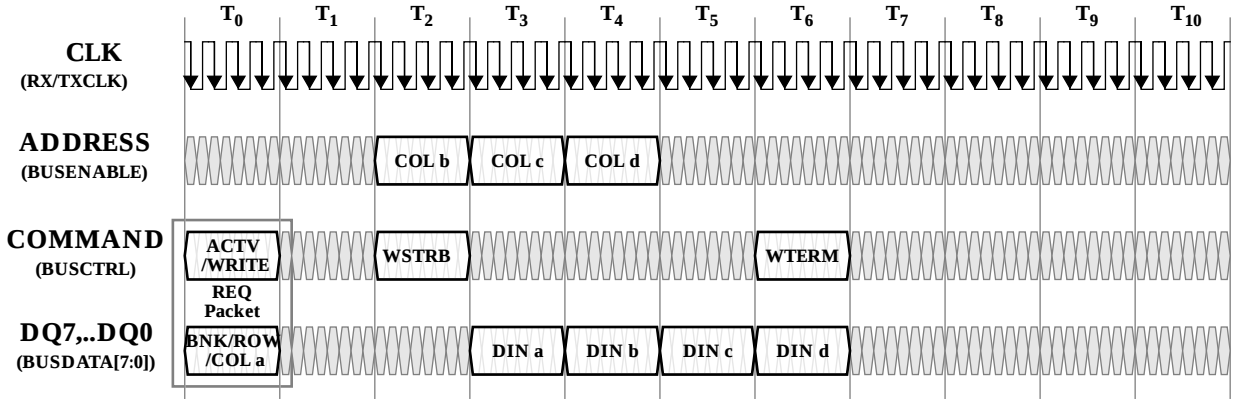



**(a) OP2 = 0 - WRITE TRANSACTION WITH BYTEMASK**

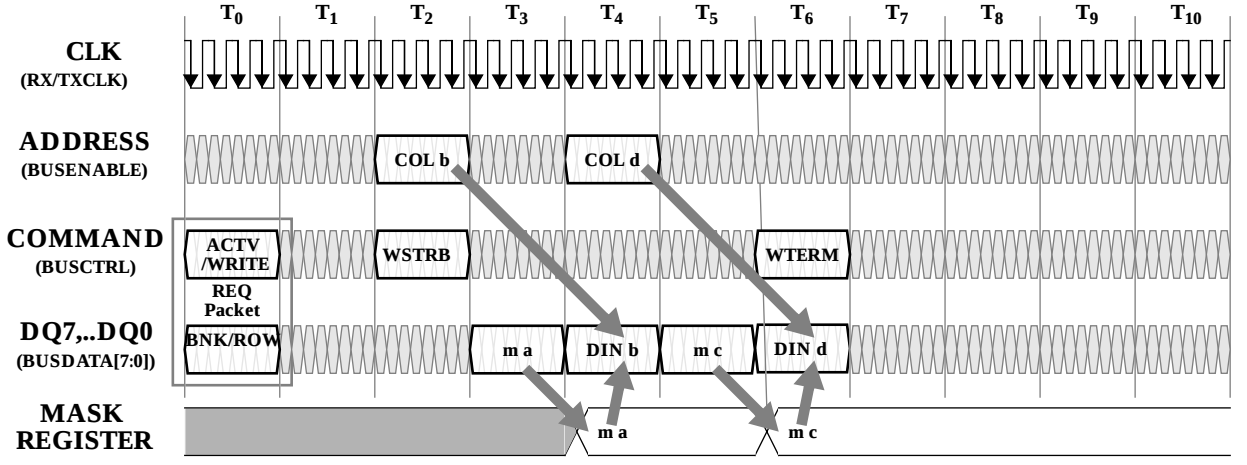



**(b) OP2 = 0 - DATA AND BYTEMASK PACKET FORMATS**

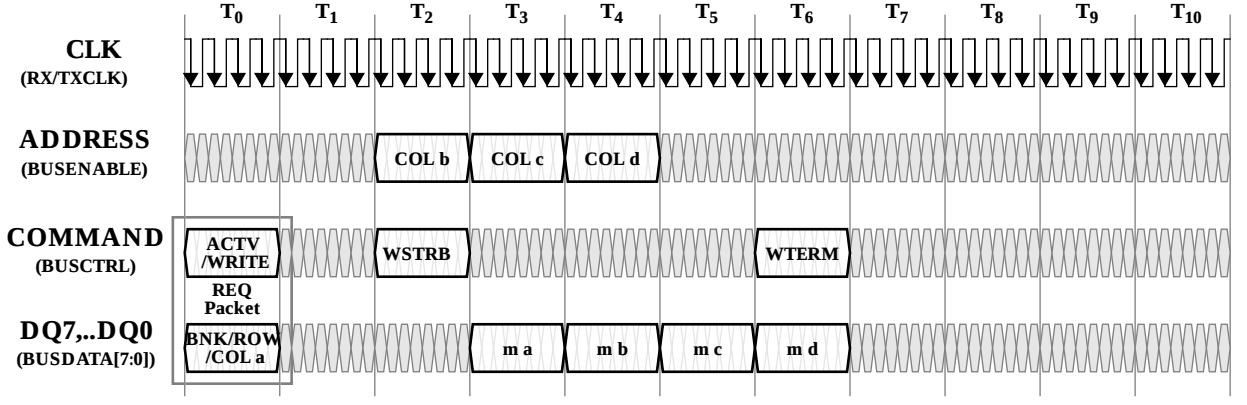
**Figure 13: Bytemask Operations**




**(a) OP5,OP4 = 0,1 - BITMASK IN MASK REGISTER, DATA FROM DQ INPUTS**




**(B) OP5,OP4 = 1,0 - BITMASK FROM DQ INPUTS, DATA FROM DQ INPUTS**




**(B) OP5,OP4 = 1,1 - BITMASK FROM DQ INPUTS, DATA IN MASK REGISTER**

**Figure 14: Bitmask Operations**

## Registers

There are six control registers in an RDRAM. They contain read-only fields, which allow a memory controller to determine the type of RDRAM that is present. They also contain read-write fields which are used to configure the RDRAM.

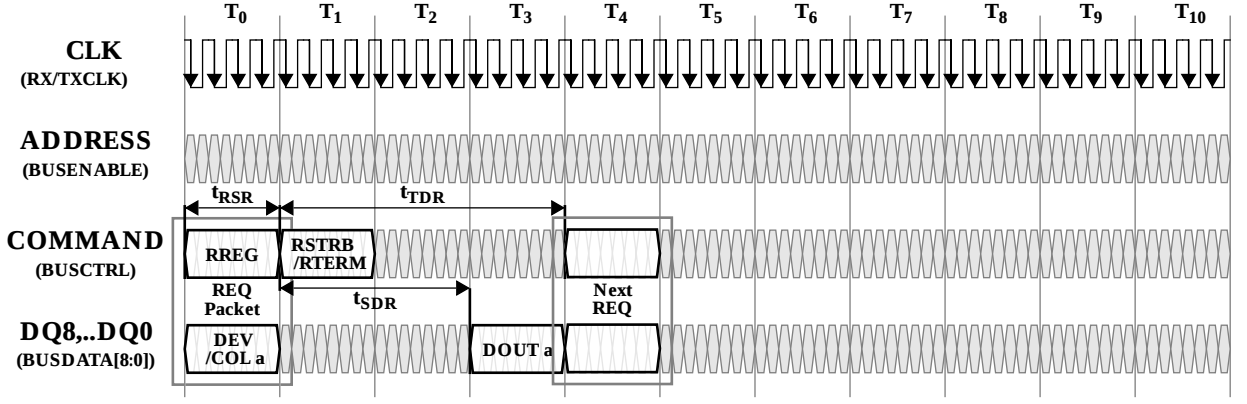
Registers are read and written with transactions that are identical to one-octbyte memory read and write transactions. These transaction formats are illustrated in Figure 15. There is one difference with respect to memory transactions; for a register write, it is necessary to allow a time of $t_{WREG}$ to elapse before another transaction is directed to the RDRAM.

In the descriptions of some of the read-write fields, the user is instructed to set the field to a default value ("Set to 1.", for example). When this is done, the suggested value is the one needed for normal operation of the RDRAM.

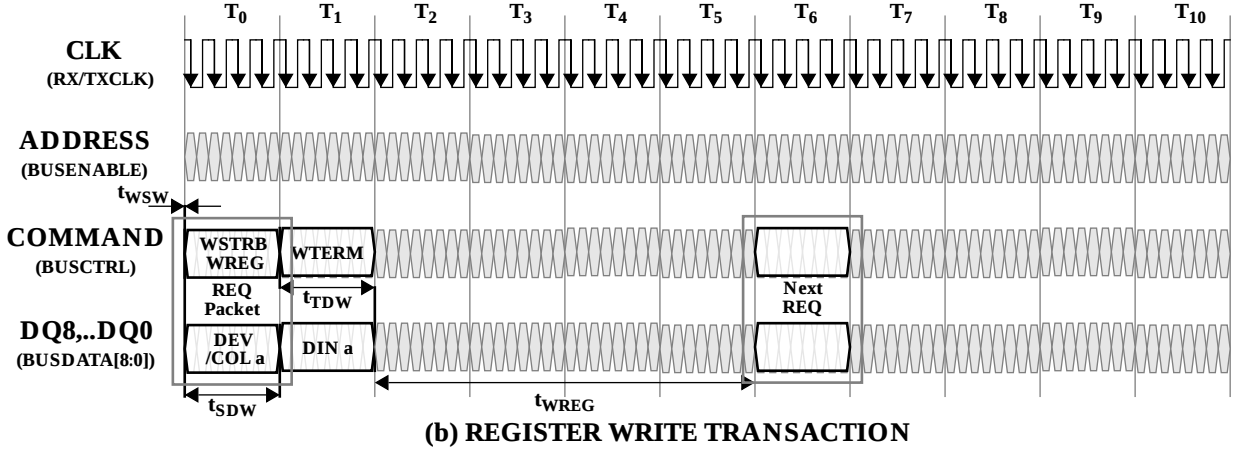
A summary of the control registers and a brief description follows

| | |
|---|---|
| DEVICETYPE | RDRAM size, type information |
| DEVICEID | Set RDRAM base address |
| MODE | Set RDRAM operating modes |
| REFROW | Set refresh address for Powerdown |
| RASINTERVAL | Set RAS intervals |
| DEVICEMFGR | RDRAM manufacturer information |

The control register fields are described in detail in the next six pages. The format of the one octbyte DIN or DOUT packet that is written to or read from the register is shown. Gray bits are reserved, and should be written as zero. The value of the A10..A3,REGSEL field needed to access each register is also shown. The ROW and BANK address fields are not used for register read and write transactions.



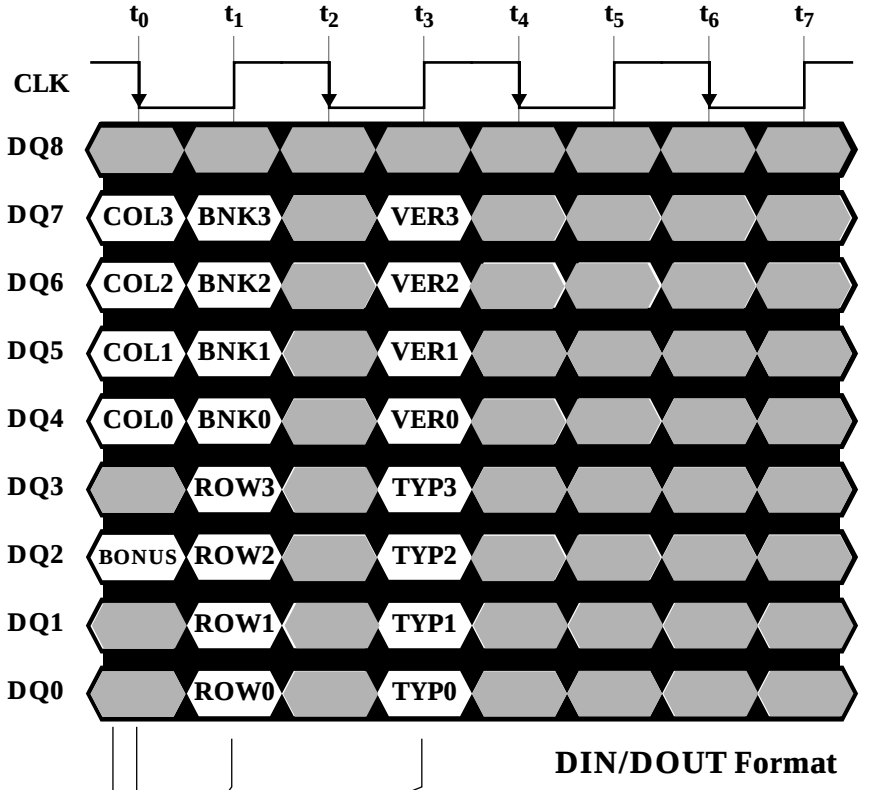

**(a) REGISTER READ TRANSACTION**




**(b) REGISTER WRITE TRANSACTION**

**Figure 15: Register Transactions**

| DEVICETYPE Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000000000_2$ |
|---|---|---|




DIN/DOUT Format

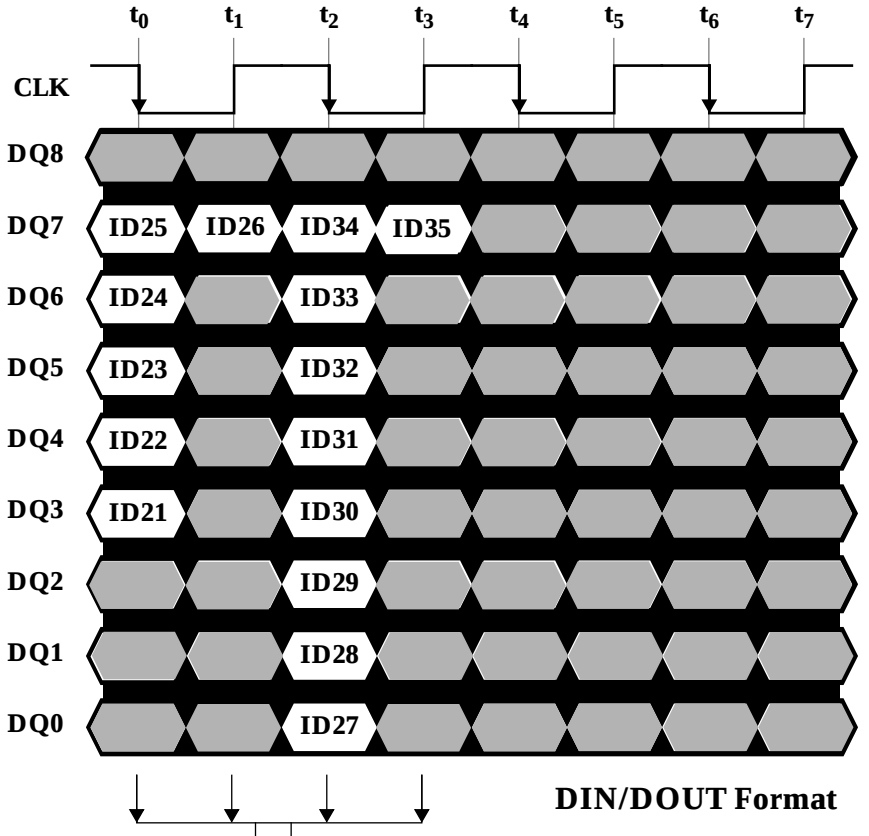
## Description

This is a read only register with fields that describe the characteristics of the device. This includes the number of address bits for bank, row, and column. The column count includes the (unimplemented) A2,A1,A0 bits. The other fields specify the architecture version, the device type, and the byte size. This register is read during initialization so the memory controller can determine the proper memory configuration.

| Field | 1KByte Page | | 2KByte Page | | | | Description |
|---|---|---|---|---|---|---|---|
| | 16M | 18M | 16M | 18M | 64M | 72M | |
| VER3...VER0 | $0010_2$ | | | | | | Architecture Version is Concurrent |
| TYP3...TYP0 | $0000_2$ | | | | | | Device is DRAM |
| BNK3...BNK0 | $0001_2$ = 1 | | $0001_2$ = 1 | | $0010_2$ = 2 | | Number of bank address bits |
| ROW3...ROW0 | $1010_2$ = 10 | | $1001_2$= 9 | | $1010_2$= 10 | | Number of row address bits |
| COL3...COL0 | $1010_2$= 10 | | $1011_2$= 11 | | $1011_2$= 11 | | Number of column address bits |
| BONUS | 0 | 1 | 0 | 1 | 0 | 1 | Specifies x8(0) or x9(1) byte length |

**Figure 16: DEVICETYPE Register**

| DEVICEID Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000000001_2$ |
|---|---|---|



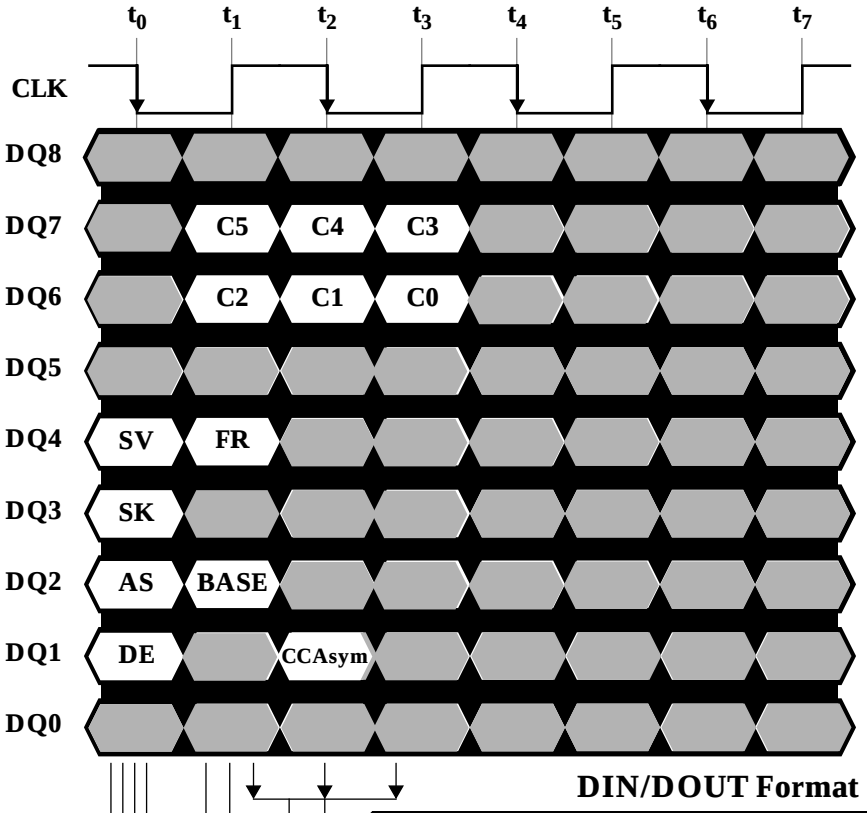

## Description

**This is a read-write register with a single field ID35...ID21. This field is compared to the A35...A21 address bits of the REQ packet to determine if the current transaction is directed to this RDRAM. If the OP3 bit of the REQ packet is set, then this match is ignored (broadcast operation to all RDRAMs). Note that some low order bits of this field are not compared for the higher density RDRAMs (see below).**

| Field | RDRAM Size | Description |
|---|---|---|
| ID35...ID21 | 16M/18M | Compared to A35...A21 for device match |
| ID35...ID23 | 64M/72M | Compared to A35...A23 for device match |

**Figure 17: DEVICEID Register**

| MODE Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000000011_2$ |
|---|---|---|




## Description

**This is a read-write register with fields that control the operating modes of the RDRAM. The modes include output current control (C5..C0), clock/power control (FR,FT), compatibility control (BASE), $t_{TR}$ skip control (SV, SK, AS), and initialization control (DE). Refer to the *Concurrent RDRAM Design Guide* for a detailed discussion of the use of these fields.**

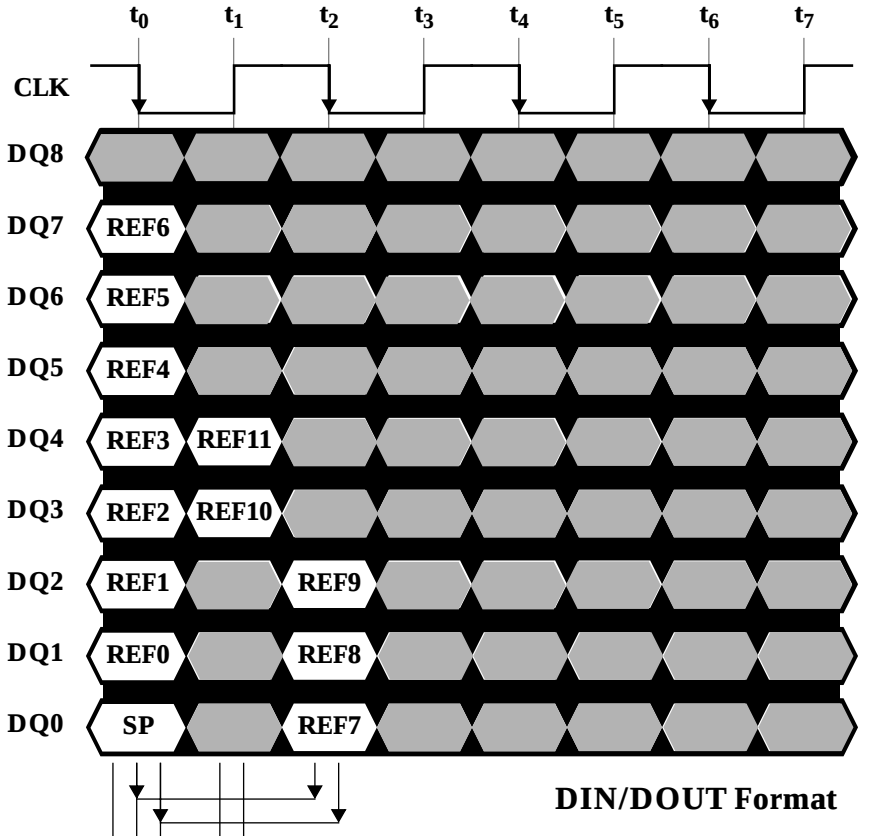
**The reset values in the MODE registers are all zeros except the AS=1 and C5...C0=111111.**

### DIN/DOUT Format

| Field | Description |
|---|---|
| C5...C0 | Specifies $I_{OL}$ output current. $000000_2 \Rightarrow$min, $111111_2 \Rightarrow$max. |
| FR | Force internal clock on. FR=1 $\Rightarrow$ RDRAM Enable. |
| BASE | Set to 1 if Base RDRAMs with acknowledge are present. |
| SV | Skip value for auto $t_{TR}$ control. Read-only. |
| SK | Specifies Skip value for manual $t_{TR}$ control. Set to 0. |
| AS | Specifies manual (0) or auto (1) $t_{TR}$ control. Set to 1. |
| DE | Device Enable. Used during initialization. |
| CCAsym | Current Control - Asymmetry adjustment.. |

**Figure 18: MODE Register**

| REFROW Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000000101_2$ |
|---|---|---|




## Description

**This is a read-write register which is used to track the bank/row address that will be refreshed by the next SIN pulse in Powerdown mode. This register is not used for normal refresh in Enable mode - the bank/row address is supplied by the external controller in the refresh transaction.**

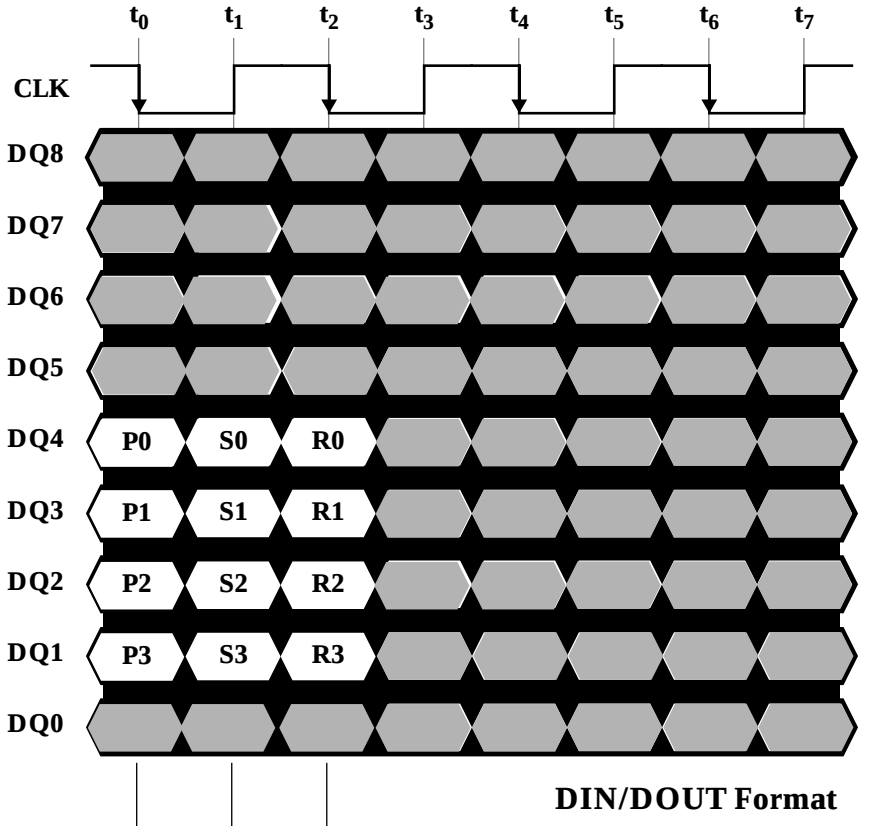
**Powerdown is entered by setting the SP field to one. The REF field should be simultaneously set with the next bank/row to be refreshed. When Powerdown is exited, this register is read from one RDRAM to set the proper bank/row address for normal refresh operation.**

**The reset values of the REFROW registers are all zeros.**

| Field | RDRAM Size | Description |
|---|---|---|
| REF10 | 16M/18M - 1 or 2KB Page | Bank address of next row to be refreshed |
| REF11,REF10 | 64M/72M - 2KB Page | Bank address of next row to be refreshed |
| REF8...REF0 | 16M/18M - 2KB Page | Row address of next row to be refreshed |
| REF9...REF0 | 16M/18M - 1KB Page<br>64M/72M - 2KB Page | Row address of next row to be refreshed |
| SP | - | Set to enter Powerdown mode. |

**Figure 19: REFROW Register**

| RASINTERVAL Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000000110_2$ |
|---|---|---|




## Description

This is a read-write register with fields that control the length of the RAS intervals of the RDRAM. The relationship between the $t_{RC}$, $t_{RCD}$, $t_{RPA}$ and $t_{RP}$ intervals (in $t_{CYCLE}$ units) and the P, S, and R fields follows:

$t_{RC} = (1010_2+R+S+P) \cdot t_{CYCLE}$

$t_{RCD} = (0101_2+S) \cdot t_{CYCLE}$

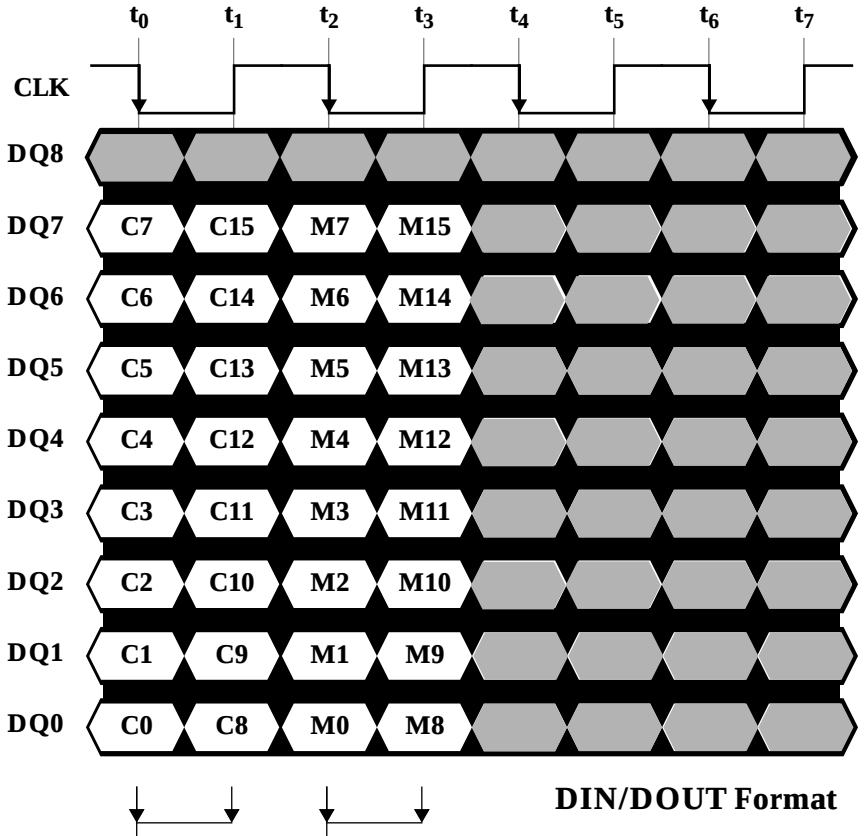
$t_{RP} = (0101_2+P) \cdot t_{CYCLE}$

$t_{RPA} = (0101_2+P) \cdot t_{CYCLE}$

| Field | Description |
|---|---|
| R3...R0 | Specifies the ($t_{RC}$ - $t_{RCD}$ - $t_{RP}$) restore interval. Set to $0111_2$. |
| S3...S0 | Specifies the $t_{RCD}$ sense interval. Set to $0011_2$. |
| P3...P 0 | Specifies the $t_{RP}$ and $t_{RPA}$ precharge intervals. Set to $0011_2$. |

**Figure 20: RASINTERVAL Register**

| DEVICEMFGR Register | A10,A9,A8,A7,A6,A5,A4,A3,REGSEL | $000001001_2$ |
|---|---|---|




## Description

**This is a read-only register with fields that specify the manufacturer's identification number and manufacturer-specific date-code and version information.**

**Contact Rambus for a list of manufacturers' identification numbers.**

| Field | Description |
|---|---|
| M15...M0 | Manufacturer's identification number |
| C15...C0 | Manufacturer's datecode or version information |

**Figure 21: DEVICEMFGR Register**

## Initialization

The first step in initialization is to reset the RDRAM. This is accomplished by driving RESET packets for a time $t_{RESET}$ or greater. This causes the RDRAM to assume a known state. This also causes the internal clocking logic (a delay-locked-loop) to begin locking to the external clock. This requires a time of $t_{LOCK}$. At this point, the RDRAM is ready to accept transactions. This timing sequence is shown in Figure 22a.

The next step for the memory controller is to read and write the six control registers, in order to determine the size and type of RDRAM that is present, and to configure it properly. A full initialization sequence is provided in the *Concurrent RDRAM Design Guide*.

## Power Management

There are several power modes available in an RDRAM. These modes permit power dissipation and latency to be traded against one another.

**Enable Mode:** The simplest option is to remain permanently in Enable power mode. This is done by setting the FR field to a one in the MODE register (refer to Figure 18). The RDRAM will return to Enable mode when it is not performing a read or write transaction. This is the operating mode which has been assumed in all the transaction timing diagrams (except in Figure 22b).

**Suspend Mode:** The average power can be reduced by using Suspend power mode. This is done by setting the FR field to a zero. A CKE packet must be sent a time $t_{CKE}$ ahead of each REQ packet (this is shown in $T_0$ in Figure 22b). This causes the RDRAM to transition from Suspend to Enable mode. When the RDRAM has finished the transaction, it returns to Suspend mode. The average power of the RDRAM is reduced, but at the cost of slightly greater latency. There is no loss of effective bandwidth, since the CKE packet may be overlapped with the other packet types.

**Powerdown Mode:** The RDRAM power can be reduced to a very low level with Powerdown mode. Powerdown is entered by setting the SP field of the REFROW register to one (the REF field is simultaneously set to the next bank and row to be refreshed). As a result, most of the RDRAM's circuitry is disabled, although its memory must still be refreshed. This is accomplished by pulsing the SIN input with a cycle time of $t_{SCYCLE}$ or less. This is illustrated in Figure 25a.

Powerdown mode is exited when PWRUP packets are asserted for a time $t_{PWRUP}$ on the Command wire. The internal clocking logic will begin locking to the external clock. After a time of $t_{LOCK}$ the RDRAM will be in Enable mode, ready for the next REQ packet. This is illustrated in Figure 22c.

## Refresh

Memory refresh (when not in Powerdown) uses a one-octbyte broadcast memory write with the following REQ field values:

| | | | |
|---|---|---|---|
| OP5..0 | $001001_2$ | A35..3 | DEV: 0..0 (unused) |
| AUTO | 1 | | BNK: next bank |
| ACTV | 1 | | ROW: next row |
| PEND | 000 / 001 / 010 | | COL: 0..0 (unused) |
| M7..0 | $00000000_2$ | REGSEL: | 0 |

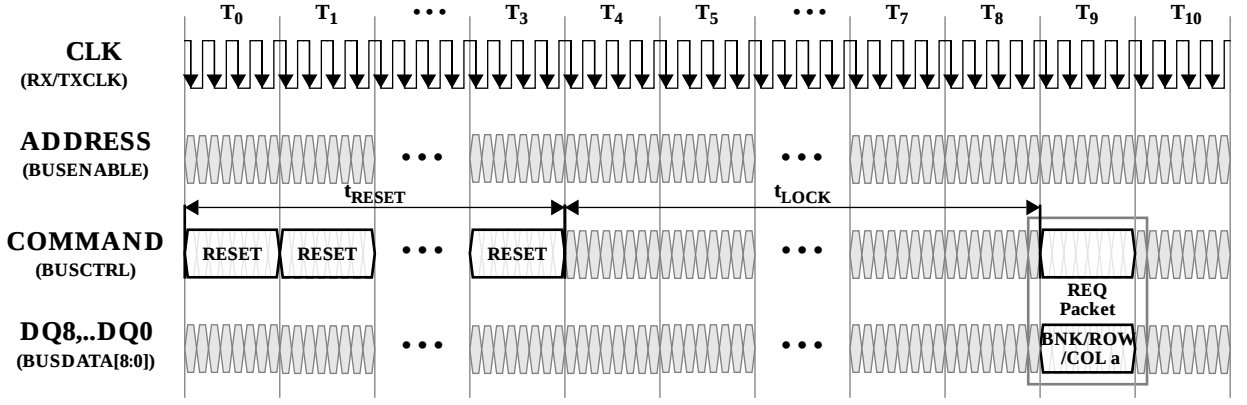
The transaction format for memory refresh is shown in Figure 23a. The transaction may be noninterleaved or interleaved (if interleaved, the PEND field must be properly filled). The transaction causes the requested row of the requested bank of *all* RDRAMs to be activated and then auto-precharged (note that the interval $t_{RP}+t_{RCD}$ should elapse since the specified bank of some RDRAMs might be open). This transaction must be repeated at intervals of $t_{REF} / (N_{BNK} \cdot N_{ROW})$, where $N_{BNK}$ and $N_{ROW}$ are the number of banks and rows in the RDRAM. This interval will be the same for the different RDRAM configurations. For each refresh transaction, the bank and row field of A35..A3 must be incremented, with the bank field changing most often so the $t_{RAS,MAX}$ parameter is not exceeded.

## Current Control

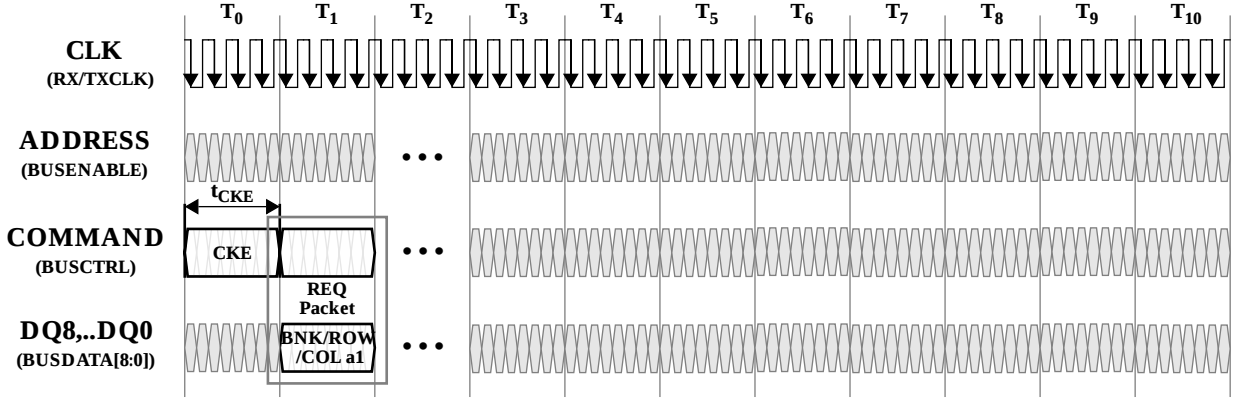
The transaction format for current control is shown in Figure 23b. This transaction is encoded as a directed register read operations, and is repeated at intervals of $t_{CCTRL} / N_{DEV}$, where $N_{DEV}$ is the number of devices on the Channel. This will maintain the optimal current control value.

| | | | |
|---|---|---|---|
| OP5..0 | $000110_2$ | A35..3 | DEV: next device |
| AUTO | 0 | | BNK: 0..0 (unused) |
| ACTV | 0 | | ROW: 0..0 (unused) |
| PEND | 000 | | COL: $00000101_2$ |
| M7..0 | $00000000_2$ | REGSEL: | 0 |

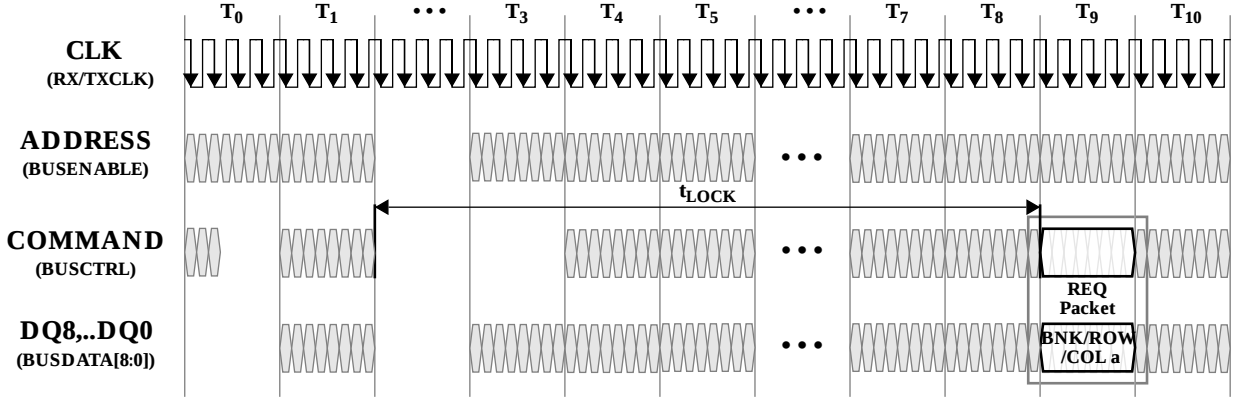
After a $t_{LOCK}$, a series of 64 of these current control transactions must be directed to each device on the Channel to establish the optimal current control value.




**(a) RESET PACKET FOR INITIALIZATION**




**(b) CKE PACKET FOR SUSPEND-TO-ENABLE POWER MODE TRANSITION**




**(c) PWRUP PACKET FOR POWERDOWN-TO-ENABLE POWER MODE TRANSITION**

**Figure 22: Transactions using RESET, CKE, and PWRUP Packets**

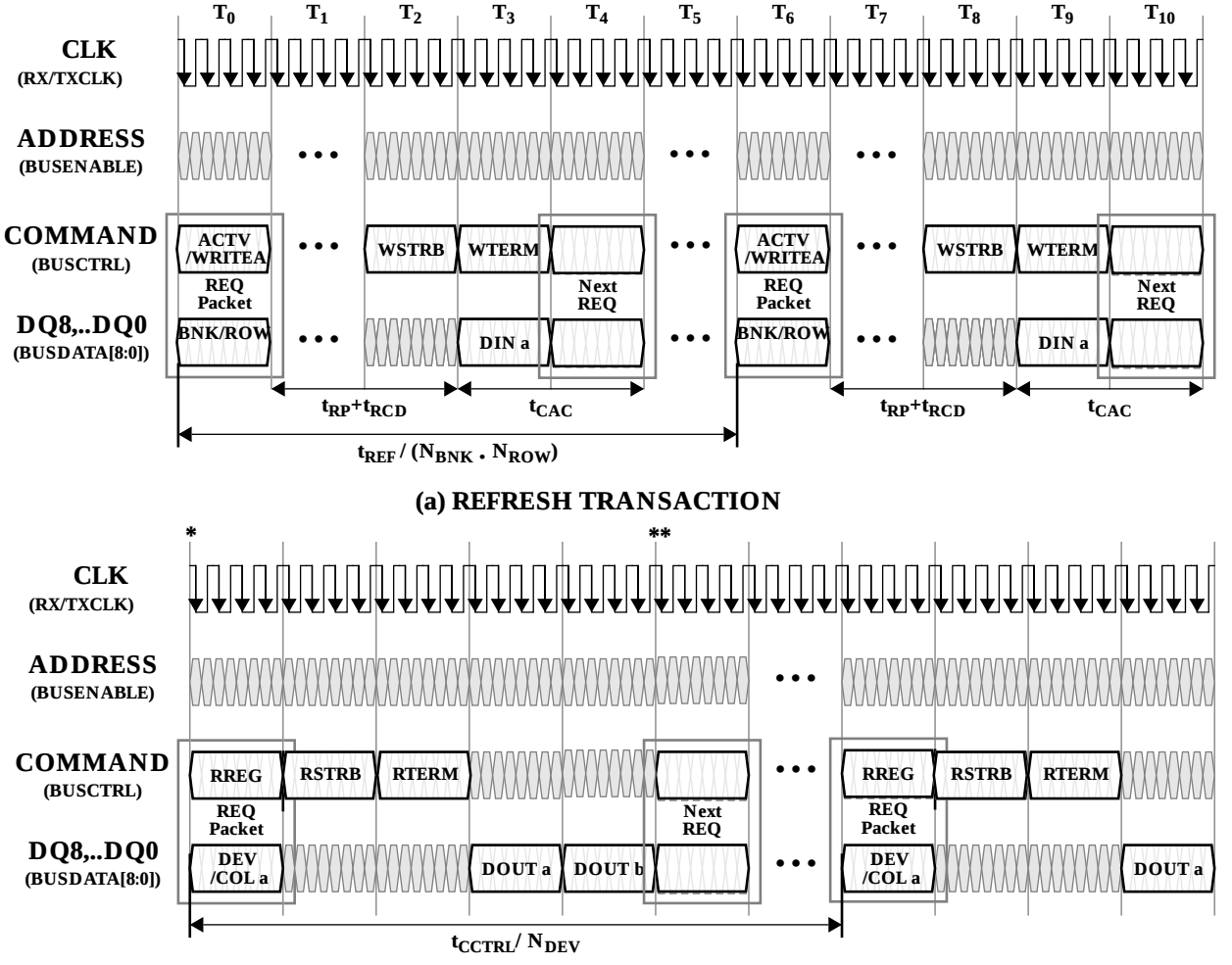



**Figure 23: Refresh and Current Control Transactions**

Due to the nature of the current control operation, a delay of 4 BusClks may be needed before and after the current control transaction.

If the request immediately before the current control request is a write request, there should be a 4 BusClks (1 Synclk) delay between the end of write data and the beginning of the RDRAM current control request (see * in Figure 23b). If the request immediately before the current control request is a read request, no delay is required.

If the current control data is followed by a request using the MODE register address, there must be a 4 BusClks (1 Synclk) delay between the end of current control data transport and the subsequent requests using the MODE register adddress (see ** in Figure 23b). Any other request may immediately follow the current control data transport.

## Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{I,ABS}$ | Voltage applied to any RSL pin with respect to Gnd | - 0.3 | $V_{DD,MAX}$+0.3 | V |
| $V_{I,CMOS,ABS}$ | Voltage applied to any CMOS pin with respect to Gnd | - 0.3 | $V_{DD}$+0.3 | V |
| $V_{DD,ABS}$ | Voltage on VDD with respect to Gnd | - 0.3 | $V_{DD,MAX}$+1.0 | V |
| $T_{J,ABS}$ | Junction temperature under bias | - 55 | 125 | °C |
| $T_{STORE}$ | Storage temperature | - 55 | 125 | °C |

## Thermal Parameters

| Symbol | Parameter and Conditions | Min | Max | Unit |
|---|---|---|---|---|
| $T_J$ | Junction operating temperature | 0 | 100 | °C |
| $\Theta_{JC}$ | Junction-to-Case thermal resistance | | 5 | °C / Watt |

## Capacitance

| Symbol | Parameter and Conditions | Min | Max | Unit |
|---|---|---|---|---|
| $C_I$ | RSL input parasitic capacitance | 1.6[a] / 2.0[b] | 2.0[a] / 2.5[b] | pF |
| $L_I$ | RSL input parasitic inductance | | 2.7[a] / 5.0[b] | nH |
| $C_{I,CMOS}$ | CMOS input parasitic capacitance | | 8 | pF |

a. 16 / 18M RDRAM.
b. 64 / 72M RDRAM.

## $I_{DD}$ - Supply Current Profile

| Mode | Description | Min | Max | Unit |
|---|---|---|---|---|
| Powerdown | Device shut down, clock unlocked | | 1.0[a] | mA |
| Suspend | Device inactive, clock locked but Suspended | | 90[a] | mA |
| Enable | Device active, clock locked and Enabled | | 270[a] | mA |
| READ | Device reading column data | | 360[a] | mA |
| WRITE | Device writing column data | | 390[a] | mA |
| ACTV / Enable | Device evaluating REQ packet and activating row in bank | | 330[a] | mA |
| ACTV / READ | Device reading column data in bank 1 and activating row in bank 2 | | 420[a] | mA |
| ACTV / WRITE | Device writing column data in bank 1 and activating row in bank 2 | | 450[a] | mA |

a. These $I_{DD}$ numbers are manufacturer-dependent; the numbers shown are representative maximum current levels at 600MB / s.

## Recommended Electrical Conditions

| Symbol | Parameter and Conditions | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$, $V_{DDA}$ | Supply voltage — 3.3-volt version | 3.15 | 3.45 | V |
| $V_{REF}$ | Reference voltage | 1.9 | $V_{DD}$ - 0.8 | V |
| $V_{IL}$ | RSL input low voltage[b] | $V_{REF}$ - 0.35 | $V_{REF}$ - 0.8 | V |
| $V_{IH}$ | RSL input high voltage[b] | $V_{REF}$ + 0.35 | $V_{REF}$ + 0.8 | V |
| $V_{IL,CMOS}$ | CMOS input low voltage | - 0.5 | 0.8 | V |
| $V_{IH,CMOS}$ | CMOS input high voltage | 1.8 | $V_{DD}$+0.5 | V |

## Electrical Characteristics

| Symbol | Parameter and Conditions | Min | Max | Unit |
|---|---|---|---|---|
| $I_{REF}$ | $V_{REF}$ current @ $V_{REF,MAX}$ | -10 | 10 | µA |
| $I_{OH}$ | RSL output high current @ ($0 \le V_{OUT} \le VDD$) | -10 | 10 | µA |
| $I_{NONE}$(manual) | RSL $I_{OL}$ current @ $V_{OUT}$ = 1.6V @ C[5:0] =000000 ($0_{10}$)[a] | 0.0 | 0.0 | mA |
| $I_{ALL}$ (manual) | RSL $I_{OL}$ current @ $V_{OUT}$ = 1.6V @ C[5:0] = 111111 ($63_{10}$)[a] | 30.0 | 80.0 | mA |
| $I_{I,CMOS}$ | CMOS input leakage current @ ($0 \le V_{I,CMOS} \le VDD$) | -10.0 | 10.0 | µA |
| $V_{OL,CMOS}$ | CMOS output voltage @ $I_{OL,CMOS}$= 1.0mA | 0.0 | 0.4 | V |
| $V_{OH,CMOS}$ | CMOS output high voltage @ $I_{OH,CMOS}$= -0.25mA | 2.0 | $V_{DD}$ | V |

a. In manual-calibration mode (CCEnable=0) this is the value written into the C[5:0] field of the Mode register to produce the indicated $I_{OL}$ value. Values of $I_{OL}$ in between the $I_{NONE}$ and $I_{ALL}$ are produced by interpolating C[5:0] to intermediate values. For example, C[5:0] = 011111 ($31_{10}$) produces an $I_{OL}$ in the range of 20 to 40mA.

b. IOL of BusData outputs is set at 30mA when BusEnable pin
VIH / VIL value is measured.

## Recommended Timing Conditions

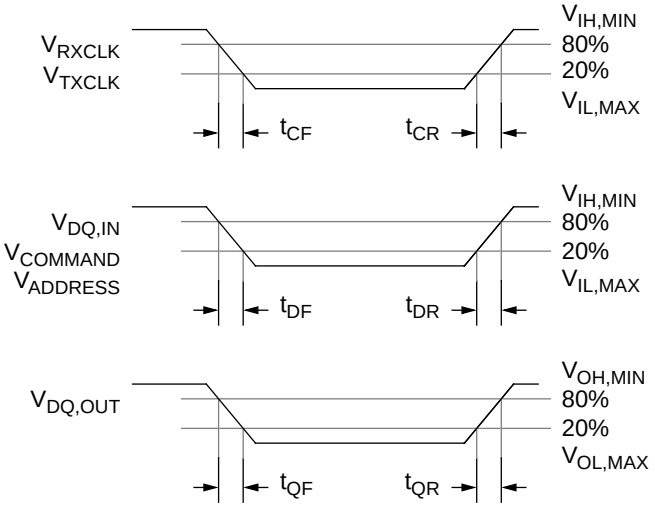
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{CR}$, $t_{CF}$ | TXCLK and RXCLK input rise and fall times | 0.3 | 0.8 | ns |
| $t_{CYCLE}$ | TXCLK and RXCLK cycle times | 3.75[a] / 3.33[b] | 4.15[a] / 4.15[b] | ns |
| $t_{TICK}$ | Transfer time per bit per pin (this timing interval is synthesized by the RDRAM's clock generator) | 0.5 | 0.5 | $t_{CYCLE}$ |
| $t_{CH}$, $t_{CL}$ | TXCLK and RXCLK high and low times | 45% | 55% | $t_{CYCLE}$ |
| $t_{TR}$ | TXCLK-RXCLK differential | 0 | 0.7 | $t_{CYCLE}$ |
| $t_{PACKET}$ | Transfer time for REQ, DIN, DOUT, COL, WSTRB, WTERM, RSTRB, RTERM, CKE,PWRUP and RESET packets | 4 | 4 | $t_{CYCLE}$ |
| $t_{DR}$, $t_{DF}$ | DQ / ADDRESS / COMMAND input rise and fall times | 0.3 | 0.6 | ns |
| $t_S$ | DQ / ADDRESS / COMMAND-to-RXCLK setup time | 0.35[c] | | ns |
| $t_H$ | RXCLK-to-DQ / ADDRESS / COMMAND hold time | 0.35[c] | | ns |
| $t_{REF}$ | Refresh interval | | 17[d] / 33[e] | ms |
| $t_{SCYCLE}$ | Powerdown refresh cycle time | 0.4 | 16.6[d] / 8.0[e] | µs |
| $t_{SL}$ | Powerdown refresh low time | 0.2 | 10 | µs |
| $t_{SH}$ | Powerdown refresh high time | 0.2 | 10 | µs |
| $t_{CCTRL}$ | Current control interval | | 150 | ms |
| $t_{RAS}$ | RAS interval (time a row may stay activated) | | 133 | µs |
| $t_{LOCK}$ | RDRAM clock-locking time for reset or powerup | | 5.0 | µs |

a. -533 MHz RDRAM
b. -600 MHz RDRAM
c. 600MHz IO timing
d. 16 / 18Mbit with 2KByte page
e. 1 64 / 72Mbit with 2KByte page

## Timing Characteristics

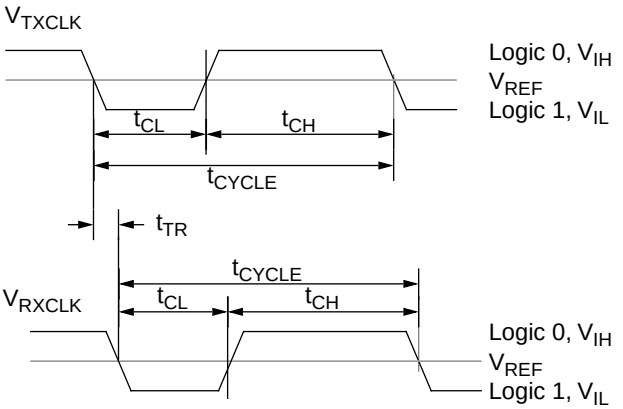
| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PIO}$ | SIn-to-SOut delay @ $C_{LOAD,CMOS= 40pF}$ | | 25 | ns |
| $t_Q$ | DQ output time | -0.4ns[a] | +0.4ns[a] | ns |
| $t_{QR}$, $t_{QF}$ | DQ output rise and fall times | 0.3 | 0.5 | ns |

a. 600MHz IO timing

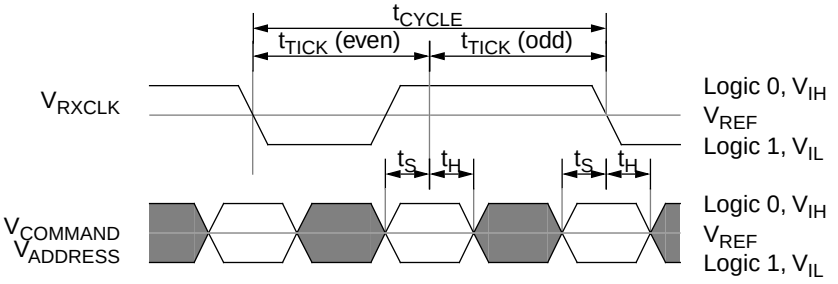



Where:
$V_{OH,MIN} = V_{TERM,MIN}$
$V_{OL,MAX} = V_{TERM,MAX} - Z_O * (I_{OL,MIN})$

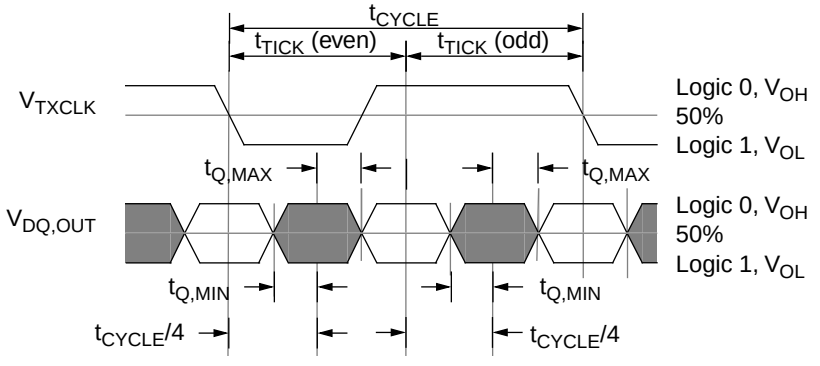
**(a) RSL Transition (Rise/Fall) Timing**




**(b) RSL Clock Timing**

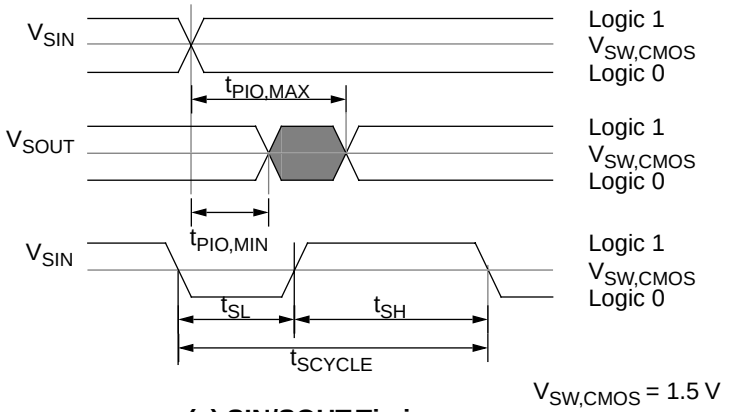



**(c) RSL Input (Receive) Timing**




**(d) RSL Output (Transmit) Timing**

**Figure 24: RSL Timing Parameters**




**(a) SIN/SOUT Timing**

**Figure 25: SIN/SOUT Timing**

## Timing Characteristics

Note: All units are $t_{CYCLE}$ when not mentioned

| Symbol and Figure | Parameter | Min | Max |
|---|---|---|---|
| $t_{CAC}$ - Figure 9,10 | Column ACcess time. May overlap $t_{RCD}$, $t_{RP}$, or $t_{RPA}$ to another bank | 6[a] / 7[b] | |
| $t_{CC}$ - Figure 9,10 | Column Cycle time. May overlap $t_{RCD}$, $t_{RP}$, or $t_{RPA}$ to another bank | 4 | |
| $t_{RCD}$ - Figure 9,10 | Row to Column Delay. May overlap $t_{CAC}$ or $t_{CC}$ to another bank | 8 | |
| $t_{RP}$ - Figure 9,10 | Row Precharge time. May overlap $t_{CAC}$ or $t_{CC}$ to another bank | 8 | |
| $t_{RPA}$ - Figure 9,10 | Row Precharge Auto. May overlap $t_{RPA}$, $t_{CAC}$ or $t_{CC}$ to another bank | 8 | |
| $t_{RAC}$ - Figure 9,10 | Row ACcess time ($t_{RAC} = t_{RCD} + t_{CAC}$). | 15 | |
| $t_{RC}$ - Figure 9,10 | Row Cycle time ($t_{RC} = t_{RP} + t_{RCD} + t_{CAC}$). | 23 | |
| $t_{RSR}$ - Figure 9a | Start of REQ (RREAD) to start of R**S**TRB packet for Read transaction. | 2 | |
| $t_{ASR}$ - Figure 9b | Start of REQ (ACTV / READ) to start of R**S**TRB packet for Read transaction. | 11 | |
| $t_{PSR}$ - Figure 9c | Start of REQ (PRE / ACTV / READ) to start of R**S**TRB packet for Read transaction. | 19 | |
| $t_{CDR}$ - Figure 9abc | Start of COL packet to start of **D**OUT packet for Read transaction. | 12 | 12 |
| $t_{SDR}$ - Figure 9abc | Start of RSTRB packet to start of **D**OUT packet for Read transaction. | 8 | 8 |
| $t_{TDR}$ - Figure 9abc | Start of RTERM packet to end of **D**OUT packet for Read transaction. | 12 | 12 |
| $t_{WSW}$ - Figure 10a | Start of REQ (WRITE) to start of W**S**TRB packet for Write transaction. | 0 | |
| $t_{ASW}$ - Figure 10b | Start of REQ (ACTV / WRITE) to start of W**S**TRB packet for Write transaction. | 5 | |
| $t_{PSW}$ - Figure 10c | Start of REQ (PRE / ACTV / WRITE) to start of W**S**TRB packet for Write transaction. | 13 | |
| $t_{CDW}$ - Figure 10abc | Start of COL packet to start of **D**IN packet for Write transaction. | 8 | 8 |
| $t_{SDW}$ - Figure 10abc | Start of WSTRB packet to start of **D**IN packet for Write transaction. | 4 | 4 |
| $t_{TDW}$ - Figure 10abc | Start of WTERM packet to end of **D**IN packet for Write transaction. | 4 | 4 |
| $t_{RESET}$ - Figure 22a | Length of RESET packets to cause RDRAM to reset. | 800 ns | |
| $t_{CKE}$ - Figure 22b | Start of CKE packet to start of REQ packet for Suspend-to-Enable. | 4 | 7 |
| $t_{PWRUP}$ - Figure 22c | Length of PWRUP packets to cause Powerdown-to-Enable. | 8 | 8 |
| $t_{WREG}$ - Figure 15b | End of DIN packet for WREG transaction to start of next REQ packet. | 16 | |

a. For READ, WRITE commands
b. For ACTV / READ, ACTV / WRITE, PRE / ACTV / READ, PRE / ACTV / WRITE commands

## Mechanical Drawings

The RDRAM is available in both horizontal and vertical surface mount plastic packages. Dimensions for the Horizontal surface mount plastic package are shown below.

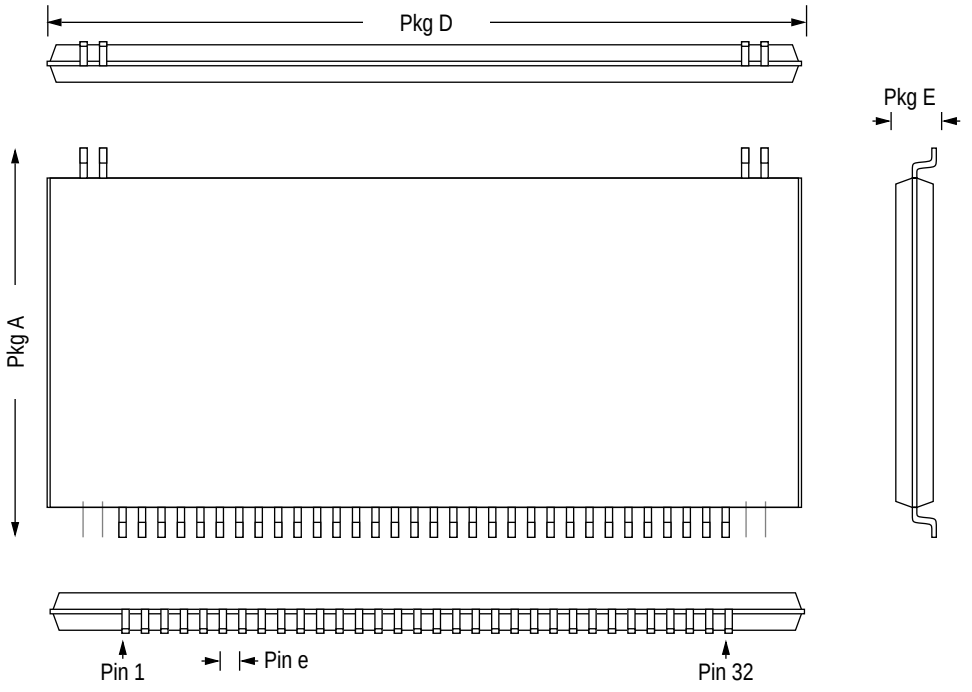



**Figure 26: SHP-32 Package**

The next figure shows the footprint of the SHP-32 package. Plane R-R is the electrical reference plane of the device on the center line of the SMT pads.

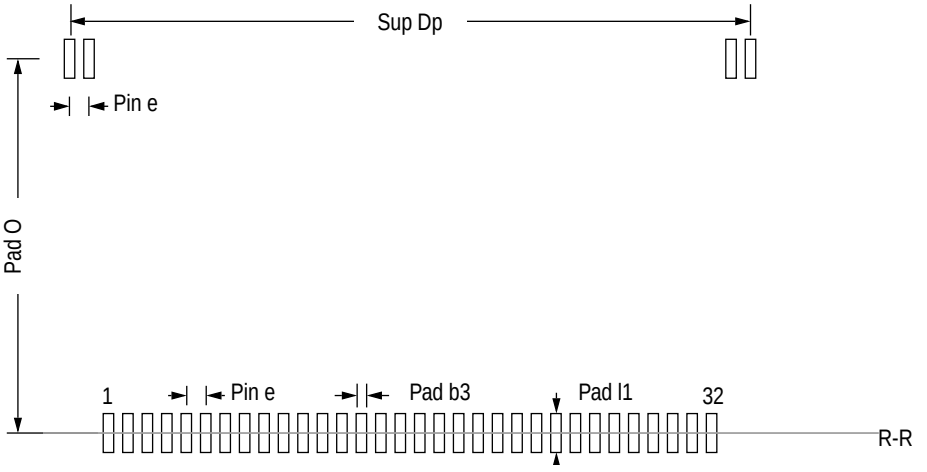



**Figure 27: SHP-32 Footprint**

This table summarizes the values of the package and footprint dimensions[3].

**Table 4: SHP-32 Package Dimensions**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Pin e | Pin pitch | 0.65 | 0.65 | mm |
| Pkg D | Package width | 24.9 | 25.3 | mm |
| Pkg A | Package total height | 12.9 | 13.1 | mm |
| Pkg E | Package thickness | - | 1.7 | mm |
| Pad b3 | SMT pad width | 0.30 | 0.40 | mm |
| Pad l1 | SMT pad length | 1.2 | 1.4 | mm |
| Sup Dp | Support pad outer pitch | 22.75 | 22.75 | mm |
| Pad O | SMT pad offset | 12.5 | 12.5 | mm |

The next figure summarizes the dimensions of the EIAJ standard SVP-32 package as used in the RDRAM. Refer to the EIAJ specifications for more details of the package dimensions and recommended footprint.

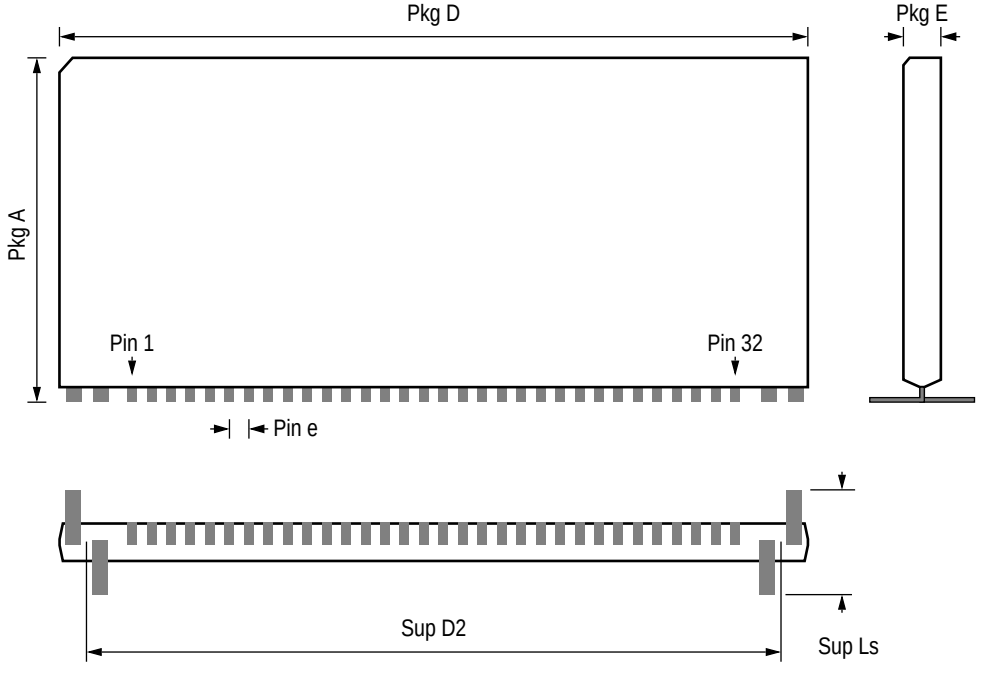



**Figure 28: SVP-32 Package**

3. All the support pad dimensions are provisional.

The figure below shows the footprint of the SVP-32 package. Plane R-R is on the center line of both the package and support leads, and offset from the center line of the SMT pads. Plane R-R is also the electrical reference plane of the device.

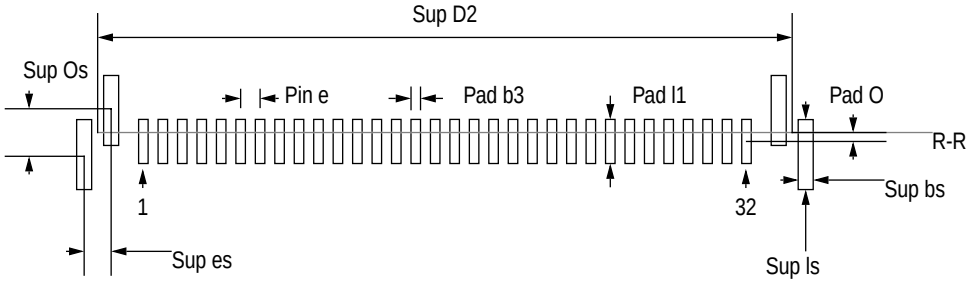



**Figure 29: SVP-32 Footprint**

This table summarizes the values of the package and footprint dimensions[4].

**Table 5: SVP-32 Package Dimensions**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| Pin e | Pin pitch | 0.65 | 0.65 | mm |
| Pkg D | Package width | 24.9 | 25.3 | mm |
| Pkg A | Package total height | 11.3 | 11.8 | mm |
| Pkg E | Package thickness | 1.2 | 1.4 | mm |
| Sup Ls | Support lead span | 3.4 | 3.6 | mm |
| Sup D2 | Support lead spacing | 23.15 | 23.25 | mm |
| Pad b3 | SMT pad width | 0.27 | 0.35 | mm |
| Pad l1 | SMT pad length | 1.4 | 1.55 | mm |
| Sup bs | Support pad width | 0.45 | 0.55 | mm |
| Sup ls | Support pad length | 2.1 | 2.3 | mm |
| Pad O | SMT pad offset | 0.25 | 0.35 | mm |
| Sup Os | Support pad offset | 1.55 | 1.65 | mm |
| Sup es | Support pad pitch | 0.90 | 0.90 | mm |

4. All the support pad dimensions are provisional.

## Document Change History

| Date | Version | Page | Description |
|---|---|---|---|
| 09-04-97 | DL0029-06 | | Previous update |
| 04-02-98 | -07 | – | Document changed from “Advance Information” to “Preliminary Information” |
| | -07 | 24 | Current Control section, OP5..0 $000010_2$ changed to OP5..0 $000110_2$ |
| | -07 | 28 | Recommended Electrical Conditions Table, footnote “b” added to $V_{IL}$ and $V_{IH}$. |
| | -07 | 28 | Electrical Characteristics Table, $I_{ALL}$ Min changed to 30.0 from 40.0 mA. |
| | -07 | 29 | Recommended Timing Considerations Table, $t_{REF}$ values changed: 32 ms deleted and 64 ms changed to 33 ms. |
| | -07 | 29 | Recommended Timing Considerations Table, $t_{SCYCLE}$ Min changed to 0.4 µs and Max changed to 16.6/8 from 15 µs. |
| | -07 | 29 | Recommended Timing Considerations Table, $t_{SL}$ Min changed from 5.6 to 0.2 µs. |
| | -07 | 29 | Recommended Timing Considerations Table, $t_{SH}$ Min changed from 5.6 to 0.2 µs. |



DL0029-07

Rambus Inc.
2465 Latham Street
Mountain View, California USA
94040

Telephone: 650-944-8000
Fax: 650-944-8080
http://www.rambus.com

*Written by: Frederick A. Ware*